CHAPTER – 2
OPERATIONAL TRANSRESISTANCE AMPLIFIER
2.1 INTRODUCTION

Ever since its development the operational amplifier (op-amp) is an integral part of analog signal processing and generating circuits. It is intended to implement closed loop voltage processing circuits which are known as voltage-mode (VM) circuits. However, high frequency performance of these circuits is limited due to constant gain-bandwidth product and low slew rate of the op-amps. The attempt to overcome this problem has led to the development of current-mode (CM) signal processing. In CM signal processing, current is used as the active variable in preference to voltage, either throughout the circuit or only in certain critical areas [72]. CM techniques can achieve a considerable improvement in system performance in terms of bandwidth, signal linearity, slew rate and power consumption. Consequently, CM signal processing has progressed considerably in past few decades and has resulted in emergence of various CM analog building blocks [4] and OTRA [36] among those is of relatively recent origin. The OTRA is a high gain current input voltage output device. Both input and output terminals of the OTRA are characterized by low impedance resulting in circuits that are insensitive to stray capacitances making OTRA appropriate for high frequency applications.

In order to maintain compatibility with existing voltage processing circuits, it is necessary to convert the input and output signals of current-mode circuits to voltage, using transconductors and transresitors respectively. This has the disadvantage of increasing both the chip area and power dissipation. However, circuits using OTRA as the active element benefit from the current processing capabilities at the input terminals, and can directly drive the existing VM signal processing circuits thus eliminating the requirement of additional circuitry and associated power consumption, at the output.

In this chapter OTRA has been dealt with in detail. The ideal OTRA is introduced first which is followed by its nullor based model. This model can be used in CAD tools to compute fully-symbolic small-signal characteristics of OTRA-based analog circuits. The existing OTRA realizations have been taken up later. Few basic applications of the OTRA such as voltage amplifiers, adder, subtractor, and integrator circuits are also described. The chapter
concludes with description of passive resistor realization in OTRA based circuits with its MOS based counterpart thereby making circuits suitable from integration viewpoint.

**2.2 THE IDEAL OTRA**

The circuit symbol of an OTRA [36] is shown in Fig. 2.1(a). An Ideal OTRA senses the difference of the currents at its two input terminals, namely p and n, amplifies it and provides a resulting voltage at the output terminal. For ideal operations the input terminal voltages should be zero. Additionally the output voltage should be independent of the current that may be drawn from the output terminal by the load impedance. Putting together, an equivalent OTRA circuit model can be drawn as shown in Fig. 2.1(b) and the port characteristics of OTRA can be expressed by (2.1) where $R_m$ is transresistance gain of OTRA. For ideal operations the $R_m$ approaches infinity and forces the input currents to be equal.

\[
\begin{bmatrix}
V_p \\
V_n \\
V_o
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
0 & 0 & 0 \\
R_m & -R_m & 0
\end{bmatrix}
\begin{bmatrix}
I_p \\
I_n \\
I_o
\end{bmatrix}
\]

(2.1)

Though the above idealized conditions can not be realized in practice yet the use of such an ideal OTRA model simplifies the mathematical analysis of OTRA circuits. The practical OTRA circuits are made to approximate the idealized characteristics. The equivalent circuit model of a practical OTRA is shown in Fig. 2.2 where $R_p$ and $R_n$ represent terminal resistances of p and n ports respectively.

OTRA in the simplest way can be used in an open loop configuration; however, its gain being infinity the output voltage saturates either at positive or negative saturation level. This operation has a limited number of applications. Thus OTRA must be used in a negative feedback configuration where the output is not driven into saturation and the circuit behaves linearly. Since the OTRA has a current input and voltage output a shunt- shunt feedback configuration is used which places the feedback network and amplifier in parallel. A parallel configuration is suitable for low voltage operations as it minimizes stacking of transistors thereby providing more head room for signal swing [37]. Also using current feedback techniques OTTRAs have a bandwidth almost independent of closed-loop gain.
2.3 NULLOR BASED OTRA MODEL

The nullor is an ideal element which is composed of a nullator, connected at the input port and a norator, connected at the output port, as shown in Fig. 2.3 (a) [73]. The terminal characteristics of nullator can be represented as

\[ V_b = V_a = \text{arbitrary} \quad \text{and} \quad I_b = I_a = 0 \] (2.2)

Similarly the terminal equations for the norator can be expressed as

\[ V_d \neq V_c = \text{arbitrary} \quad \text{and} \quad I_d = -I_c \] (2.3)
Fig. 2.3 Pathological elements [73]. (a) Nullor. (b) VM-CM pair.

The nullor with inverting characteristics can be implemented with voltage mirror-current mirror (VM-CM) pair as shown in Fig. 2.3(b) [73]. This pair is also an ideal element and it is composed of a VM at the input port and a CM at the output port. The VM and CM can be characterized by (2.4) and (2.5) respectively

\[
V_b = -V_a = \text{arbitrary and } I_b = I_a = 0
\]  
\[
V_d \neq V_c = \text{arbitrary and } I_d = I_c
\]  

The VM-CM can also be modeled using nullators, norators along with unity grounded resistors as shown in Fig. 2.4.

Fig. 2.4 Nullor based models [73] of (a) Voltage mirror (VM). (b) Current mirror (CM).

The nullators, norators and VM-CM pair collectively are known as pathological elements. The behavior of active devices can be modeled using pathological elements. Thus the analog circuits can be transformed to nullor and/or VM-CM pairs based equivalent circuits and symbolic analysis techniques can be applied to approximate smallsignal characteristics of
these analog circuits. The nullor based model of OTRA [71] is shown in Fig. 2.5. According to the nullor concept if one terminal of a nullator is connected to signal-ground, the other terminal is considered as a virtual ground; therefore, a node of low impedance is obtained. Also, nullator does not allow current to flow through it. In OTRA the currents $I_p$ and $I_n$ enter into the low impedance input terminals. This can be modeled with the nullor if one terminal of the nullator is connected to signal-ground and the input current is flowing through the norator. Hence, both the input terminals can be modeled with current followers (CFs), as shown in Fig. 2.5. The output voltage is the difference of the input currents multiplied by the transresistance gain, $R_m$, which is ideally infinity; therefore, a change of direction of $I_n$ must be required to force the input currents to be equal. A current mirror as shown in Fig. 2.4 (b) is used to reverse the direction of $I_n$. A voltage follower consisting of a nullor is used at the output terminal, where the current difference is transformed to voltage by $R_m$.

![Fig. 2.5 Nullor based model of OTRA [71].](image)

### 2.4 NONIDEAL MODEL OF OTRA

The transresistance gain $R_m$ of an OTRA should ideally be infinity. However, in practice it is finite and its effect along with the frequency limitations associated with the OTRA must be considered [36]. Thus the $R_m$ can be represented using a single-pole model given by
\[ R_m(s) = \left( \frac{R_0}{1 + \frac{s}{\omega_0}} \right) \]  
(2.6)

where \( R_0 \) is DC open loop transresistance gain. For high frequency applications, the transresistance gain, \( R_m(s) \), can be expressed as

\[ R_m(s) \approx \left( \frac{1}{s/R_0 \omega_0} \right) = \left( \frac{1}{sC_p} \right); \quad C_p = \frac{1}{R_0 \omega_0} \]  
(2.7)

The \( C_p \) is called the parasitic capacitance of OTRA.

### 2.5 OTRA IMPLEMENTATION

In this section a review of existing literature on OTRA implementation is presented. An extensive review suggests that various implementations of OTRA are available in literature and are based on:

(i) Using commercially available AD844 (CFOA) ICs [35].

(ii) Using integrated circuit implementations [27], [36] – [40].

#### 2.5.1 CFOA Based Realization

CFOAs are commercially available as IC AD844. The circuit symbol of CFOA is shown in Fig. 2.6 and the port relations of a CFOA can be characterized by

\[ V_x = V_y; \quad I_y = 0; \quad I_z = I_x; \quad V_w = V_z \]  
(2.8)

![CFOA circuit Symbol](image)
The OTRA can be realized using two AD844 CFOA ICs as shown in Fig. 2.7 [35]. From Fig. 2.7 various currents can be calculated as

\[ I_{z1} = I_p \] (2.9)

\[ I_{x2} = I_n - I_{x1} \] (2.10)

\[ I_{z2} = I_{x2} \] (2.11)

From (2.9) and (2.10), the current through \( z_2 \) terminal can be computed as

\[ I_{z2} = I_n - I_p \] (2.12)

The voltages at various ports may be written as

\[ V_p = V_{1-} = V_{1+} = 0 \] (2.13)

\[ V_n = V_{2-} = V_{2+} = 0 \] (2.14)

\[ V_o = V_{z2} = -I_{z2}R_{z2} = (I_p - I_n)R_{z2} \] (2.15)

Fig. 2.7 OTRA realization using CFOA AD844 [35].
Ideally the input resistance at the x terminal of CFOA is zero and is infinite at the z terminal. However for the AD844 CFOA the input resistance $R_x$ is around 50 $\Omega$ and $R_z$ is around 3 M$\Omega$ [74].

Fig. 2.8 Equivalent circuit of OTRA constructed with AD844 [66].

To investigate the effect of the parasitic resistances ($R_x$ and $R_z$), the CFOAs have been replaced with current conveyors having finite input resistances ($R_x$) and finite resistance at its z terminal ($R_z$) in Fig. 2.7 and the equivalent circuit model [66] with parasitics for non ideal analysis is presented in Fig. 2.8. From Fig. 2.8 various currents can be computed as

\[ I_{z1} = I_p \]  
(2.16)

\[ I_D = I_{z1} \left( \frac{R_{z1}}{R_{x2} + R_{z1}} \right) \]  
(2.17)

\[ I_{x2} = I_n - I_D \]  
(2.18)

\[ I_{z2} = I_{x2} \]  
(2.19)
Ideally $I_D$ should be equal to $I_{z1}$, which can be approximated only if $R_{z1} \gg R_{x2}$, which is true for AD844. Also the approximation that the input terminals are virtually grounded will be true only if the external resistance at the input terminal of the OTRA is much larger than $R_X$. If these two conditions are satisfied the OTRA constructed with AD844 closely approximates an ideal OTRA. From (2.16), (2.17), (2.18) and (2.19) the output voltage $V_o$, taking into account the above mentioned approximations, can be calculated as

$$V_o = (I_p - I_n)R_{z2}$$

(2.20)

where $R_{z2}$ is the transresistance gain of the OTRA.

### 2.5.2 Integrated Circuit Implementation

Various integrated circuit implementations of OTRA [27], [36]–[40] are available in literature and are briefly described in this section. The OTRA implementation of [27] consists of a differential current controlled current source followed by a voltage buffer. The OTRA proposed in [36] is based on cascaded connection of the modified differential current conveyor (MDCC) [41] and a common source amplifier. The MDCC provides the current differencing operation whereas the common source amplifier provides the high gain stage [36]. The OTRA presented in [37] consists of a low voltage regulated cascode current mirror with a low voltage regulated cascode load as the core of the circuit, common source amplifiers gain boosting stage and level shifters followed by common source output stage [37]. The OTRA structure available in [38] is similar to [36] but uses smaller number of current mirrors than [36]. This reduces the transistor mirror mismatch effect and also increases the frequency capabilities. Due to smaller number of transistors the power dissipation is also reduced. The CMOS OTRA realization in [39] uses same input stage as in [38] while a differential gain stage is used instead of the single common source amplifier. This differential stage reduces the DC offset current and increases the DC open loop transresistance gain. Yet another differential OTRA structure is proposed in [40]. It uses two symmetrically placed basic input cells consisting of four transistors each. Each cell forms two Class AB current mirror connections. This basic input unit is followed by four similar basic cells to decrease the process variation effects [40]. Gain is provided using three stages of differential amplifier. The non buffered, dual differential outputs are buffered through
unity gain configurations which are designed using CMOS op-amps [40]. This structure is a completely differential design.

### 2.6 CMOS OTRA [38] USED IN THIS WORK

This section describes the OTRA implementation used to verify the functionality of all the circuit structures proposed in this thesis. The CMOS based OTRA structure proposed in [38] has been reproduced in Fig. 2.9. The circuit operation is based on the assumptions that all the transistors (M1-M14) operate in saturation region and the transistor groups (M1-M3), (M5 and M6), (M8-M11) and (M12 and M13) are perfectly matched. Transistors M8-M11 form current mirrors wherein the transistor M8 sets the reference current $I_B$ which is repeated by M9-M11 thus forcing equal currents in the transistors M1, M2 and M3. This provides the gate to source voltages of M1, M2 and M3 and, consequently, forces the two input terminals to be virtually grounded. The current mirrors formed by the transistor pairs M10-M11 and M12-M13 provide the current differencing operation, thus developing gate to source voltage for M14 which is connected as common source amplifier and provides the high gain.

![CMOS Realization of OTRA Proposed in [38]](image)

**Fig. 2.9** CMOS Realization of OTRA Proposed in [38].

### 2.6.1 OTRA Characterization

The SPICE simulation is performed using 0.5µm, CMOS process parameters provided by MOSIS (AGILENT) which are listed in Table 2.1. Supply voltages for simulations are taken
as \( \pm 1.5 \) V. Aspect ratios used for different transistors are same as in [38] and are given in Table 2.2.

Table 2.1: Device Model parameters.

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Model parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS LEVEL=3 UO=460.5 TOX=1E-8 TPG=1 VTO=.62 JS=1.8E-6 XJ=.15E-6 RS=417 RSH=2.73 LD=4E-8 ETA=0 VMAX=130E3 NSUB=1.71E17 PB=.761 PHI=.905 THETA=.129 GAMMA=.69 KAPPA=0.1 AF=1 WD=1.1E-7 CJ=76.4E-5 MJ=.357 CJSW=5.68E-10 MJSW=.302 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 DELTA=0.42 NFS=1.2E11</td>
<td></td>
</tr>
<tr>
<td>PMOS LEVEL=3 UO=100 TOX=1E-8 TPG=1 VTO=-.58 JS=.38E-6 XJ=.1E-6 RS=886 RSH=1.81 LD=3E-8 ETA=0 VMAX=113E3 NSUB=2.08E17 PB=.911 PHI=.905 THETA=.12 GAMMA=.76 KAPPA=2 AF=1 WD=1.4E-7 CJ=85E-5 MJ=.429 CJSW=4.67E-10 MJSW=.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29 DELTA=0.81 NFS=.52E11</td>
<td></td>
</tr>
</tbody>
</table>

Table 2.2: Aspect ratio of the transistors in OTRA circuit.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W(( \mu )m)/L(( \mu )m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M3</td>
<td>100/2.5</td>
</tr>
<tr>
<td>M4</td>
<td>10/2.5</td>
</tr>
<tr>
<td>M5,M6</td>
<td>30/2.5</td>
</tr>
<tr>
<td>M7</td>
<td>10/2.5</td>
</tr>
<tr>
<td>M8-M11</td>
<td>50/2.5</td>
</tr>
<tr>
<td>M12,M13</td>
<td>100/2.5</td>
</tr>
<tr>
<td>M14</td>
<td>50/0.5</td>
</tr>
</tbody>
</table>

The DC transfer characteristic of the OTRA is shown in Fig. 2.10 which shows that input differential current range is \(-50 \) \( \mu \)A to \( 50 \) \( \mu \)A. The input resistance is plotted in Fig. 2.11 and
its value is observed to be 13 Ω. The AC characteristic is shown in Fig. 2.12. It shows that the DC open loop transresistance gain is 95.8 dBΩ. The gain bandwidth product equals 19.56 GHz Ω. The power dissipation of the circuit is 1.17 mW. These results are summarized in Table 2.3.

![Graph of DC Transfer Characteristics in (a) Noninverting, (b) Inverting configuration.](image-url)
Table 2.3: Simulated results of the circuits shown in Fig. 2.9.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input current dynamic range</td>
<td>-50 to 50 μA</td>
</tr>
<tr>
<td>Input resistances $R_p, R_n$</td>
<td>$\approx 13 \Omega$</td>
</tr>
<tr>
<td>DC open loop transresistance</td>
<td>95.8 dBΩ</td>
</tr>
<tr>
<td>Gain bandwidth product</td>
<td>19.56 GHzΩ</td>
</tr>
<tr>
<td>Transresistance gain B.W. (-3dB)</td>
<td>317 KHz</td>
</tr>
<tr>
<td>Total power dissipation</td>
<td>1.17 mW</td>
</tr>
</tbody>
</table>
2.7 BASIC CIRCUIT APPLICATIONS

This section describes the basic circuit applications of OTRA which have been used in this thesis.

2.7.1 Inverting Voltage Amplifier

An inverting amplifier is shown in Fig. 2.13. It consists of an OTRA and two resistors $R_1$ and $R_2$ where $R_2$ is connected from output to negative input terminal $n$, thus closing the loop around OTRA. The current at terminal $n$ can be computed as

$$i_n = \frac{v_{in}}{R_1} + \frac{v_o}{R_2} \quad (2.21)$$

And the current at terminal $p$ can be expressed as

$$i_p = 0 \quad (2.22)$$

Assuming the OTRA to be ideal, voltage gain of the amplifier can be computed by equating the currents of $p$ and $n$ terminal resulting in

$$\frac{v_{in}}{R_1} + \frac{v_o}{R_2} = 0 \quad (2.23)$$

Thus the close loop inverting gain can be computed to be

$$\frac{v_o}{v_{in}} = -\frac{R_2}{R_1} \quad (2.24)$$
2.7.2 Noninverting Voltage Amplifier

A noninverting amplifier consists of an OTRA and two resistors $R_1$ and $R_2$ as shown in Fig. 2.14. The current at terminal n and p can respectively be computed as

$$i_n = \frac{v_o}{R_2} \quad (2.25)$$

$$i_p = \frac{v_{in}}{R_1} \quad (2.26)$$

Assuming the OTRA to be ideal, voltage gain of the amplifier can be computed as

$$\frac{v_{in}}{R_1} = \frac{v_o}{R_2} \quad (2.27)$$

Thereby resulting in voltage gain as

$$\frac{v_o}{v_{in}} = \frac{R_2}{R_1} \quad (2.28)$$

2.7.3 The Summing Amplifier

An OTRA based summer is shown in Fig. 2.15 and can be used as a weighted summer. The circuit makes use of a single OTRA, a feedback resistor $R_F$ and N feed- in resistors ($R_1$ to $R_N$) through which input signals $v_1$ to $v_N$ are applied. By equating the current at the inverting and the non inverting terminal, the output voltage can be obtained as given by (2.29) which can be further simplified to (2.30) if $R_1 = R_2 = \ldots = R_N = R_F = R$.

![Fig. 2.15 The summing amplifier.](image)

![Fig. 2.16 The difference amplifier.](image)
\[ v_O = \frac{R_F}{R_1} v_1 + \frac{R_F}{R_2} v_2 + \cdots + \frac{R_F}{R_N} v_N \]  
\[ (2.29) \]

\[ v_O = v_1 + v_2 + \cdots + v_n \]  
\[ (2.30) \]

### 2.7.4 The Difference Amplifier

Considering the OTRA to be ideal the output voltage for the circuit shown in Fig. 2.16, can be expressed as

\[ v_O = \frac{R_F}{R_1} v_1 - \frac{R_F}{R_2} v_2 \]  
\[ (2.31) \]

Thus the circuit can be used as a difference amplifier with a gain of \( \frac{R_F}{R} \) if \( R_1 = R_2 = R \) and the output voltage can be written as

\[ v_O = \frac{R_F}{R} (v_1 - v_2) \]  
\[ (2.32) \]

The circuit of Fig. 2.16 can also be used as a subtractor if \( R_1 = R_2 = R_F \) and the output voltage can be expressed as

\[ v_O = (v_1 - v_2) \]  
\[ (2.33) \]

### 2.7.5 Lossy Integrator

The circuit shown in Fig. 2.17(a) represents an inverting lossy integrator. Assuming the OTRA to be ideal and using the concept of current feedback, the transfer function can be computed as

\[ \frac{v_o}{v_{in}} = -\left(\frac{R_F}{R}\right) \left(1 + sCR\right) \]  
\[ (2.34) \]

From (2.34) the DC gain (K) of the integrator can be found to be

\[ K = -\frac{R_F}{R} \]  
\[ (2.35) \]

And the 3-dB frequency (\( \omega_0 \)) is observed to be

\[ \omega_0 = \frac{1}{CR} \]  
\[ (2.36) \]
Applying input voltage at p terminal of OTRA a noninverting integrator can be realized as depicted in Fig. 2.17(b) and its transfer function can be expressed as

\[
\frac{v_o}{v_{in}} = \left(\frac{R_F}{R}\right) \frac{1+sCR}{1+sCR}
\]

having a non-inverting DC gain of \( K = \frac{R_F}{R} \) and \( \omega_0 \) being same as (2.36).

![Fig. 2.17 Lossy integrator configurations (a) Inverting. (b) Noninverting.](image)

### 2.8 ACTIVE RESISTOR REALIZATION USING OTRA

It is well know that the linear passive resistor consumes a large chip area as compared to the linear resistor implementation using transistors operating in non-saturation region. The current differencing property of the OTRA allows the resistors connected to the input terminals of OTRA to be implemented using MOS transistors with complete non-linearity cancellation [36].

The circuit configuration of Fig. 2.18 shows MOS based resistor realization. Assuming that \( M_a \) and \( M_b \) are matched transistors and operating in ohmic region the currents \( I_a \) and \( I_b \) [75] can be expressed as

\[
I_a = K_n(V_a - V_T)(V_{DSa}) + x_1V_{DSa}^2 + x_2V_{DSa}^3 + \cdots
\]

\[
= K_n(V_a - V_T)(V_1 - V_2) + x_1(V_1 - V_2)^2 + x_2(V_1 - V_2)^3 + \cdots
\]
\[ I_b = K_n(V_b - V_T)(V_{DSb}) + x_1V_{DSb}^2 + x_2V_{DSb}^3 + \cdots \]

\[ = K_n(V_b - V_T)(V_1 - V_2) + x_1(V_1 - V_2)^2 + x_2(V_1 - V_2)^3 + \cdots \]  \hspace{1cm} (2.39)

where \( K_n = \mu C_{OX} \frac{W}{L} \) and \( \mu, C_{OX} \) and \( W/L \) represent standard transistor parameters.

![Fig. 2.18 MOS based resistor realization [36].](image)

Since the transistors \( M_a \) and \( M_b \) are perfectly matched and have equal drain to source voltages, the difference of the currents flowing in the two transistors can be expressed as

\[ (I_a - I_b) = K_n(V_a - V_b)(V_1 - V_2) \]

\[ = G(V_1 - V_2) \]  \hspace{1cm} (2.40)

![Fig. 2.19 MOS implementation of a linear resistance connected between negative and output terminals of OTRA.](image)
From (2.40) it can be observed that and a resistor $R = \frac{1}{G}$ can be implemented, cancelling both even and odd non-linearities. The value of the resistance may be computed to be

$$R = \frac{1}{K_n(V_a - V_b)}$$  \hspace{1cm} (2.41)

$K_n$ is determined through model parameters and W/L ratio of the transistors used to implement the resistor. Once $K_N$ value is fixed the resistance value can be adjusted by appropriate choice of gate voltages thereby making it electronically tunable.

**2.9 CONCLUDING REMARKS**

In this chapter an ideal OTRA along with its terminal characteristics is presented. Nullor based model of OTRA has also been described. Nonidealities of practically realized OTRA are taken into consideration which would be helpful in performance evaluation of any OTRA based circuit. A brief on existing literature on OTRA realization is presented. The OTRA CMOS realization proposed in [38] is explained and characterized using SPICE. Few basic applications of the OTRA are also described which can be readily used in designing the complex applications. Finally MOS based resistor realization using the current differencing property of OTRA has been discussed which helps in making circuits fully integrable and electronically tunable.