CHAPTER 7

DEVELOPMENT OF CONTROL ALGORITHM FOR BUCK AND BOOST DC-DC CONVERTERS USING FPGA

7.1 INTRODUCTION

The FPGA based digital control allows the implementation of more functional control schemes, standard control hardware design for multiple platforms and flexibility of quick design modifications to meet specific customer needs. It also provides rapid prototyping by synthesizing the desired system with an appropriate electronic design automation (EDA) tool. In contrast to general purpose processors, the FPGA actually constitutes the logic circuits required to implement the desired algorithm instead of a sequence of instructions on predefined hardware resources. Thus, it can achieve higher performance than general purpose processors. The FPGA based system is also useful because it can reduce development time greatly. Due to these beneficial features of the reconfigurable FPGA system, it is used as the implementation platform for the proposed PI algorithm. When the FPGA based system is used for implementing the desired PI, many possible designs can be tried due to the reusability of the FPGA. Often, a hardware implementation on the FPGA based system is supported by many existing EDA tools for modeling, synthesis, verification and implementation. The FPGA technology is now considered by an increasing number of designers in various fields of application such as telecommunication (Lee et al 1999), video (Pirsch et el 1995), signal processing (Chou et al 1993), embedded control systems (Kappos and Kinniment 1996) and electrical control systems.
(Pinmentel and Le-Huy 2000). This chapter deals with the implementation of a controller for DC-DC buck and boost converters, using the FPGA.

7.2 HARDWARE DESCRIPTION LANGUAGES

The existence of an IEEE standard has spread the use of Very High Speed Integrated Circuit Hardware Description language (VHDL) and has allowed the creation and development of high performance CAD tools in the field of microelectronics (Ashenden 1996). The designer can take advantage of this language to build his own circuit by using a hierarchical and modular approach that is defined at different levels of abstraction (Navabi 1998). A design approach by abstraction levels can be applied to ASCIs as well as to FPGAs and is referred to in the literature as “top-down methodology” (Riesgo et al 1999).

More recently, FPGA manufacturers have designed software packages that enable both the simulation and automatic translation of a design into hardware (Xilinx 2006). This software runs inside the Matlab-Simulink environment. Such an approach offers an FPGA-based rapid prototyping platform (Ricci and Le-Huy 2002). It should be mentioned that the concept of automatic code generation has already been applied with success to DSP processors (dSPACE 2002). No doubt, this kind of solution will be more and more utilized in the immediate future. However, up to now, this approach is still limited to applications that do not require the use of complex sequencers.

7.3 SPECIFICATIONS OF SPARTAN – 3 FPGA

The FPGA used for the implementation of the controller for buck and boost converter is a dual spartan 3 FPGA, and it has the following features
- One separate powerful FPGA provided to generate PWM signals using the software IP
- Another FPGA to process the fast ADC inputs and DAC outputs
- Two numbers of spartan each provided with 400K gates
- Each FPGA has configuration flash PROM and JTAG interfacing facility
- 16 x 2 or 20 x 4 LCD display and 8 numbers of push button keys for various functions
- 8 channel 12 bit serial DAC and output terminated at 10 pin connector
- 2 channel DAC outputs also terminated at 4 pin screw type connector
- 2 FPGAs can be interconnected through I/O LINES
- First FPGA contains 16 PWM outputs (isolated), 24 isolated digital I/Os, 8 capture isolated inputs and 16 output LEDs
- Second FPGA with ADC & DAC contains 16 channel 12 bit serial ADCs, 4 Numbers of AD7266, each has dual 12 bit ADC, 2 MSPS throughput for each ADC
- Drives power modules connectivity with one 34 pin header to terminate PWM output and capture inputs, and another 26 pin header for the ADC input signals.

### 7.4 BLOCK DIAGRAM

The buck and boost converter is implemented as a discrete-time digital system controller using a SPARTAN–3 FPGA, which is shown in
Figure 7.1. The FPGA contains ADC, comparator, PI Controller and PWM. In addition, an interface board is built to sample and convert the analog switching converter output voltage into digital data and then convert the inferred results into control signals, which is the duty cycle. The instantaneous output voltage $V_{out}$ is sensed and conditioned by the voltage sensing circuit and provides input to the FPGA via the ADC channel. The digitalised sensed output voltage $V_o$ is compared to the reference $V_{ref}$ and depending on the error signal the PI controller generates the control signal which is given to the PWM, and it generates the control pulse. The control pulse generated by the PWM is given to the buck/boost regulator and it is switched on according to the duty cycle, so that the output voltage is maintained constant irrespective of load and input variations.

![Block Diagram of the FPGA Based Controller for the Buck and Boost Converter](image)

**Figure 7.1 Block Diagram of the FPGA Based Controller for the Buck and Boost Converter**

### 7.5 CIRCUIT DIAGRAM

The FPGA is implemented as a controller for the buck and boost converters for which the circuit diagrams are explained in following sections:
7.5.1 Buck Converter

The circuit shown in Figure 7.2 is used to drive the actual buck converter circuit. The optoisolator used next to the FPGA is used to isolate the driver circuit from the FPGA. The output control pulses from the FPGA are given to the optoisolator (6N 137) and it gives the same signal in the output, but it is in the inverted form. The inverted signal from the optoisolator is given to the inverter (4584) to get the actual signal which is given to the driver (IR 2110). The driver gives the 15V signal to the MOSFET of the buck converter, and it is turned on and off with respect to the control signal given by the FPGA to maintain the output voltage constant, irrespective of the input voltage and load variations.

7.5.2 Boost Converter

The circuit shown in Figure 7.3 is used to drive the actual boost circuit. The optoisolator used after the FPGA is used to isolate the driver circuit from the FPGA. The output control pulses from the FPGA are given to the optoisolator (6N137) and it gives the same signal in the output, but it is in the inverted form. The inverted signal from the optoisolator is given to the inverter (4584) to get the actual control signal which is given to the driver (IR 2110). The driver gives a 15 volts output to turn ON and OFF the MOSFET of the buck converter with respect to the control signal from the FPGA to maintain the output voltage constant, irrespective of the input voltage and load variations.
Figure 7.2 Complete Circuit Diagram of the FPGA-based Controller for the Buck Converter
Figure 7.3 Complete Circuit Diagram of the FPGA-based Controller for the Boost Converter
7.5.3 Power Supply

The power supply to the buck/boost circuit is shown in Figure 7.4. The transformer used is a step-down transformer with an output voltage of 15 V. The voltage is given to the diode rectifier and it is rectified to DC voltage which is filtered using the filter. The filtered output voltage is given to the series regulator which regulates the output voltage. It gives a constant output voltage of 15volts.

![Figure 7.4 Circuit Diagram of Power Supply](image)

7.6 RESULTS AND DISCUSSION

Experimental investigations hasve been performed for the various input voltage and load conditions on the buck and boost converter with a controller implemented using the FPGA; these are given below.

7.6.1 Boost Converter Subjected to an Input Voltage Variations

The PI control algorithm is implemented by VHDL coding in a SPARTAN – 3 FPGA, to drive the actual circuit of the boost converter with $K_p = 0.12$ and $K_i = 0.03$. The parameters of the circuit are $L = 0.16\text{mH}$, $C = 47\mu\text{F}$, the load resistor $R = 8\Omega$. The input voltage is varied from 1 to 4 volts both in an increasing and decreasing manner. The set value of the output voltage is 6V and the effectiveness of the controller with respect to overshoot and settling time is studied.
Figure 7.5  Boost Converter Subjected to a Variation of Input Voltage from 2 Volts to 4.2 Volts

Figure 7.5 shows the variation of output voltage vs time. It is found that the controller acts very effectively and it maintains the constant output voltage of 6 volts, irrespective of a variation of input voltage from 2 volts to 4.2 volts. The peak overshoot voltage at the time of input voltage variation is 10% and the settling time is 75ms.

Figure 7.6  Boost Converter Subjected to a Variation of Input Voltage from 3.8 Volts to 3.4 Volts
Figure 7.6 shows the variation of output voltage vs time. It is found that the controller acts very effectively and it maintains the constant output voltage of 6 volts, irrespective of a variation in the input voltage from 3.8 volts to 3.4 volts. The peak overshoot voltage at the time of input voltage variation is 5% and the settling time is 65 ms.

![Graph](image)

**Figure 7.7 Boost Converter Subjected to a Variation of Input Voltage from 2.2 Volts to 2.8 Volts**

Figure 7.7 shows the variation of output voltage vs time. It is found that the controller acts very effectively and it maintains the constant output voltage of 6 volts irrespective of a variation in the input voltage from 2.2 volts to 2.8 volts. The peak overshoot voltage at the time of input voltage variation is 10% and the settling time is 60 ms.

### 7.6.2 Boost Converter with Load Variations

The boost converter is subjected to a variation of load from 2 Ω to 6 Ω both in an increasing and decreasing manner. The effectiveness of the controller with respect to overshoot and settling time at the time of load variations are studied.
Figure 7.8 Boost Converter Subjected to a Variation of Load from 3 $\Omega$ to 6 $\Omega$

Figure 7.8 shows the variation of output voltage vs time. It is found that the controller acts very effectively and it maintains the constant output voltage of 6 volts, irrespective of variation of the load from 3 $\Omega$ to 6 $\Omega$. The peak overshoot at the time of load variation is 20% and the settling time is 150ms.

Figure 7.9 Boost Converter Subjected to a Variation of Load from 6 $\Omega$ to 3$\Omega$
Figure 7.9 shows the variation of output voltage vs time. It is found that the controller acts very effectively and it maintains the constant output voltage of 6 volts irrespective of variation in the load from 6 $\Omega$ to 3 $\Omega$. The peak overshoot at the time of load variation is 20% and the settling time is 125ms.

### 7.6.3 Buck Converter with an Input Voltage Variations

The PI control algorithm was implemented in a SPARTAN-3 FPGA to drive the actual circuit of the buck converter with $K_p = 0.12$ and $K_i = 0.03$. The parameters of the circuit are $L = 1$ mH, $C = 1000$ $\mu$F, and the load resistor $R = 100$ $\Omega$. The input voltage is varied from 10 to 30 volts both in an increasing and decreasing manner. The set value of the output voltage is 10 V.

![Graph showing output voltage vs time for buck converter with input voltage variation](image)

**Figure 7.10 Buck Converter Subjected to a Variation of the Input Voltage from 25volts to 15 Volts**

Figure 7.10 shows the variation of output voltage vs time. It is found that the controller acts very effectively and it maintains the constant output voltage of 10 volts, irrespective of a variation of the input voltage from 25 volts to 15volts. The peak overshoot voltage at the time of input voltage variation is 5% and the settling time is 100ms.
Figure 7.11 Buck Converter Subjected to a Variation of Input Voltage from 18 Volts to 30 Volts

Figure 7.11 shows the variation of output voltage vs time. It is found that the controller acts very effectively and it maintains the constant output voltage of 10 volts, irrespective of a variation of the input voltage from 18volts to 30volts. The peak overshoot voltage at the time of input voltage variation will be 10% and the settling time will be 125 ms.

Figure 7.12 Buck Converter Subjected to a Variation of Input Voltage from 15 Volts to 25 Volts
Figure 7.12 shows the variation of output voltage vs time. It is found that the controller acts very effectively and it maintains the constant output voltage of 10volts, irrespective of variation of the input voltage from 15 volts to 25volts. The peak overshoot voltage at the time of input voltage variation will be 10% and the settling time will be 75ms.

7.6.4 Buck Converter with Load Variations

The buck converter is subjected to a variation of load from 100 Ω to 10 Ω both in an increasing and decreasing manner. The effectiveness of the controller with respect to overshoot and settling time at the time of load variations are studied.

Figure 7.13 Buck Converter Subjected to a Variation of Load from 20 Ω to 100 Ω

Figure 7.13 shows the variation of output voltage vs time. It is found that the controller acts very effectively and it maintains the constant output voltage of 6 volts, irrespective of a variation of load from 20 Ω to 100 Ω. The peak overshoot at the time of load variation is 20% and the settling time is 75ms.
Figure 7.14 Buck Converter Subjected to a Variation of Load from 100 Ω to 20 Ω

Figure 7.14 shows the variation of output voltage vs time. It is found that the controller acts very effectively and it maintains the constant output voltage of 6 volts, irrespective of a variation of load from 100 Ω to 20 Ω. The peak overshoot at the time of load variation will be 20% and the settling time will be 85 ms.

Figure 7.15 Buck Converter Subjected to a Variation of Load from 100 Ω to 60 Ω
Figure 7.15 shows the variation of output voltage plotted with respect to time. It is found that the controller acts very effectively and it maintains the constant output voltage of 6 volts irrespective of a variation of load from 100 Ω to 60 Ω. The peak overshoot at the time of load variation will be 20% and the settling time will be 150ms.

7.7 HARDWARE IMPLEMENTATION

The photographs shown in Figures 7.16 and 7.17 show the hardware implementation of the FPGA based controller for a buck and boost converter.

Figure 7.16 Photograph of the FPGA Based Controller for a Buck Converter
7.8 RESULTS COMPARISON FOR CONTROLLERS WITH THE DSP AND FPGA

The controllers for buck and boost converters are successfully implemented using the DSP and FPGA. The controllers are tested for both input voltage and load variations. From the experimental result and analysis as shown in Tables 7.1 and 7.2, it is observed that with a controller using the FPGA, the spike occurs at the time of input voltage and load changes will be very minimum as compared to the controller implemented using the DSP. The settling time of output voltage due to input voltage and load changes, will also be less for a controller implemented using the FPGA when compared to the DSP.
Table 7.1  Performance Comparison of a Boost Converter with the DSP and FPGA

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Load</th>
<th>Overshoot of output voltage in %</th>
<th>Settling time in ms</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>DSP</td>
<td>FPGA</td>
</tr>
<tr>
<td>1.</td>
<td>3 Ω– 6Ω</td>
<td>40 %</td>
<td>20 %</td>
</tr>
<tr>
<td>2.</td>
<td>6 Ω– 3 Ω</td>
<td>30 %</td>
<td>20 %</td>
</tr>
</tbody>
</table>

Table 7.2  Performance Comparison of a Buck Converter with the DSP and FPGA

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Load</th>
<th>Overshoot of output voltage in %</th>
<th>Settling time in ms</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>DSP</td>
<td>FPGA</td>
</tr>
<tr>
<td>1.</td>
<td>20Ω– 100Ω</td>
<td>25 %</td>
<td>20 %</td>
</tr>
<tr>
<td>2.</td>
<td>100Ω– 20Ω</td>
<td>30 %</td>
<td>20 %</td>
</tr>
</tbody>
</table>

7.9  CONCLUSION

In this research study the buck and boost converter, implemented using the FPGA provides fast transient recovery for load and input voltage disturbances. It is shown that the proposed controller is robust because the output voltage will not be affected by input voltage and load changes. It is also clear that this technique can accurately drive the output voltage to the desired level, with very minimum spike and settling time, at the time of parameter changes, when compared to the DSP.