CHAPTER 2

MODELLING, SIMULATION AND ANALYSIS
OF SRM WITH PFC

2.1 INTRODUCTION

This chapter presents the modelling of Switched Reluctance Motor drive with and without a power factor controller by using MATLAB / SIMULINK. Many of the variable speed drives have no input power factor correction circuits. This results in harmonic pollution of the utility supply, which should be avoided. SRM runs in different modes of operation like single pulse, soft chopping and hard chopping. A power factor controller consists of boost and buck converter with the above said modes of operation for SRM drive with improved power factor. The proposed topologies are simulated using MATLAB/ SIMULINK software package and the results are obtained.

Switched Reluctance Motor (SRM) drives have been used for a variety of applications, such as aerospace systems, marine propulsion systems, linear drives, mining drives, hand held tools and home utility applications. SRM has simple and robust structure, high efficiency and high ratio of torque to rotor volume (Krishnan 2001). It is suitable for variable speed as well as servo type applications.

SRM requires a power controller for its operation. It draws a pulsating ac line current, resulting in low input power factor and high harmonic line current. The distortion of the current leads to the reduction of
the quality of power supply. Therefore, it is necessary to improve the input current waveform to near sinusoidal. This is accomplished by a power factor correction circuit, which improves the input current waveform.

SRM drives are normally supplied from a stable DC link voltage. A simple rectifier and a large DC-link capacitance provide the DC-link voltage. During the operation of the drive the associated harmonics with the input current often exceeds the limits given in the existing norms. Some of the standards available for the harmonic distortions are

- ANSI / IEEE Standard C 57.12.00 and C 57.12.01 specify the current distortion in transformers within 5%.
- ANSI Standard C 82.1 specifies that the high frequency ballast should have maximum total current harmonic distortion within 32%.
- IEEE/ANSI 519, “IEEE recommended practices and requirements for Harmonic control in Electrical Power Systems”, specifies the standard limits for voltage and current distortion as tabulated in Tables 2.1 and 2.2.

### Table 2.1 Voltage Distortion Limits

<table>
<thead>
<tr>
<th>Operating voltage</th>
<th>Individual Harmonics</th>
<th>Total Harmonic distortion</th>
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</thead>
<tbody>
<tr>
<td>&lt; 69 kV</td>
<td>3 %</td>
<td>5 %</td>
</tr>
<tr>
<td>&lt; 161 kV</td>
<td>1.5%</td>
<td>2.5%</td>
</tr>
<tr>
<td>&gt; 161 kV</td>
<td>1 %</td>
<td>1.5%</td>
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</table>
Table 2.2 Current Distortion Limits ( < 69 kV )

<table>
<thead>
<tr>
<th>(I_{sc} / I_L)</th>
<th>kV</th>
<th>&lt; 11</th>
<th>&lt; 17</th>
<th>&lt; 23</th>
<th>&lt; 25</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 20</td>
<td>4</td>
<td>2</td>
<td>1.5</td>
<td>0.6</td>
<td></td>
</tr>
<tr>
<td>&lt; 50</td>
<td>7</td>
<td>3.5</td>
<td>2.5</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>&lt; 100</td>
<td>10</td>
<td>4.5</td>
<td>4</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>&lt; 1000</td>
<td>12</td>
<td>5.5</td>
<td>5</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>&gt; 1000</td>
<td>15</td>
<td>7</td>
<td>6</td>
<td>2.5</td>
<td></td>
</tr>
</tbody>
</table>

* where \( I_{sc} / I_L \) is the ratio between the short circuit current to the load current.

- International Electro technical standards (IEC) – EN 61000-3-2 specifies the limit for the odd and even harmonics presenting the class A category which includes the motor driven equipment with phase angle control, domestic appliances and all three phase equipment (\( \leq 16 \) Amps). The limits are specified for 230 V single phase and 230 / 400 V three phase equipment.

Table 2.3 IEC –EN -61000-3-2 Standards for Class A category

<table>
<thead>
<tr>
<th>Harmonic order (n)</th>
<th>Maximum permissible harmonic current (Amps)</th>
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<tbody>
<tr>
<td></td>
<td>ODD HARMONICS</td>
</tr>
<tr>
<td></td>
<td>3</td>
</tr>
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<td>13</td>
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<td></td>
<td>15( \leq n \leq 39 )</td>
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<td></td>
<td>EVEN HARMONICS</td>
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<tr>
<td></td>
<td>2</td>
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<tr>
<td></td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>8( \leq n \leq 40 )</td>
</tr>
</tbody>
</table>
In SRM drive, the input current waveform is distorted due to the switching of currents in the phase winding. Energy saving in SRM can be achieved by maintaining sinusoidal input current with improved power factor. Researchers have introduced the following power factor correction methods, which have been employed in practice:

- Buck- Boost converter (Geun-Hie Rim 1994, Barnes 1998)

The selection of these methods depends on the application of the drive, specifically, on the power, speed, cost and performance requirement. The first method has many advantages including higher efficiency at all operating points, high reliability, high starting torques and four-quadrant operation. It is used only for low power applications. The second method is employed for medium-power applications, in which the pulsating phase currents are not filtered by the smaller DC link capacitor. These pulsating currents produce additional voltage ripple in the system. In diode bridge rectifier with step up converter method, the switched input current waveform is modified to a sinusoidal one. The additional inductor used in the controller increases the cost, weight and volume of the drive. In the buck boost converter method, the boost converter is used to improve the sinusoidal input current and the buck converter is used to regulate the DC source voltage.
This chapter is mainly focused on a boost and buck converter topology for PFC, which is simulated for single pulse, soft and hard chopping modes of operation with the help of MATLAB / SIMULINK environment. The boost converter is used to increase the input voltage and to improve the input current waveform. The buck converter stage consists of inverter, isolation transformer and rectifier used to provide the low operating voltages to SRM.

2.2 SWITCHED RELUCTANCE MOTOR OPERATION

SRM has simple structure with salient poles on both stator and rotor as shown in Figure 2.1. It has no windings or magnets on the rotor. The concentrated windings on the stator are wound around each pole, and diametrically opposite pole stator windings are connected in series. The operation of the SR motor is based on the principle that the rotor always tends to align its poles with the position that provides minimum reluctance in the magnetic circuit. To make the rotor to rotate in a particular direction, the stator phase windings are energized with a pre-determined sequence. The switching sequence must be synchronized to the rotor position by means of a rotor position sensor. The inductance of the stator winding depends on the reluctance of the magnetic circuit, which varies as a function of the rotor position. The variation of the phase inductance is shown in Figure 2.2.

Figure 2.1 Cross section of 6/4 SRM
If saturation is neglected, it can be shown that the motor torque is given by equation (2.1) (Krishnan 2001),

\[ T = \frac{1}{2} i^2 \frac{dL}{d\theta} \]  

(2.1)

where \( i \) is the instantaneous stator current and \( dL/d\theta \) is the variation of phase inductance with rotor position. The developed torque is proportional to the square of the current and it is independent of the current direction. The motoring torque is developed by exciting the phases during the rising inductance period. The generating torque is developed by exciting the phases when their inductances are decreasing. As a result, motoring or braking operation can be obtained by simply changing the switching instants of the current into the stator windings. The direction of rotation can be changed by inverting the switching sequence of the converter switches.

2.3 SRM CONVERTER OPERATION

In SRM drive, the different motor converters like Classic bridge, R-dump, C-dump, C-dump with freewheeling, Shared switch, Minimum switch with variable DC link, Bifilar, Split DC type and mid-point converters are used to drive the motor (Ray 1981, Slobodan Vukosavid 1991, Krishnan 2001). The classical bridge converter has the advantages of high efficiency,
complete phase independence, better performance in all operating conditions (Krishnan 2001).

Figure 2.3 Classic bridge converter

Figure 2.3 shows the classic bridge converter circuit for the 6/4 pole SRM drive, where S1-S6 represents the switches, D1-D6 represents the diodes and A, B, C represents the phase windings. In classic bridge SRM converter, two switches and two diodes are used for each phase windings of the SRM. One phase of the SRM is represented in Figure 2.4 in which S1 and S2 are the power switches, D1 and D2 are the diodes and A represents a phase winding of SRM.

Figure 2.4 SRM per phase converter
The switching action of this circuit is as follows:

(i) When both the switches S1 and S2 are ON, then the winding is in energizing mode.

(ii) When any one of the switches is ON and another switch is OFF, then the winding is in current regulation mode.

(iii) When both the switches S1 and S2 are OFF, then the winding is in de-energizing mode.

2.3.1 Energizing Mode

During energizing mode, switches S1 and S2 are in ON state as shown in Figure 2.5. The input DC source magnetizes the phase. This mode is usually initiated before the start of the rotor and stator pole overlap. The phase current reaches the reference value before the phase inductance begins to increase. This helps to overcome the back EMF at higher speeds. When the current reaches the reference value, the converter steps into the current regulation mode. The voltage across the phase is given in equation (2.2).

\[
V_{dc} = V_{ph}(t) = i_{ph}(t)r_{ph} \cdotp \frac{\dot{i}_{ph}}{i_{ph}} \cdotp \frac{di_{ph}}{dt} + \frac{\ddot{\psi}_{ph}(i_{ph}, \dot{\theta}_{ph})}{\ddot{\theta}_{ph}} \cdotp \frac{d\theta}{dt} \quad (2.2)
\]

![Figure 2.5 Energizing mode](image)
2.3.2 Current Regulation Mode

The current regulation can be achieved by switching S1 ON and OFF continuously, while leaving the other switch S2 continuously ON as shown in Figure 2.6.

In this current regulation mode, the voltage across the phase is given in the equation (2.3),

\[
V_{dc} = 0 = V_{ph}(t) = i_{ph}(t)r_{ph} + \frac{\hat{c}}{\hat{i}_{ph}} \psi_{ph} \left( i_{ph}, \theta_{ph} \right) \frac{di_{ph}}{dt} + \frac{\hat{c}}{\hat{\theta}} \psi_{ph} \left( i_{ph}, \theta_{ph} \right) \frac{d\theta}{dt}
\]

2.3.3 Demagnetization Mode

The switching devices S1 and S2 are turned OFF in the demagnetization mode. The current flows through the freewheeling diodes D1 and D2. The electrical equivalent circuit for this mode is shown in Figure 2.7. The current in the phase winding decreases rapidly as energy is returned from the motor to the supply. This is called demagnetization mode. In demagnetization mode, the motor phase winding voltage is \(-V_{dc}\). While a
phase is demagnetizing, another phase can be magnetized. The voltage across the phase winding is given in the equation (2.4).

\[-V_{dc} = V_{ph}(t) = i_{ph}(t)r_{ph} + \frac{\hat{\psi}}{\hat{i}_{ph}} \frac{di_{ph}}{dt} + \frac{\hat{\psi}}{\hat{\theta}} \frac{d\hat{\theta}}{dt}\] (2.4)

![Diagram of Demagnetization mode](image)

Figure 2.7 Demagnetization mode

2.4 OPERATING MODES OF CLASSICAL SRM DRIVE

2.4.1 Single Pulse Mode of Operation

The switches, S1 and S2 are continuously turned ON during the conduction period of the particular phase. This mode is applicable for only high-speed operation of SRM. Since the motor operates at high speed, the back emf of the motor is high. This does not allow the current to rise to higher values. A controller is used to regulate the turn-on and turn-off angle for desired speed and torque. The inductance, voltage, flux linkage and current during the operation are shown in Figure 2.8 (Miller 1989).
2.4.2 Soft Chopping Mode of Operation

The PWM signal to the switch S1 is turned ON and OFF continuously and the switch S2 is continuously turned ON during the conduction period. This mode is applicable only for low speed operation. Normal mode of operation is used in soft chopping method. In this method the torque and current ripples are less. The inductance, voltage, flux linkage and current during the operation are shown in Figure 2.9 (Miller 1989).
2.4.3 Hard Chopping Mode of Operation

The switches S1 and S2 are turned ON and OFF simultaneously at high frequency. The Torque and Current ripples are more as compared to other modes due to high frequency switching. This method is preferred for Low speed operation. When both S1 and S2 are open, the voltage across the phase winding is \(-V_{dc}\) which causes the current to rise very rapidly. The inductance, voltage, flux linkage and current during the operation is shown in Figure 2.10 (Miller 1989).
Figure 2.10  Inductance, Voltage, Flux linkage and Current waveforms during hard chopping mode
2.5 GENERATION OF GATE PULSES FOR SRM OPERATION AND CONTROL

The generation of gate pulses to the classical bridge converter is described in the following sections.

2.5.1 Rotor Position Sensor

The slotted disk is one of the methods to find the rotor position information. A slotted disc is attached with the shaft of the motor as shown in Figure 2.11. This slotted disk with optical interrupters is used for sensing the rotor position. The sensing of the signal is more important at all speeds, since, where the current waveform is mainly dependent on the firing angle. In this arrangement, three sensors displaced by an angle of 30 degrees are fixed on the frame. In Figure 2.11, A, B, C indicates the position of the sensors and 1,2,3 indicates the phases of the SRM. This Figure shows the alignment of rotor with phase 1 (Miller 1989, Becerra 1993).

![Figure 2.11 Position of Sensors](image)
2.5.2 Rotor Position Sensor Circuit

Figure 2.12 shows the rotor position sensor circuit to get the information about the rotor position. In this research, Photo diode (MLED 930) and Photo transistor (MRD 5009) are used. When the transistor detects the light emitted by the photo diode, the circuit output is zero and when the transistor does not detect the light emitted from the photo diode, the circuit output is one. The resistances in the sensor circuit are used to reduce the current flow in the photo diode and photo transistor.

![Figure 2.12 Photo diode and photo transistor arrangement](image)

2.5.3 Operating Modes of SRM Drive

SRM is operated in different operating modes like normal, braking, advanced long dwell angle and braking modes. The operation is based on the signals from the rotor position sensor as shown in Figure 2.13. The sensor signal has ON period of 45 degrees and OFF period of 45 degrees. The ON period for the normal, boost and braking modes are 30 degrees and OFF periods are 60 degrees. The advanced long dwell period has ON period of 45 degrees and OFF period of 45 degrees (Miller 1989).
The combinational logic circuit is developed for all the modes and is shown in Figure 2.14. The sensor signals are passed through proper combinational logic circuits to implement the different modes of operation.

Figure 2.13 Commutation waveforms for different operating modes
Figure 2.14 Combinational logic circuit (a) Normal mode (b) Boost mode (c) Advanced dwell angle mode (d) Braking mode
2.5.4 Gate driver and Opto Isolator

The signals from the combinational logic circuit are amplified to the level required for switching the power MOSFET’s using a totem pole gate drive circuit. To turn ON the MOSFET, the input to the driver is OFF, thus turning ON the NPN transistor, which provides a positive gate voltage to the
MOSFET. To turn OFF the device, the input to the driver is ON, thus turning OFF the NPN transistor, which provides a zero gate voltage to the MOSFET. The output of the gate driver is connected across the gate and source of the power MOSFET.

The upper MOSFET is floating and it can be either at 0 V or 160 V. This floating ground would generate a lot of common mode noise. This would interfere with the normal operation of the circuit and it might malfunction. To avoid this situation, the ground of each gate driver output is isolated from the grounds of the other gate drivers and also from the input stage ground.

A high-speed opto coupler (HCPL 4503) is used to transfer the control signal from the input stage to the gate driver stage. An isolated DC/DC converter ensures that the grounds of each gate driver circuits are isolated from the other. The complete gate driver and opto isolator circuit for one switch of the converter is shown in Figure 2.15.

![Figure 2.15 Driver and isolation circuit](image)

### 2.6 RELATIONSHIP BETWEEN POWER FACTOR AND HARMONICS

The current and voltage are sinusoidal and in phase when the power factor is 1.0. If both are sinusoidal but not in phase, the power factor is the cosine of the phase angle difference between them. This occurs when the load
is composed of resistive, capacitive and inductive elements and all are linear. In many power electronic circuits, the current and voltage may be perfectly in phase, in spite of the severe distortion of the current waveform. The “cosine of the phase angle” definition would lead to the erroneous conclusion that the power supply has a power factor of 1.0. Therefore, the power factor of the power electronic circuit is normally defined by its displacement factor and distortion factor (Rashid 2004).

Power factor = Real power /Apparent power

\[
\frac{V_{\text{rms}} I_{\text{rms}} \cos \phi}{V_{\text{rms}} I_{\text{rms}}}
\]

\[
= \frac{I_{\text{rms}} \cos \phi}{I_{\text{rms}}}
\]

\[
= K_d K_d
\]  

(2.5)

Power factor = Distortion factor x Displacement factor

The relationship between the total harmonic distortion to the power factor is given by equation (2.6),

\[
THD(\%) = 100 \times \sqrt{\frac{1}{K_d^2} - 1}
\]  

(2.6)

where \(K_d\) is the distortion factor and is equal to:

\[
K_d = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}}
\]

(2.7)

when the fundamental component of the input current is in phase with the input voltage, \((K_d = 1)\).
\[ PF = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}} \]  

(2.8)

A perfectly sinusoidal current could have a poor power factor, simply by having its phase not in line with the voltage.

### 2.7 SCHEMATIC DIAGRAM OF SRM

Figure 2.16 illustrates the conventional SRM drive which consists of rectifier, filter and machine converter circuits. The rectifier circuit converts the input AC voltage into DC voltage. The filter circuit reduces the voltage ripple. The asymmetric bridge converter, which switches voltage into the winding of the SRM, draws a pulsating current with high harmonic content resulting in poor power factor.

Figure 2.17 shows the proposed PFC with SRM drive. In this method, a boost and buck converter is introduced to minimize the distortion of line current switched into the windings of SRM. This is done by sensing the output current and voltage of rectifier. The boost converter is used to improve the input current waveform and buck converter is used to regulate the DC voltage. Figure 2.18 shows the basic boost PFC circuit.

![Schematic diagram of SRM without power factor controller](image)

**Figure 2.16 Schematic diagram of SRM without power factor controller**
A voltage error amplifier compares the output voltage of the PFC and the reference voltage ($V_{ref}$) and produces an error signal into the reference multiplier. The other input to the multiplier is the input rectified ac input voltage. The multiplier output is the product of the DC signal from the voltage error amplifier and rectified input AC voltage. The output of the multiplier is a full wave rectified sine wave.
The inputs to the current error amplifier are the output of the multiplier circuit and the output current signals of rectifier circuit. The output of the current error amplifier and the PWM signals are compared. The carrier frequency of PWM modulator is 50 kHz. The gate signals for the boost converter switch are generated from the output of the PWM modulator.

2.8 SIMULATION PROCEDURE AND RESULTS

The SRM drive is simulated by using MATLAB / SIMULINK software platform with and without the power factor controller. Figure 2.19 shows the modeling of SRM without the power factor controller. The 6/4 pole SRM is fed by a three-phase asymmetrical power converter having three legs, each of which consists of two power devices and two free-wheeling diodes. During conduction periods, the active power device applies positive source voltage to the stator windings to drive positive currents into the phase windings. During free-wheeling periods, negative voltage is applied to the windings and the stored energy is returned to the DC source through the diodes. The phase currents are independently controlled by three hysteresis controllers which generate the drive signals by comparing the measured currents with the references.

Figure 2.20 shows the SRM with power factor controller. The power factor controller consists of a boost and buck converter circuit. In the first stage, the input AC voltage is converted into DC voltage. The power factor converter circuit as shown in Figure 2.21 is used to increase the voltage to a maximum of 400Volts. The boost converter output voltage is reduced to lower machine operating voltage. The firing pulses to the boost converter are given by sensing the input current to the boost stage and the output voltage of boost converter. A PI controller is used to shape the input current.

Figure 2.22 shows the input and output terminals of the simple converter model. The inputs to the converter block are gate signal to the power device and DC input voltage to the Asymmetric bridge converter. The
output voltages are given to the machine windings (A1-A2, B1-B2, C1-C2). Three asymmetric bridge converters are used for all the three phases of 6/4 pole SRM. Figure 2.23 shows the connections of one phase of the simple asymmetric bridge circuit configuration.

Figure 2.19   Modeling of SRM without PFC
Figure 2.20  Modeling of SRM with PFC
Figure 2.21 Power factor controller
Figure 2.22 Simple Converter model

Figure 2.23 Simple Asymmetric bridge converter
Figure 2.24 Converter model for single pulse mode
Figure 2.25 Converter model for soft chopping mode
Figure 2.26 Converter model for hard chopping mode
Figure 2.27 Input voltage, current waveforms and current harmonic spectrum (without power factor correction circuit)
Figure 2.28 Input voltage, current waveforms and current harmonic spectrum with power factor correction circuit at Single pulse operation.
Figure 2.29 Input voltage, current waveforms and current harmonic spectrum with power factor correction circuit at soft chopping
Figure 2.30  Input voltage, current waveforms and Input current harmonic spectrum with power factor correction circuit at hard chopping
The converter models for pulse generation for the single pulse, soft chopping and hard chopping modes are shown in the Figures 2.24 -2.26. In soft chopping mode, the PWM control signals are given to the upper power devices and in hard chopping mode the PWM control signals are given to both upper and lower power devices.

Figure 2.27 shows the input voltage and current waveforms without power factor correction circuit. This Figure shows four cycles of voltage and current. Current waveform is seen to be distorted very much. By introducing PFC, the current was found to be smooth in single pulse mode of operation as shown in Figure 2.28. Figure 2.28 also shows the harmonic spectrum for the input current with power factor controller in single pulse mode operation.

In soft chopping, one of the switches remains ON and therefore the ripple content is less. In hard chopping, both the switches are ON and OFF simultaneously; therefore the current ripple is high compared to soft chopping and single pulse operation. Though, the current is distorted, it is nearly sinusoidal and the power factor is nearer to unity. The current distortions will be more when SRM is switched by soft chopping and hard chopping modes of operation, when compared to single pulse operation.

The voltage and current output for the soft and hard chopping mode and its relevant current harmonic spectrum are shown in Figures 2.29 and 2.30. The comparison of the harmonic current magnitudes is tabulated in Table 2.3.
Table 2.4 Comparison of Power factor and % Current Harmonics

<table>
<thead>
<tr>
<th>PF, % THD and Harmonic Number</th>
<th>% Current Harmonics</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Without power factor controller</td>
<td>With power factor controller</td>
<td>Single pulse operation</td>
<td>Soft chopping mode</td>
</tr>
<tr>
<td>PF</td>
<td>0.96</td>
<td>0.9984</td>
<td>0.9975</td>
<td>0.9971</td>
</tr>
<tr>
<td>% THD</td>
<td>25.10</td>
<td>4.79</td>
<td>11.24</td>
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From the above analysis it is clearly observed that, the current waveform of the circuit is improved with power factor controller. Thus the power factor of the circuit is improved by employing the boost and buck converter circuit for the different operating modes.
2.9 SUMMARY

In this chapter, operation of SRM drive, SRM converter operation and generation of gate pulses are discussed. The SRM drive system with and without power factor correction circuit are simulated and results are discussed. In the SRM drive, without power factor controller, the current waveform has discontinuity and has more input current harmonics. Due to switching of voltage into the windings and the input current wave shape, the power factor of SRM is less. The proposed power factor correction circuit which consists of boost and buck converter stage is simulated with SRM in different operating modes such as single pulse, soft chopping and hard chopping. From the simulated results, the SRM operation with power factor controller improves the input current waveform. It is observed that the proposed scheme achieves near sinusoidal current and the harmonics in the system are reduced.