CHAPTER 2

Experimental Details

2.1 INTRODUCTION

In this chapter, the experimental techniques used for characterization of electrical properties of semiconductors are discussed. The chapter starts with a brief description to Schottky diode, which is used for conventional experimental characterization of the semiconductors in the present thesis. The current transport process and diode fabrication procedure used in this thesis are also discussed in brief. The facilities, which have been developed to study the effects of ion irradiation on Schottky barrier diodes at Inter-University Accelerator Centre, New Delhi are described. The techniques like current-voltage characterization, capacitance-voltage characterization and deep level transient spectroscopy developed in materials science beam line of the 15 UD Pelletron accelerator at IUAC are discussed.
2.2 SCHOTTKY BARRIER DIODE

A Schottky barrier is formed when a metal of work function \( e\Phi_m \) and an \( n \)-type semiconductor of work function \( e\Phi_s \) (for a \( p \)-type semiconductor \( e\Phi_s > e\Phi_m \)) and electron affinity \( e\chi_n \) are joined [1-3].

The different positions of the Fermi levels in the isolated materials cause a diffusion of electrons from the semiconductor to the metal, leaving behind uncompensated donor ions in the depletion space charge region. In thermodynamic equilibrium, the energy band diagram of the Schottky diode is constructed from the requirement of constant Fermi level and continuous vacuum level, as shown in Figure 2.1. In the ideal case, the Schottky barrier from the metal to the semiconductor is given by [1]

\[
\Phi_B = \Phi_m - \chi_n
\]  

(2.1)

while the built in potential from the semiconductor to metal is given by

\[
V_{bi} = \Phi_m - \Phi_s
\]  

(2.2)

An external applied bias will disturb the fine balance of electron transport across the junction and allow a net current to flow through the device. The various ways in which electron can be transported across the metal-semiconductor junction under forward bias are shown in Figure 2.2. The basic current transport processes are [1]:

1) transport of electron from the semiconductor over the top of the barrier into the metal (thermionic emission).
2) quantum-mechanical tunneling of electrons through barrier.
3) carrier recombination in the depletion region
4) hole injection from the metal to the semiconductor
Figure 2.1: The energy band diagram of the Schottky barrier diode

Figure 2.2: Basic current transport process in a forward biased Schottky barrier diode
Process (1) is usually the dominant current transport mechanism in Schottky contacts with moderately doped semiconductors and leads to the ideal current-voltage characteristics. Process (2) and (3) causes the departure from ideal behaviour. In forward bias process (4) is not important because minority carrier injection is negligible. Since in the present thesis work, moderately doped semiconductor is used throughout the studies, so process (1) is discussed in detail.

2.2.1 Thermionic emission process

An electron emitted over the barrier from the semiconductor into the metal moves first through the depletion region of the semiconductor. The motion of electron in this region is governed by the usual mechanism of drift and diffusion while the emission is governed by the density of available states in the metal. Thus the two processes, emission over the barrier and the drift and diffusion in depletion region are essentially in series and the current is determined predominantly by whichever offers the higher resistance. Schottky and Spenke [4] developed the first diffusion theory of current transport in Schottky contacts. The current-voltage relationship according to diffusion theory is given by

\[ J = qN_c \mu E_m \exp \left( \frac{-q \Phi_B}{kT} \right) \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right] \]

where \( N_c \) is the effective density of states in the conduction band of the semiconductor, \( \mu \) is the electron mobility, \( E_m \) is the maximum electric field strength in the barrier, and \( q \Phi_B \) is the Schottky barrier height.

Bethe showed [5] that the current is limited by thermionic emission over the barrier and is not in agreement with Eq.(2.3). The effect of drift and diffusion in the depletion region is assumed to be negligible in the thermionic emission theory. Only those electrons with
energy exceeding the height of potential barrier will be able to reach the top of the barrier and then emit into the metal. Under a forward bias $V$, the electron concentration in the semiconductor just inside the interface is given by

$$n = N_e \exp \left( \frac{E_c - E_F}{kT} \right)$$  \hspace{1cm} (2.4)

where $E_c$ is the energy at the bottom of the conduction band in the semiconductor just inside the interface, and $E_F$ is the quasi Fermi level for electrons at the interface. The thermionic theory assumes that the electrons entering in the metal have energy higher than the metal electrons and the quasi-Fermi level for electrons remains horizontal throughout the depletion region, which leads to

$$E_c - E_F = q \Phi_B - qV \quad .$$  \hspace{1cm} (2.5)

Therefore Eq.(2.4) becomes

$$n = N_e \exp \left( \frac{-q(\Phi_B - V)}{kT} \right) \quad .$$  \hspace{1cm} (2.6)

Using elementary kinetic theory the flux of these electrons across the interface from the semiconductor to the metal can be given by $n\bar{u}/4$, where $\bar{u}$ is the average thermal velocity of electrons in the semiconductor. The current density from semiconductor to the metal $J_{s\rightarrow m}$ is given by

$$J_{s\rightarrow m} = \frac{qN_e\bar{u}}{4} \exp \left( \frac{-q(\Phi_B - V)}{kT} \right) \quad .$$  \hspace{1cm} (2.7)

If no bias is applied then the flux from metal to semiconductor will balance the $J_{m\rightarrow s}$. The current density from the metal to the semiconductor can be written as

$$J_{m\rightarrow s} = -\frac{qN_e\bar{u}}{4} \exp \left( \frac{-q(\Phi_B)}{kT} \right) \quad .$$  \hspace{1cm} (2.8)
So the net current density is given by

\[
J = \frac{qN_c n_0}{4} \exp \left( -\frac{q\Phi_B}{kT} \right) \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right]
\] (2.9)

For a Maxwellian distribution, the average velocity \( \bar{u} \) is given by

\[
\bar{u} = \sqrt{\frac{8kT}{\pi m'}}
\] (2.10)

The effective density of states \( N_c \) in the conduction band of the semiconductor is given by

\[
N_c = 2 \left( \frac{2\pi m' kT}{h^2} \right)^{3/2}
\] (2.11)

Putting these values in Eq.(2.9) gives

\[
J = \left( \frac{4\pi m' q k}{h^3} \right) T^2 \exp \left( -\frac{q\Phi_B}{kT} \right) \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right]
\] (2.12)

or

\[
J = A^* T^2 \exp \left( -\frac{q\Phi_B}{kT} \right) \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right]
\] (2.13)

where \( A^* = \left( \frac{4\pi m' q k}{h^3} \right) \) is the Richardson constant corresponding to the effective mass \( m' \) in the semiconductor. Eq.(2.13) can also be written in the form

\[
J = J_0 \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right]
\] (2.14)

where \( J_0 \) is the saturated current density and given by

\[
J_0 = A^* T^2 \exp \left( -\frac{q\Phi_B}{kT} \right)
\] (2.15)

Eq.(2.14) represents the current-voltage relation for an ideal Schottky barrier diode.
2.3 SAMPLE PREPARATION

As shown in section 2.2, when a metal makes intimate contact with semiconductor, a barrier may be formed at the metal-semiconductor interface. This kind of barrier is rectifying in nature and is known as Schottky barrier. If an Ohmic contact, which is non-rectifying in nature, is made on the same semiconductor sample then this complete system is known as Schottky barrier diode. In the present work, Au/n-Si (100) and Ni/n-Si (100) Schottky barrier diodes were fabricated. Before deposition of metals wafers were properly cleaned using the procedure described in the following section:

2.3.1 Chemical cleaning procedures for Si wafer

2.3.1.1 Degreasing

Step1: Dip the wafer in trichloroethane, (TCE), boil for 10 mins.

Step2: Dip the wafer in acetone, boil for 10 mins.

Step3: Dip the wafer in methanol, boil for 10 mins.

Step4: Rinse the wafer in de-ionized (DI) water.

Step5: Dry the Wafer.

2.3.1.2 RCA Cleaning

SC 1:

Step1: Solution containing DI water: H₂O₂: NH₄OH in the ratio of 5:1:1 is prepared. The Si wafer is immersed in solution for 10 mins. Subsequently the wafer is thoroughly rinsed in DI water.
Step 2: Wafers are immersed in DI water: HF (50:1), for a few seconds.

SC 2:

Step 1: This solution contains DI water: H₂O₂: HCL in the ratio of 6:1:1. The Si wafer is immersed in solution for 10 mins. Followed by thoroughly rinse in DI water.

Step 2: Wafer is immersed in DI water: HF (50:1).

2.3.1.3 Piranha

Step 1: This solution contains H₂SO₄: H₂O₂ in the ratio 7:1. The wafer is immersed in solution for 10 mins.

Step 2: The wafer is thoroughly rinsed in DI water.

Step 3: Wafer is immersed in DI water: HF (50:1), for few seconds.

Step 4: Dry the wafer.

2.3.2 Schottky diode fabrication

Al was deposited on cleaned backside surface by thermal evaporation method in a high vacuum chamber followed by a temperature treatment in argon gas environment at 525°C for 25 minutes to make low resistivity Ohmic contacts. After standard cleaning, the front side oxide was removed by an HF dip and subsequently Schottky contacts were formed by depositing metal (Au or Ni) on the sample having Ohmic contact by electron beam heating technique in an ultra high vacuum (UHV) chamber. A 100 nm metal layer was deposited through a stainless steel mask having contact diameter of 2 mm at a base pressure of 10⁻⁸ mbar region. The photograph of the cryo-pump operated UHV chamber used for Schottky
diode fabrication is shown in Figure 2.3. The thickness of the metal layer was monitored with quartz crystal thickness monitor.

2.4 ION IRRADIATION FACILITIES

2.4.1 Low energy ion beam facility (LEIBF)

A low energy ion beam facility [6,7] based on electron cyclotron resonance (ECR) ion source, at IUAC, New Delhi was used for low energy (few keV) ion irradiation. The important feature of this facility is the availability of large currents of multiple charged
positive ions from an ECR ion source placed entirely on a high voltage platform. Materials science chamber in low energy ion beam facility is shown in Figure 2.4. All the electronic control devices and vacuum systems related to the 10 GHz ECR source including high power ultra high frequency (UHF) transmitter, high voltage power supplies for extractor and Einzel lens placed on the 200 kV high voltages (HV) platform, are controlled through optical fiber communication in multiplexed mode. The energy of the ions emerging from the accelerator is given by $E = q(V_s + V_p) \text{keV}$, where $q$ is the charge state of the ion, $V_s$ and $V_p$ are the potentials in kV of the source and HV platform, respectively.
Nearly 20 samples could be mounted on the target ladder in the materials science experimental chamber and the ladder also has provisions for controlling irradiation temperature. A constant temperature up to 500° C can be maintained using a temperature controller during irradiation. For uniform irradiation, there is an electrostatic beam scanner capable of scanning an area of 50 mm × 50 mm on the sample in x- and y- directions.

2.4.2 Pelletron Accelerator

Inter-University Accelerator Centre (IUAC), New Delhi, Pelletron has a 15 UD tandem electrostatic accelerator [8], capable of accelerating almost any ion from proton to uranium (except Ne, Ar, Kr, and Xe) to the energies from 50 MeV to 250 MeV. A schematic diagram of the Pelletron accelerator is shown in Figure 2.5. The Pelletron having vertical geometry is installed in a stainless steel tank, which is a 26.5 m long and 5.5 m in diameter. It is filled up with sulfur hexa-fluoroide (SF₆) insulating gas at a pressure of about 6-7 bar. At the middle of tank, there is a high voltage terminal of about 1.52 m in diameter and 3.81 m in height. This terminal can be charged to a potential upto 16 MV. A potential gradient is maintained with ceramic titanium diffusion bonded accelerating tubes from high voltage to ground at the top of the tank as well as bottom of the tank. The negative ions are produced inside a sputter type ion source known as MC-SNICS (Multi-Cathode Source of Negative Ions by Cesium Sputtering) and pre accelerated to about 250 keV. The negative ions of different masses are analyzed by a 90° dipole magnet called injector magnet and are turned in vertically downward direction towards the high voltage terminal. On reaching the terminal, the ions pass through a stripper (Carbon foil or N₂ gas) that strips the ions off their electrons, thus changing them to positive ions, which are further accelerated as they proceed.
Figure 2.5: Schematic diagram of 15UD Pelletron accelerator.
towards the bottom of the tank at ground potential. The final energy of the ions emerging from the accelerator is given by

\[ E = E_{\text{deck}} + (1+q) V_T, \]  

(2.16)

where \( V_T \) is the terminal potential in MV, \( q \) is the charge state of the ion after stripping and \( E_{\text{deck}} \) (few hundred kV) is the deck potential of the MC-SNICS source. These high energy ions are analyzed in energy with the help of a 90° bending magnet known as analyzer magnet and directed to the desired experimental beam line with the help of a multiport switching magnet which can deflect the beam in any of the seven beam lines in the beam hall. The whole beam line of the accelerator is in ultra-high vacuum (UHV). During passage of ions through accelerator beam line, the ion beam is kept centered and focused using steering magnets and quadrupole triplet magnets. The beam is visually monitored by glow on quartz and beam profile monitors (BPM). The beam current is measured by means of Faraday cups.

2.4.2.1 Materials science beam line

The accelerated beam from the Pelletron is brought to the beam hall and can be switched to anyone of the seven beam lines. Among them, one is materials science beam line, which is at 15° to the right with respect to the zero degree beam line. Materials science beam line has three chambers connected one after another. The high vacuum chamber where most of the irradiation and elastic recoil detection analysis experiments are performed is shown in Figure 2.6. It is of 68 cm diameter and is made of stainless steel. The vacuum inside this chamber is created by using turbo molecular pump. The vacuum during the irradiation experiment is of the order of 10^{-6} mbar.
To conduct *in situ* transport measurements, a variable temperature cryostat was designed and installed in the high vacuum chamber in materials science beam line. The schematic diagram of cryostat is shown in Figure 2.7. The double-walled stainless steel ladder has a provision for cooling the samples by filling liquid nitrogen in the inner hollow tube. The samples holders used are machined using electro discharge machining (EDM) from oxygen free high conductivity (OFHC) copper and are mounted in the slot at the bottom of the ladder. The sample is mounted on the specifically designed copper sample holder. Electrical connections to the samples are provided by two ten pin electrical feed-throughs.
Figure 2.7: Layout of the cryostat for in situ electrical measurements.

The provision of twenty electrical connections enables mounting of multiple samples at the time for in situ studies. A Lakeshore Si diode and 50 watt heater mounted on sample holder are used to monitor the temperature. The temperature was controlled by Lakeshore 331 temperature controller. A temperature of 90K is achieved after filling liquid nitrogen in cryostat. The cryostat design is such that the sample ladder can be moved downward/upward and rotated (upto 360°) to bring the sample exactly perpendicular to the ion beam. A stepper motor in conjunction with suitable mechanical assembly is used to control the up and down motion of the ladder. This up and down motion can also be done in remote mode from the data acquisition room using an electronic control system. For irradiation, the beam is scanned
in x- and y- directions with the help of a magnetic scanner. The scanning ensures the uniformity of irradiation over the whole area of the sample. A cylindrical enclosure of stainless steel (suppressor) surrounds the sample ladder, which is kept at a negative potential of nearly 120 V. This enclosure suppresses the secondary electrons coming out of sample during irradiation. An opening in the suppressor allows the ion beam to fall on the sample. The total number of the particles/charges falling on the sample can be estimated by a combination of the current integrator and the pulse counter from which the irradiation fluence can be measured.

The various in-situ techniques developed and installed in high vacuum chamber for electrical characterization of semiconductor materials are described below in Section 2.5.

2.5 SCHOTTY DIODE CHARACTERIZATIONS

2.5.1 Current-voltage characterization

2.5.1.1 Theoretical basis for I-V measurements

The current-voltage (I-V) characteristics of a rectifying Schottky contact are used to determine the Schottky barrier height. The I-V relationship for an ideal Schottky diode under thermionic emission is given by Eq.(2.14). But most of the Schottky barrier diodes exhibit non-ideal behaviour having contribution from other transport processes like tunneling, generation-recombination etc. in current. The current I through a Schottky contact under forward bias \( V \) at a fixed temperature \( T \) is normally described with the thermionic emission equation [2]

\[
I = I_0 \left[ \exp \left( \frac{q(V-I_R)}{nkT} \right) - 1 \right]
\]  

(2.17)
where \( n \) is the ideality factor, \( R_s \) is the diode series resistance and other symbols have their usual meanings. Ideality factor describes the deviation of practical contacts from the pure thermionic-emission model characterized by \( n=1 \). From a fit of linear region of the forward bias semilogarithmic \( I-V \) curve (where \( V > \frac{3kT}{q} \) and series resistance is negligible) the values of ideality factor and Schottky barrier height can be determined. The straight line portion of the plot yields \( I_0 \) by extrapolating it to \( V=0 \), and it gives \( n \) from the slope \( S=d(lnI)/dV \). At a temperature \( T \), ideality factor is obtained using the relation

\[
n = \frac{q}{kT} \tag{2.18}
\]

From the intercept of \( \ln(I) \) versus \( V \) plot on the y-axis, the value of \( I_0 \) is obtained. From \( I_0 (=J_0A, \text{here } A \text{ is the contact Area}) \), the barrier height is obtained using Eq.(2.15) and is given as

\[
\Phi_B = \frac{kT}{q} \ln \left( \frac{AA^*T^2}{I_0} \right) \tag{2.19}
\]

In case \( A^* \) is not known it is still possible to deduce the Schottky barrier height. The diode forward \( I-V \) characteristics are obtained at a number of temperatures and \( I_0 \) determined at each temperature. A plot of \( \ln(I_0/T^2) \) versus \( I/T \) gives a straight line whose slope gives the Schottky barrier height \( q\Phi_B \) and the intercept on the \( \ln(I_0/T^2) \) axis gives the value of \( A^* \). This method gives the barrier height at 0K.

2.5.1.2 Experimental setup for \( I-V \) measurements

The current-voltage (\( I-V \)) measurement setup for doing electrical characterization of Schottky diodes was tested and installed. For doing \( I-V \) measurements, Keithley's 2400 source meter was used. The schematic diagram for \( I-V \) measurements is shown in Figure 2.8. The temperature is controlled by a stabilization loop consisting of a temperature sensing
diode, a heating resistance and a Lakeshore PID temperature controller, which regulates the temperature to a preset value. The variation of temperature is better than ±0.5 K during measurement at each temperature point. The setup is fully automated with source meter and temperature controller being interfaced to the computer using standard IEEE interfacing. The interfacing program is written using LabVIEW software.

![Schematic diagram for I-V measurement setup](image)

**Figure 2.8:** Schematic diagram for I-V measurement setup

2.5.2 Capacitance-voltage characterization

2.5.2.1 Theoretical basis for C-V measurements

The capacitance-voltage (C-V) technique relies on the fact that the width of a reverse biased space-charge region of a Schottky diode depends on the applied voltage. The capacitance of a reverse-biased Schottky junction, when considered as a parallel plate capacitor, is expressed as [3]

\[
C = \frac{\varepsilon_s A}{W} = \frac{q\varepsilon_s N_D}{\sqrt{2(V_B + |V| - kT/q)}}
\]  

(2.20)
where \( A \) is the area of the Schottky contact, \( W \) is the depletion region width, \( N_D \) is the dopant concentration, \( V_{bi} \) is the built in potential, and \( V \) is the applied reverse bias voltage. Other symbols have their usual meanings. Equation can be used to derive the relation for dopant concentration as

\[
N_D = \frac{2}{q\varepsilon_0 A^2 \left[ d(1/C^2)/dV \right]}
\]  \hspace{1cm} (2.21)

If \( N_D \) is constant throughout the depletion region, one should obtain a straight line by plotting \( 1/C^2 \) versus \( V \). If the \( N_D \) do not remain constant with respect to depth, then differential capacitance method can be used to determine the doping profile from Eq.(2.20). It is to be noted here that the charges that actually move in response to the ac voltage during \( C-V \) measurements are the mobile free carriers and not the ionized dopants atoms. Hence the differential \( C-V \) profiling technique determines the majority carrier concentration and not the doping concentration. The majority carriers do not follow the profile of the dopant atoms if the dopant atom profile varies spatially over distances less than the Debye length.

If the dopant concentration is uniform with respect to depth, then the Schottky barrier height may also be calculated using \( C-V \) technique. The built-in potential is related to the barrier height by the relationship

\[
\Phi_B = V_{bi} + V_0.
\]  \hspace{1cm} (2.22)

Here \( V_0 \) is the energy difference between the conduction band edge and the Fermi level is given as

\[
V_0 = \frac{kT}{q} \ln \left( \frac{N_C}{N_D} \right)
\]  \hspace{1cm} (2.23)
where $N_c$ is the effective density of states in the conduction band. Plotting $1/C^2$ versus $V$ gives a curve with a slope $2/(qε_F A^2 N_D)$, and with intercept on the $V$-axis, $V_i = -V_{bi} + kT/q$. The barrier height is determined from the intercept voltage by

$$\phi_B = -V_i + V_0 + kT/q$$  \hspace{1cm} (2.24)

The barrier height calculated by this method is approximately the flat-band barrier height.

2.5.2.2 Experimental setup for C-V measurements

The capacitance-voltage (C-V) measurement setup for doing electrical characterization of Schottky diodes consists of a Bontoon 7200 capacitance meter and a temperature controller. The schematic diagram for C-V measurements is shown in Figure 2.9. The capacitance meter uses a test signal of 1 MHz having levels of 15, 30, 50 or 100 mV. The capacitance meter works in a measurement range of -2000 pF to 2000 pF. The whole setup is fully automated with capacitance-meter and temperature controller being interfaced to computer using standard IEEE interface. The interfacing program is written using LabVIEW software. The temperature dependent C-V characteristics also can be recorded using a close cycle He refrigerator.

![Figure 2.9. Schematic diagram for C-V measurement setup](image)
2.5.3 Deep level transient spectroscopy characterization

2.5.3.1 Theoretical basis for DLTS measurements

Since its invention deep level transient spectroscopy (DLTS) has been established as a unique and powerful tool for the studies of electrically active defects in semiconductors. The DLTS method is based on capacitance transients produced by thermal emission of carriers from the deep levels within the depletion region in a reverse biased diode (Schottky barrier or MOS structure). Such an emission process is produced by a sudden change of the negative bias value towards a more negative one as shown in Figure 2.10(a), the bias as a function of time changes suddenly at time $t_0$ from a negative value $V_1$ to a more negative value $V_0$. In Figure 2.10(b) the energy band diagram of a Schottky barrier for a n-type semiconductor with a deep level $E_I$ is illustrated, with a depletion region width $W_I$, corresponding to a voltage $V_1$. Traps below the Fermi level are occupied by electrons. As the voltage change to $V_0$, the depletion region width tends to increase, producing a stronger band bending, as shown in Figure 2.10(c). Hence, some of the traps first placed below the Fermi level ($E_F$), are shifted up above Fermi level, increasing their probability of being empty. This means that an emission process starts to take place. As the electrons are released, a charge change in the depletion region is induced, leading to a capacitance transient as shown in Figure 2.10(d). As time goes on, the capacitance tends to attain the value $C_\infty$, corresponding to the steady voltage $V_0$. After restoration of the original bias $V_1$, the charge in the depletion region will be lower than before in the case of a majority carrier pulse, due to carrier stored in the deep levels. These carriers are released through thermal emission, which proceeds exponentially in time, with a time constant given by

$$\tau_e = \frac{1}{kT^2} exp\left(\frac{E_I}{kT}\right) \quad (2.25)$$
This thermal discharging of the occupied trap is monitored by measuring the capacitance of the reverse biased diode as a function of time after the filling pulse. In the first instance, for not too large concentrations, the resulting capacitance transient proceeds exponentially with time, having the same time constant, \( t \),

\[
\Delta C(t) = C(t) - C(\infty) = -\Delta C \exp\left(-\frac{t}{\tau_c}\right) \quad (2.26)
\]

where \( \Delta C \) is the absolute value of the capacitance transient amplitude and \( C(\infty) \) is the steady-state capacitance for \( t \) going to \( \infty \). The amplitude of the capacitance transient is proportional to the trap concentration. The sign of the amplitude is negative for majority charge carrier emission, and positive for minority charge carrier emission.

As mentioned earlier, the main feature of DLTS is to monitor capacitance transient as a function of sample temperature. In the original system proposed by Lang [9] the
capacitance transient is measured at two fixed times \( t_1 \) and \( t_2 \) after the pulse and then the signal \( \Delta C = C(t_1) - C(t_2) \) is plotted. Figure 2.11 shows how the peak-shaped signal will appear as the temperature is varied. The peak maximum corresponds to a time constant \( \tau_{\text{max}} \) defined by the selected instrumental times \( t_1 \) and \( t_2 \) as

\[
\tau_{\text{max}} = (t_2 - t_1) \left[ \ln \frac{t_1}{t_2} \right]^{-1} \tag{2.27}
\]

The corresponding emission rate \( e_{\text{max}} = 1/\tau_{\text{max}} \) is often called the emission rate window. Changing \( t_1 \) and/or \( t_2 \) will change \( e_{\text{max}} \) and hence the peak position \( T_{\text{max}} \), corresponding to a certain deep level \( E_T \). For each deep level present in the material above a minimum concentration limit (\( \sim 10^{10} \text{cm}^{-3} \)) a DLTS peak will show up. The limit of detection of capacitance transient spectroscopy is approximately \( 10^{-5} \) times the background free carrier.

![Figure 2.11: Rate window and peak shaped signal as a function of temperature.](image)
concentration. At typical doping levels of $10^{14}$-$10^{16}$ cm$^{-3}$ sensitivity of the technique is $10^9$-$10^{11}$ defects cm$^{-3}$, several orders of magnitude better than the most of the other techniques used for defect characterization in semiconductors.

A complete analysis of DLTS data yields the defect state concentration, the activation energy for the electronic transition, the majority carrier capture cross-section, and the depth distribution of the defects.

A. Activation Energy

If the temperature scans are repeated for different emission rate windows, a set of peak maxima $t_{\text{max}}$ can be obtained. Activation energy of electron and hole emission can be obtained from the slope of an Arrhenius plot of $1/T$ versus corrected electron and hole emission rates. The intercept is proportional to the majority carrier capture cross section.

B. Capture cross section

The capture cross section of a defect for majority carriers is determined experimentally by measuring the height of the DLTS signal as a function of the duration of the filling pulse at a constant temperature. The signal must saturate at long filling pulses, corresponding to complete occupation of the defects with majority carriers. Plotting $\ln[(\text{saturated maximum signal})-(\text{signal at pulse width equal to } t)]$ versus pulse width $t$, should yield a straight line (for point like defects) with slope equal to the capture rate $c$. For $n$-type materials, capture rate $(c)$ is given by

$$c = n\sigma_n v_{th}$$  \hspace{1cm} (2.28)
Based on the observed kinetics (exponential or logarithmic), it is possible to distinguish point-like and extended defects. From the magnitude of the capture cross section it is also possible to derive the nature of the trap, i.e. whether it is a Coulombic attractive trap (a deep donor in n-type or a deep accepter in p-type material) for \( \sigma_n \) or \( \sigma_p > 10^{-14} \text{ cm}^2 \). Neutral traps have a cross-section in the range \( 10^{-15} \text{ cm}^2 \). Deep levels below \( 10^{-16} \text{ cm}^2 \) can be considered repulsive for the majority carrier, i.e. they correspond to deep donors in p-type and deep acceptor in n-type material. An alternative way to distinguish the charge state of the defect is by studying the electrical field dependence of the activation energy.

**C. Depth profiling**

The DLTS signal from a defect is directly related to its concentration. The concentration of a defect is found using the relation

\[
N_T = 2N_D \frac{\Delta C}{C_0}
\]  

(2.29)

where \( \Delta C \) is measured from the DLTS peak amplitude and \( C_0 \) is the capacitance of the sample at the peak temperature and reverse bias \( V_R \). Combined with C-V measurements, the DLTS technique can be used to determine the defect profiles as a function of the depletion width. The most common way to do it is to measure the incremental change in the DLTS signal, which corresponds to a small change in the pulse amplitude, keeping the reverse bias on the sample constant. This becomes increasingly difficult for shallow junctions, where the fundamental limit of resolution is the Debye length. The Debye length defines a small transition region at the boundary between the space charge region and the electrically neutral region and it is partly depleted of free carriers. DLTS technique works under the assumption that no free carriers exist within the space charge region and electrically neutral region and that the boundary to the electrically neutral region is sharp. This assumption is known as the
depletion approximation. This assumption is satisfied when the width of the space charge region is much larger than the Debye length. It has been shown in many studies that for numerically correct estimation of the defect concentration $\lambda$-effect (position where Fermi level and deep level are crossing) should be taken into account. Zohta et al [10] has introduced correction as

$$f(W) = (W_0 - \lambda_0)^2 - \left(\frac{W_1 - \lambda_1}{W_0}\right)^2$$  \hspace{1cm} (2.30)

where $W_0$ and $W_1$ are depletion widths for reverse bias and pulse, while $\lambda$ is defined as

$$\lambda = L_D \sqrt{2 \ln \left(\frac{c_n N_D}{e_n}\right)}$$  \hspace{1cm} (2.31)

where $L_D$ is Debye length, defined as

$$L_D = \sqrt[2]{\frac{\varepsilon_0 e k T}{e^2 N_D}}$$  \hspace{1cm} (2.32)

The final formula for defect concentration can be written as

$$N_T = 2 \frac{\Delta C_0}{C} N_D \frac{1}{f(W)}$$  \hspace{1cm} (2.18)

To summarize, DLTS is a method that produces a sequence of peaks as the temperature is scanned. Each of the peaks could be interpreted as related to an electrically active defect. In other words, it is a filtering method in which a peak is produced when the emission rate matches the filter rate window. In general, thermal emission transients from deep level states are often small and superimposed on a background potential that changes slowly as the temperature is scanned.
2.5.3.2 Experimental setup for DLTS measurements

The functions described above are done by the experimental setup installed in material science beam line and shown in Figure 2.12. The details of DLTS setup are given in following sections:

![Experimental setup for DLTS measurements](image)

**Figure 2.12:** *Electronic equipments, which are interfaced for measurements of DLTS signals.*

### A. Hardware Description

The block diagram of the DLTS system is shown in Figure 2.13. The system is based on the Boonton 7200 capacitance meter. The Boonton 7200 has a fast response and recovery time less than 50μs after an overload condition. The advantages of Boonton 7200 model in
Figure 2.13: Schematic diagram of the in situ DLTS setup in the beam line.

DLTS systems have been described in detail earlier by Doolittle et al [11]. A Hewlett Packard HP 8012B pulse generator is used to supply the filling pulse (pulse width range: 10ns to 1s) through the capacitance meter to fill the traps in space charge region. The capacitance transient of the sample is measured by the Boonton 7200 and fed to the SCB-68 box inputs of the Data Acquisition Card (DAQ) NI PCI-6251. The oscilloscope allows us to view both, the train of pulses and the capacitance transients produced. The sample was mounted on sample ladder in irradiation chamber and the temperature is read and controlled by a Lakeshore model 331 temperature controller. The capacitance meter and the temperature controller are set up by means of a National Instruments general purpose interface bus (GPIB) interface.
B. Software Description

Software package LabVIEW has been used for data acquisition, instrument control, and to automate the DLTS system. In the course of the thesis, LabVIEW virtual instruments (VIs) program was developed for DLTS measurements, which provides precise instrument control, fast, and accurate data collection, as well as real time display of transient signal. The transient signal from capacitance meter is acquired using DAQ NI PCI-6251 with SCB-68 box. The NI PCI-6251 is a high-speed multifunction M-Series data acquisition board optimized for superior accuracy at fast sampling rates. This has an onboard NI-PGIA 2 amplifier designed for fast settling times at high scanning rates, ensuring 16-bit accuracy even when measuring all channels at maximum speeds. LabVIEW (version 7.1) was used to create a VI to read the capacitance transient from Boonton 7200 capacitance meter. Figure 2.14 shows the front panel of our DLTS VI demonstrating the transient and rate windows. The user is given the option of saving data to a file before starting the data acquisition. The user has to give starting temperature, final temperature, temperature step, stability time, and the positions of cursors to fix the rate windows as the input to the program. The VI has been programmed to collect data until the threshold temperature has been reached. The temperature is ramped as per requirements of the user. The capacitance and capacitance difference at different cursors corresponding to rate windows are saved in file on disc and plotted online on the front panel in different windows. One can fix as many rate windows as one wishes, by using cursors on the front panel screen on transient signal. Acquired data is plotted online and stored in the disk for further analysis. The program is written in such a way that it can be redesigned as per requirements at any stage.
Figure 2.14: Front panel of VI for DLTS System
References


