5.1 INTRODUCTION

This chapter presents the design of the track-and-hold and multiplying digital-to-analog converter functional blocks. They are realized by Switched Capacitors (SC) circuits. Typical SC circuit stage consists of sampling capacitors and Metal Oxide Semiconductor (MOS) switches which turn on and off at the clock rate to store the input signal (charge) on the sampling capacitors and subsequently transfer that charge to the next stage. As the MOS switches are turned on and off, charge is injected from the gate to the drain and the source of these switches. The turn-on resistance of a MOS switch is input signal dependent and creates nonlinear distortion. The charge injection and signal dependent on-resistance of the MOS switches introduce nonlinearity errors in the switched capacitor circuits. Capacitor mismatch is another error source that significantly affects ADC performance. A detailed investigation on circuit nonidealities degrading the performance of the switched capacitor ADC is carried out. Exploration of the circuit techniques for reducing the nonlinearities is addressed in this chapter.

5.2 TRACK-AND-HOLD AMPLIFIER CIRCUIT

Sample-and-hold circuit grabs the signal in certain instances and hold the value at the next set of time period for doing conversion process. Actually ideal Dirac sampling is impractical since, it requires a switch, to switch on and off in infinitely small in time (in the order of pico second (ps)),

CHAPTER 5

DESIGN OF TRACK-AND-HOLD AMPLIFIER AND MULTIPLYING DIGITAL TO ANALOG CONVERTER
analog circuit to process the information in that period and a clock to switch ON (Φ = HIGH) and OFF (Φ = LOW) for such a high speed is practically impossible (Kok Chin Chang 1991). The practical solution is Track-and-Hold (T/H) circuit. Instead of grabbing the signal in the instances, the circuit operates in two modes. In one of the two modes, it tracks the signal and in the other mode, it holds the signal (Waltari and Halonen 2002). Normally, in literature, track-and-hold circuit is known as sample-and-hold circuit. The process of analog-to-digital conversion is shown in Figure 5.1. The continuous time signal is shown in Figure 5.1(a). At certain time instant, it tracks the continuous time signal of the input and then during other time slots, it holds at the constant value that ideally corresponds to the last value of the track instant is as shown in Figure 5.1(b). Hence the output of the T/H circuit is called as sampled data signal. During the hold phase, the ADSC quantizes the sampled data signal and gives the binary numbers equivalent to the sampled data signal as shown in Figure 5.1(d).

(a) Continuous time signal (b) Signal is tracked by track-and-hold circuit (c) Clock signal (d) Binary equivalent of sampled data signal

Figure 5.1 Process of analog-to-digital conversion
In practice, a T/H circuit can be realized by a switch in the form of transistor and capacitor as shown in Figure 5.2. During the track phase, the switch is closed and the capacitor tracks the input signal with certain RC time constant. In the next clock phase, the switch is opened and the capacitor holds the latest value.

![Practical track-and-hold circuit](image)

**Figure 5.2 Practical track-and-hold circuit**

Normally the hold signal contains signal with distortion due to circuit nonidealities. The nonidealities are classified by their associates, they are

- **The error associated with RC time constant**
  Finite acquisition time and thermal noise

- **The error associated with clock signal**
  Sampling time uncertainty
- **The error associated with sampling mode**
  Voltage dependent of switch, track mode nonlinearity and signal dependent sampling instant

- **The error associated with transition from sampling mode to hold mode**
  Pedestal error and charge injection error

- **The error associated with hold mode**
  Hold mode feedthrough and droop

The above nonidealities of the circuit can be compensated by the combination of the following methods:

(i) CMOS switches are replaced for NMOS switches

(ii) Bootstrap (Clock boosting) switches are used in the signal path

(iii) Fully differential bottom plate sampling

**5.2.1 Finite Acquisition Time**

In an ideal sampler, the signal is tracked instantaneously, but in a practical track-and-hold circuit, the signal is tracked with finite speed due to RC time constant. The finite acquisition time \( t_{\text{acq}} \) is the time required for the THA output to experience the full scale transition and settle within the specified error band around its final value (Razavi 1995). Clock frequency is shown in Figure 5.3(a) and simple T/H circuit is shown in Figure 5.3(b).
The maximum signal transition occurs when the signal tracking instant is from zero signal value to \(V_{FS}\). Calculate \(\tau\) such that \(V_{OUT}\) settles within \(mT_s\) period and \(\pm \frac{1}{2}\) LSB quantization error. Normally \(m = 0.5\) (assume track and hold phase for equal time intervals). Assuming the step voltage applied as input, the step value is equal to the full scale conversion range. The voltage stored across the capacitor is

\[
V_{OUT}(t) = V_{FS}(1-e^{-t/\tau})
\]

\[
V_{OUT}(t) = V_{FS} - V_{FS}e^{-t/\tau}
\]

\[
V_{FS}e^{-t/\tau} = V_{FS} - V_{OUT}(t) \quad \text{(Quantization error)}
\]

where \(t\) is the time period to settle \((t = mT_s)\) and \(\tau\) is the RC time constant.
Quantization error must be less than \( \pm \frac{1}{2} \) LSB.

Minimum signal can be resolved by ADC is \( \Delta = \frac{V_{FS}}{2^{B_{ADC}}} \) \((5.2)\)

From this Equation, \( V_{FS} \) can be expressed as \( \Delta 2^{B_{ADC}} \)

Hence the quantization error is

\[
2^{B_{ADC}} \Delta e^{\frac{mT_s}{\tau}} < \frac{1}{2} \Delta \tag{5.3}
\]

Taking natural logarithm on both sides of Equation (5.3) gives the number of settling time constant \( M \).

\[
M = \frac{mT_s}{\tau} > \ln \left( \frac{2^{B_{ADC}}}{0.5} \right) \tag{5.4}
\]

Table 5.1 shows the relation between ADC resolution and the settling time constant based on the Equation (5.4).

**Table 5.1  Relation between ADC resolution and the settling time constant**

<table>
<thead>
<tr>
<th>Resolution of the ADC ((B_{ADC}))</th>
<th>Minimum required time constant ((M))</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>4.9</td>
</tr>
<tr>
<td>8</td>
<td>6.23</td>
</tr>
<tr>
<td>10</td>
<td>7.6</td>
</tr>
<tr>
<td>12</td>
<td>9.0</td>
</tr>
<tr>
<td>14</td>
<td>10.4</td>
</tr>
<tr>
<td>16</td>
<td>11.78</td>
</tr>
<tr>
<td>18</td>
<td>13.2</td>
</tr>
</tbody>
</table>
### 5.2.2 Thermal Noise

Any sampling circuit can be considered as consisting of at least a switch and a capacitor. The switch always has some finite on-resistance which generates thermal noise as shown in Figure 5.4. The power spectral density of this noise is the well-known $4kT_R$ ($V^2/Hz$), where $k$ is the Boltzmann’s constant ($1.3807 \times 10^{-23}$), $T$ is the absolute temperature in Kelvin and $R$ is the resistance. The noise in the voltage sample is the resistor noise filtered by the low-pass circuit formed by the sampling capacitor and the switch on-resistance. Integrating the resistor noise spectral density weighted by the low-pass transfer function yields the mean square noise voltage on the capacitor (Johns and Martin 2004, Schreier et al 2005).

![Simple thermal noise generator circuit](image)

**Figure 5.4 Simple thermal noise generator circuit**

\[
\overline{V_n^2} = 4kT R \Delta f
\]

\[
\overline{V_{o_{total}}^2} = 4KTR \int_0^\infty \left| \frac{1}{1 + j2\pi RC} \right|^2 df \quad (5.5)
\]

\[
\overline{V_{o_{total}}^2} = \frac{4kTR}{(2\pi RC)^2} \left[ 2\pi RC \arctan(2\pi f RC) \right]_0^\infty = \frac{kT}{C} \quad (5.6)
\]

Normally, thermal noise is equated to the quantization noise of the ADC.
\[ \frac{kT}{C} = \frac{\Delta^2}{12} \quad \text{and hence} \quad C = 12kT \left( \frac{2^{B_{\text{ADC}}}}{V_{\text{FS}}} \right)^2 \] (5.7)

The minimum value of sampling capacitance \( C_{\text{MIN}} \) and maximum value of switch on-resistance \( R_{\text{MAX}} \) for various \( B_{\text{ADC}} \) can be found from Equations (5.4) and (5.7). For \( V_{\text{FS}} = 2V, m = 0.5 \) and \( f_s = 100\text{MHz} \); \( C_{\text{MIN}} \) and \( R_{\text{MAX}} \) for various \( B_{\text{ADC}} \) are listed in Table 5.2.

**Table 5.2 Relationship between \( B_{\text{ADC}}, C_{\text{MIN}} \) and \( R_{\text{MAX}} \)**

<table>
<thead>
<tr>
<th>Resolution of the ADC (( B_{\text{ADC}} ))</th>
<th>( C_{\text{MIN}} )</th>
<th>( R_{\text{MAX}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>0.814fF</td>
<td>9,84,640 ( \Omega )</td>
</tr>
<tr>
<td>10</td>
<td>13.03 fF</td>
<td>50,328 ( \Omega )</td>
</tr>
<tr>
<td>12</td>
<td>208.5fF</td>
<td>2661 ( \Omega )</td>
</tr>
<tr>
<td>14</td>
<td>3.3356pF</td>
<td>144 ( \Omega )</td>
</tr>
<tr>
<td>16</td>
<td>53.37pF</td>
<td>8 ( \Omega )</td>
</tr>
<tr>
<td>18</td>
<td>853.93pF</td>
<td>0.45 ( \Omega )</td>
</tr>
</tbody>
</table>

**5.2.3 Sampling Time Uncertainty**

Clock jitter may cause variations in the sampling instances which limit the dynamic performance of the T/H circuit (Razavi 1997). The effect of the sampling time uncertainty is illustrated in Figure 5.5, where \( t \) is the desired sampling instant but due to clock jitter \( t + \Delta t \) is the actual sampling instant.
The error $\Delta V_{IN}$ caused by this jitter delay. The error increases with high signal frequencies but is independent of sampling frequency. Much of the error causing sampling time uncertainty can be reduced by using the bottom plate sampling technique. The performance is however fundamentally limited by clock jitter in the clock generator. If the clock jitter is assumed to be random noise with variance $\sigma_t^2$ the error power can be approximated as (Laker and Sansen 1994).

\[
\Delta V_{IN} \approx \frac{dV_{IN}}{dt} \tau_i \quad (5.8)
\]

\[
E\{\Delta V_{IN}\} \approx E\left\{ \left(\frac{dV_{IN}}{dt}\right)^2 \tau_i^2 \right\} \approx E\left\{ \left(\frac{dV_{IN}}{dt}\right)^2 \right\} E\left\{\tau_i^2 \right\} \quad (5.9)
\]

where $E\{\Delta V_{IN}\}$ is the noise power due to sampling time uncertainty.

\[
\approx E\left\{ \frac{d}{dt} A \cos[2\pi f_{in} t]^2 \right\} \sigma_t^2 \quad (5.10)
\]

\[
\approx \frac{1}{2} (2\pi A f_{in})^2 \sigma_t^2 \quad (5.11)
\]

where $A$ is the magnitude of the input signal $V_{IN}$. 

Figure 5.5  Sampling time uncertainty
\[ \text{SNDR}_{\text{aperture}} \approx 10 \log \left( \frac{1}{(2\pi f_{\text{in}} \sigma_t)^2} \right) \quad (5.12) \]

\[ \text{ENOB} = \frac{\text{SNDR}_{\text{aperture}} - 1.76}{6.02} \quad (5.13) \]

The SNDR is independent of the signal frequency. To reduce the sampling time uncertainty, the clock is designed to give maximum rms jitter of one ps (Gustavsson et al 2004). The obtainable ENOB as a function of the clock jitter, \( \sigma_t \), is plotted for different input frequencies in Figure 5.6.

![Figure 5.6 ENOB as a function of sampling time uncertainty](image-url)
The following errors are associated with the sampling transistors.

5.2.4 Voltage Dependence of Switch

An MOS transistor can be used as an analog switch shown in Figure 5.7. The gate voltage of the MOS controls the on-resistance $R_{ON}$ of the drain and source (Razavi 1995).

![Figure 5.7 MOS act as switch](image)

The switch always operates in the linear region and its on-resistance is given by

$$I_{D(triode)} = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_t - \frac{V_{DS}}{2} \right) V_{DS}$$

(5.14)

$$R_{ON} = \left[ \frac{dI_D(triode)}{dV_{DS}} \right]_{V_{DS} \to 0}^{-1} = \frac{1}{\mu C_{OX} \frac{W}{L} (V_{GS} - V_t)}$$

(5.15)

In Equation (5.14), $I_{D(triode)}$ is the drain current during the transistor operating in the linear region, $V_{GS}$ is the gate source voltage, $V_{DS}$ is the drain source voltage and $V_t$ is the threshold voltage of the MOS transistor. In Equation (5.15), $\mu$ is the mobility, $C_{OX}$ is the capacitance per unit area, $W$ is the width and $L$ is the length of the MOS transistor.
From Equation (5.15), it is observed that the MOS switch has following problems

(i) Transistor turns off is signal dependent, occurs when \( \Phi = V_{\text{IN}} + V_t \).

(ii) \( R_{\text{ON}} \) is modulated by \( V_{\text{IN}} \) (\( \Phi = V_{\text{DD}} = \text{Constant} \)).

The above problems can be overcome by using CMOS switch or bootstrap switch.

5.2.5 Track Mode Nonlinearity

A frequency dependent nonlinearity error is introduced in MOS sampling circuits due to variation of the switch on-resistance (the variation in the input signal). For high frequency inputs, this variation introduces input dependent phase shift and hence harmonic distortion (Razavi 1995). The distortion caused by switch-on resistance during the track mode is shown in Figure 5.8. The magnitude of the third harmonic due to the track mode nonlinearity is given by

\[
|HD_3| \approx \frac{1}{4} \frac{A^2}{(V_{GS}-V_t)^2} 2\pi f_{\text{in}} R_C
\]  

(5.16)

![Figure 5.8 Distortion caused by switch-on resistance during track mode](image-url)
To reduce the third harmonic distortion in high speed sampling circuit, either input signal swing is reduced (but this is not feasible for low noise contribution of T/H circuit) or \( \frac{1}{RC} \) is selected greater than the \( 2\pi f_{in} \) (bigger switch). Otherwise CMOS or bootstrap switch is employed in the T/H circuit to reduce the track mode nonlinearity error.

### 5.2.6 Signal Dependent Sampling Instant

Normally ideal sampling instant is the mid of the clock phase. Due to rise time and fall time delay of the clock signal, if the signal is sampled other than \( \frac{V_{DD}}{2} \), it causes signal dependent error (Moscovici 2000). This error is shown in Figure 5.9. This error is more dominant when the rate of change of input signal is faster than the falling rate of the clock signal. The THD of the THA is

\[
\text{THD} = 20 \log \left( \frac{V_{CLK}}{A f_{in} t_F} \right)
\]

(5.17)

\( V_{CLK} \) and \( t_F \) are the amplitude and fall time of the clock signal respectively.

![Figure 5.9 Signal dependent sampling instant error](image-url)
Normally this is not a big issue for high-speed and medium-resolution pipelined ADC. For example, 100MS/s sampling circuit, the clock frequency is 100MHz, the fall and rise time of the clock is few tens of ps. During Nyquist rate, input frequency (50MHz) the peak-to-peak signal occurs during the time interval of 20ns and hence clock fall rate is steeper than rate of change of input signal.

5.2.7 Pedestal Error

Pedestal error voltage is the offset voltage error introduced at the THA output during the transition from track mode to hold mode. This error caused due to finite overlap capacitance $C_{OV}$ between gate and source or drain terminals as depicted in Figure 5.10.

![Figure 5.10 Transition of the switch state from track mode to hold mode](image)

When the gate control voltage $\Phi$ changes the state to turns off the switch, $C_{OV}$ conducts the transition and changes the voltage stored on the hold capacitor $C_H$ by an amount equal to

$$\Delta V = \frac{C_{OV}}{C_{OV} + C_H} V_{CLK} \quad (5.18)$$
\[ \Delta V = \frac{C_{OV}}{C_{OV} + C_H}(V_{IN} + V_t \cdot \Phi_L) \]  
(5.19)

\[ V_{OUT} = V_{IN} - \Delta V \]  
(5.20)

\[ V_{OUT} = V_{IN} \cdot \frac{C_{OV}}{C_{OV} + C_H}(V_{IN} + V_t - \Phi_L) \]  

\[ V_{OUT} = V_{IN}(1+\varepsilon) + V_{OS} \]  
(5.21)

\[ \varepsilon = -\frac{C_{OV}}{C_{OV} + C_H} V_{IN} \quad \& \quad V_{OS} = -\frac{C_{OV}}{C_{OV} + C_H}(V_t - \Phi_L) \]

In Equation (5.19), \( \Phi_L \) stands for \( V_{CLK} = 0V \). In Equation (5.21), \( \varepsilon \) stands for nonlinearity error and \( V_{OS} \) stands for offset voltage. Pedestal voltage error can be reduced to minimum by selecting a larger value of the hold capacitor.

### 5.2.8 Charge Injection Error

In addition to finite on-resistance, the MOS switch exhibits channel charge injection. When the MOS switch is on, it carries a strong channel charge under strong inversion region which can be expressed as

\[ Q_{Ch} \approx W L C_{OX}(V_{GS} - V_t) \]  
(5.22)

When the device is turned off, this charge leaves the channel through the drain and source terminals, introducing the error voltage in the sampling capacitors as depicted in Figure 5.11. If the charge is not distributed uniformly over the drain and source terminals, it causes a nonlinearity error in the T/H circuit (Wegmann et al 1987, Ding and Harjani 2000). This error can be eliminated by using the bottom plate sampling technique.
5.2.9 Hold Mode Feedthrough

The percentage of input signal appearing at the output during the hold mode is called the hold mode feedthrough (Plassche 2007). This effect appears because the switch has parasitic capacitance path between the source and drain via gate overlap capacitance even in off state. This is shown in Figure 5.12. This causes an additional noise in the T/H circuit. The hold mode feedthrough can be expressed as

\[
\frac{V_{\text{OUT}}}{V_{\text{IN}}} \bigg|_{(\text{hold})} \approx \frac{C_{\text{OV}}}{C_{\text{H}}} \frac{2\pi f_{\text{in}} R_{\text{OUT}} C_{\text{OV}}}{4\pi f_{\text{in}} R_{\text{OUT}} C_{\text{OV}} + 1}; \quad C_{\text{H}} \sqsubset C_{\text{OV}} \quad (5.23)
\]

\( R_{\text{OUT}} \) is the output resistance of the clock circuit. \( R_{\text{OUT}} \) is selected such that, for the maximum input frequency, the hold mode feedthrough should be minimum.

\[ Figure 5.12 \text{ Hold mode feedthrough} \]
5.2.10 Droop Rate

When the T/H circuit is in the hold mode, the output signal is stored on the hold capacitor. The voltage across the hold capacitor is sensed with an amplifier with a small input bias current. This input bias current, together with possible leakage currents, discharge the hold capacitor, resulting in a droop of the voltage across this capacitor (Plassche 2007).

\[ V_{\text{droop}} = \frac{I_{\text{leakage}}}{C_H} T_{\text{CONV}} \]  

(5.24)

where \( I_{\text{leakage}} \) is the leakage current, \( T_{\text{CONV}} = \frac{\text{CLK}}{2} \), where \( \text{CLK} = \frac{1}{f_S} \).

Larger value of hold capacitor is selected so as to reduce the droop rate.

5.2.11 Compensation methods for Circuit Nonidealities

The nonidealities of the switched capacitor circuit cause nonlinearity errors in the ADC. These nonlinearity errors can be reduced by combining the following compensation methods.

5.2.11.1 CMOS Switch

The signal swing is limited by the dynamic range of the MOS switches. In NMOS switches, the dynamic range is \( V_{\text{DD}} - V_{\text{in}} \), where \( V_{\text{in}} \) includes the body effect also. Hence in the simple NMOS switch, the dynamic range of the signal swing is limited by \( (V_{\text{DD}} - V_{\text{in}})/2 \). The substantial increase in switch on-resistance results in frequency dependent harmonic distortion component. Complementary switches are used to extend the signal swing as rail-to-rail signal swing. A CMOS switch is depicted in Figure 5.13.
The NMOS switch conducts the signal \( 0 < V_{IN} < V_{DD} - V_{tn} \) and PMOS switch conducts the signal \( |V_{tp}| < V_{IN} \leq V_{DD} \), thereby providing rail-to-rail as input and output signal swing. The on-resistance of the CMOS switch is independent of \( V_{IN} \) as shown in Figure 5.14. It minimizes the harmonic distortion caused by variation in on-resistance (Razavi 1995, Brown et al 2006).

Figure 5.14 Variation in on-resistance of NMOS, PMOS and CMOS switches
The on-resistance of the CMOS switch can be expressed as

\[
R_{ON}^{\text{CMOS}} = \frac{1}{\mu_n C_{\text{OX}} \left[ \frac{W}{L} \right]_n (V_{\text{GSn}} - V_{\text{in}}) || 1}{\mu_p C_{\text{OX}} \left[ \frac{W}{L} \right]_p (V_{\text{GSp}} - |V_{\text{tp}}|)} \tag{5.25}
\]

\[
= \frac{1}{\mu_n C_{\text{OX}} \left[ \frac{W}{L} \right]_n (V_{\text{DD}} - V_{\text{IN}} - V_{\text{in}}) || 1}{\mu_p C_{\text{OX}} \left[ \frac{W}{L} \right]_p (V_{\text{IN}} - |V_{\text{tp}}|)}
\]

\[
= \frac{1}{\mu_n C_{\text{OX}} \left[ \frac{W}{L} \right]_n (V_{\text{DD}} - V_{\text{in}}) - \left( \mu_n C_{\text{OX}} \left[ \frac{W}{L} \right]_n || \mu_p C_{\text{OX}} \left[ \frac{W}{L} \right]_p \right) V_{\text{IN}} - 1}{\mu_p C_{\text{OX}} \left[ \frac{W}{L} \right]_p |V_{\text{tp}}|}
\]

if \( \mu_n \left[ \frac{W}{L} \right]_n = \mu_p \left[ \frac{W}{L} \right]_p \)

then \( R_{ON}^{\text{CMOS}} = \frac{1}{\mu_n C_{\text{OX}} \left[ \frac{W}{L} \right]_n (V_{\text{DD}} - V_{\text{in}} - |V_{\text{tp}}|)} \tag{5.26} \)

The channel charge \( Q_{\text{Ch}} \) accumulated on the NMOS cancels the PMOS charge accumulation once their dimensions are equal. But the \( Q_{\text{Ch}} \) depends on \(|V_{\text{GS}} - V_t|\), which is not same in NMOS and PMOS switches. In high speed applications, the switches must be turned on and off at the same instant, otherwise input dependent phase shift is introduced. Hence to overcome the charge injection error, bottom plate sampling technique is used in switched capacitor circuits.

### 5.2.11.2 Bootstrap Switch

To reduce the signal dependant error associated with the transistor switches and to increase the linearity of the THA, the Bootstrapping technique is employed (Abo and Gray 1999). The ideal bootstrapped MOS switch is
shown in Figure 5.15. During the OFF state ($\Phi = \text{HIGH}$), the gate is grounded and the device is cutoff. Simultaneously, the capacitor, which acts as the battery, is charged to supply voltage. During the ON state ($\Phi = \text{HIGH}$), the capacitor is then switched across the gate and source terminals of the switching device. A constant voltage of $V_{DD}$ is applied across the gate-to-source terminals and a low on-resistance is established from drain-to-source independent of the input signal.

![Ideal bootstrap switch](image)

**Figure 5.15  Ideal bootstrap switch**

The logic can be implemented using an actual bootstrapped switch as shown in Figure 5.16. During the $\Phi$ phase, the transistor $M_{11}$ is to be switched off and during $\Phi$ phase, the transistor $M_{11}$ is to be switched on. During the $\Phi$ phase, $M_8$ and $M_9$ discharge the gate voltage of $M_{11}$ to ground. At the same time capacitor $C_{boot}$ charges $V_{DD}$ via $M_3$ and $M_{12}$. This capacitor will act as a battery across the gate and source of $M_{11}$ during $\Phi$ phase. $M_7$ and $M_{10}$ isolate the switch from $C_{boot}$ while it is charging up. During the $\Phi$ phase, $M_5$ pulls down the gate of $M_7$ and makes a conducting path between the capacitor and $M_{11}$. $M_{10}$ enables gate $G$ to track the input voltage $V_{IN}$ at source $S$ shifted by $V_{DD}$ and set the gate-source voltage constant regardless of the input signal. $M_6$ ensures that the $M_7$ gate voltage does not go beyond $V_{DD}$. And $M_8$ reduces the $V_{GS}$ and $V_{GD}$ experienced by the device $M_9$ during $\Phi$. 
phase. To reduce the latch up problem, $M_7$ substrate is tied up with its source terminal. $C_{boot}$ must be sufficiently large to supply charge to the gate of the switching device in addition to all parasitic capacitances in the charging path. Otherwise, charge sharing will significantly reduce the boosted voltage according to Equation (5.27).

$$V_G = V_S + \frac{C_{boot}}{C_{boot} + C_p} V_{DD}$$ \hspace{1cm} (5.27)

where $V_S$ is the source voltage of the switch and $C_p$ is the parasitic load at the gate of the switch transistor when $\Phi$ is high (Abo and Gray 1999, Jian Li et al 2008). The $V_G$ (gate voltage) and $V_D$ (drain voltage) of bootstrap switch for 1V input signal and 100MHz sampling frequency are shown in Figure 5.17. The figure depicts that the gate signal is the superimposed component of $V_{IN}$ and $V_{DD}$.

![Figure 5.16 Actual bootstrap switch](image-url)
5.2.11.3 Bottom Plate Sampling Technique

Bottom plate sampling technique is used to eliminate the charge injection error in switched capacitor circuit (Allstot and Black 1983, Lee and Meyer 1985). The circuit-level implementation of the bottom plate sampling technique and the non-overlapping clock phases are shown in Figures 5.18(a) and 5.18(b) respectively.

**Figure 5.17** $V_{IN}$, $V_G$ and $V_D$ of the Bootstrap switch

**Figure 5.18(a)** Circuit-level implementation of the bottom plate sampling technique
In this circuit $C_s$ and $C_F$ are the sampling and feedback capacitors respectively. $C_P$ is the input capacitance (parasitic) of the OTA. When the clock phases $\Phi_1$ and $\Phi_{1e}$ are high, the capacitor $C_s$ tracks the voltage $V_{IN}$ across it. The total charge accumulated on node X in Figure 5.18(a) is

$$Q(X(0)) = -C_s V_{IN}$$  \hspace{1cm} (5.28)$$

$\Phi_{1e}$ falls earlier than $\Phi_1$, the transistor $M_2$ is switched off. The total charge accumulated on node X is

$$Q(X(1)) = -C_s V_{IN} - \Delta Q_2$$  \hspace{1cm} (5.29)$$

$\Delta Q_2$ is charge injection due to $M_2$ turning off. When $\Phi_1$ turns low, $\Delta Q_1$ leads to a change in voltage across all capacitors, but the total charge on node X remains unchanged. During the $\Phi_2$ clock phase, the charge is redistributed to the feedback capacitor.

$$Q(X(2)) = -C_F V_{OUT}$$  \hspace{1cm} (5.30)$$

By charge conversion principle

$$Q(X(1)) = Q(X(2))$$  \hspace{1cm} (5.31)$$

$$-C_s V_{IN} - \Delta Q_2 = -C_F V_{OUT}$$
\[ V_{\text{OUT}} = \frac{C_S}{C_F} V_{\text{IN}} + \frac{\Delta Q_2}{C_F} \quad (5.32) \]

The output signal contains the signal independent offset error \( \frac{\Delta Q_2}{C_F} \). This error can be easily cancelled by using fully differential switched capacitor circuit.

### 5.3 THA ARCHITECTURES

The front-end THA circuit is an important part of the pipelined ADC. The T/H circuit tracks the analog signal during the track period and holds the signal during the hold period. This often greatly relaxes the bandwidth requirements of consecutive MDAC sections which now can work with a DC voltage. Because the THA is often the first block in the signal processing chain, the accuracy and speed of entire application cannot exceed that of the T/H circuit. Hence the design of T/H circuit is more stringent than the overall design requirements of an ADC (Chang-Hyuk Cho 2005). Since, THA has been designed as a high-gain and high-bandwidth module, the power consumption is almost fifty percent of overall power consumption of the pipelined ADC. Hence exploration of the circuit techniques for reducing the power consumption of the THA ultimately reduces the overall power consumption of the ADC. Two different track-and-hold amplifiers are investigated.

#### 5.3.1 Charge-transferring THA

The first architecture is referred to as charge-transferring T/H circuit as shown in Figure 5.19 (Yen and Gray 1982, Lewis and Gray 1987). Four capacitors with the same value are used in this structure. During the
track phase ($\Phi_1 =$ HIGH), the differential input signal is tracked by the two input sampling capacitors $C_S$. Next, during the hold phase ($\Phi_2 =$ HIGH), the bottom plates of the two sampling capacitors are connected together. Thus only the differential charge is transferred to the feedback capacitors. As a result, this T/H can handle very large input common-mode variation. $\Phi_{1e}$ is the early clock phase which performs the bottom plate sampling to avoid the charge injection errors during charge-transfer in THA (Allstot and Black 1983, Lee and Meyer 1985).

Figure 5.19 Charge-transferring track-and-hold amplifier

In this circuit $V_{\text{IN}}^+$, $V_{\text{IN}}^-$ are differential input signals, $V_{\text{OUT}}^+$ and $V_{\text{OUT}}^-$ are differential output signals, $V_{\text{CMI}}$ is the common-mode voltage. The non-overlapping clock phases are as already shown in Figure 5.18(b). During the $\Phi_1$ clock phase, the capacitor $C_S$ acquires the charge. The charge stored in the capacitor on node X is $-C_S (V_{\text{IN}} - V_{\text{CMI}})$. During the $\Phi_2$ clock phase, the
acquired charge is transferred to the $C_F$. The charge on the node $X$ is conserved.

\[ Q(\Phi_1) = Q(\Phi_2) \]  
\[ -C_S(V_{IN} - V_{CMI}) = -C_F(V_{OUT} - V_{CMI}) \]  
\[ -C_SV_{IN} + C_SV_{CMI} = -C_FV_{OUT} + C_FV_{CMI} \]  
\[ -C_SV_{IN} + C_SV_{CMI} - C_FV_{CMI} = -C_FV_{OUT} \]

Hence \[ V_{OUT} = \frac{C_S}{C_F}V_{IN} + \frac{C_F - C_S}{C_F}V_{CMI} \]  
(5.35)

Since \[ C_S = C_F; \ V_{OUT} = V_{IN} \]  
(5.36)

5.3.2 Flip-around THA

The second architecture is the capacitor flip-around THA as shown in Figure 5.20. No charge-transfer occurs in this scheme and only two capacitors are used. During the track phase, the differential input signal is sampled by the input capacitors in the same way as the first THA. However, during the hold phase, the input capacitors are flipped over by connecting their bottom plates to the output of the amplifier. By doing this, both the common-mode and differential-mode charges are transferred (Yang et al 2001, Yun-Shiang Shu and Bang-Sup Song 2008). Though the common-mode feedback circuit of the amplifier will force the output common-mode to the nominal value, its input common-mode level will change according to the difference between the input signal’s common-mode level and the common-mode level of the amplifier output. It means that the amplifier must be capable of handling a large input common-mode variation.
During the $\Phi_1$ clock phase, the capacitor acquires the charge. The charge stored in the capacitor on node $X = -C_S (V_{IN} - V_{CMI})$. During the $\Phi_2$ clock phase, the capacitor is flip-around. The charge stored in the capacitor on node $X = -C_S (V_{OUT} - V_{CMI})$.

$$Q(\Phi_1) = Q(\Phi_2)$$  \hspace{1cm} (5.37)

$$-C_S (V_{IN} - V_{CMI}) = -C_S (V_{OUT} - V_{CMI})$$  \hspace{1cm} (5.38)

Hence $V_{OUT} = V_{IN}$  \hspace{1cm} (5.39)

When parasitic capacitance is ignored, the feedback factor $\beta$ of a flip-around THA is 1, whereas the feedback factor of a charge-transferring THA is 0.5. As the feedback factor of the flip-around THA is twice as large compared to the charge-transferring THA, it requires only half of OTA gain bandwidth to produce the same closed-loop bandwidth. Thus, the same performance can be achieved with much less power by using the flip-around architecture. THA circuit contributes more than fifty percent of noise in ADC. Reducing the THA noise, overall noise of the ADC is significantly reduced.
The second advantage of flip-around architecture is that it contributes less noise. The noise contributed by the track-and-hold amplifier circuit is the summation of noise contribution in the track phase and that in the hold phase. The hold phase noise depends on the topology of the OTA. In the flip-around architecture, the input-referred noise in track phase is \( \frac{kT}{C_s} \), whereas in charge-transferring THA the input-referred noise in the track phase is \( \frac{kT}{C_F} \left(1 + \frac{C_S}{C_F}\right) \). When \( C_S = C_F \), the noise contribution is twice as that of flip-around architecture. The drawback of the flip-around THA is that, an OTA for a flip-around THA should have a large input common-mode range when the input common-mode level is different from the output common-mode level. In this design both the input and the output common-mode levels are set to the middle of a supply voltage. Hence there is no concern about the input common-mode range of an OTA. Therefore, the flip-around architecture is chosen for the advantages related to power and noise. Transient response of the flip-around THA for \( 2V_{pp} \) differential input signal (\( V_{id} \)) and 100MHz sampling frequency is shown in Figure 5.21. The figure depicts that the THA circuit perfectly tracks and holds the input signal at the rate of 100MS/s.

Figure 5.21 Transient response of the flip-around THA
5.4 MDAC DESIGN

The MDAC combines the functions of a track-and-hold, a DASC, a subtracter and a gain amplifier. Each MDAC section is implemented using the switched capacitor circuit with the resolution of 1.5-bit-per-stage and an interstage gain of 2 as shown in Figure 5.22 (Cline 1995, Iizuka et al 2006, Picolli et al 2008).

Figure 5.22 Implementation of MDAC in switched capacitor circuit
During the track phase ($\Phi_1=$HIGH), the input signal $V_{IN}$ is applied to the set of capacitors $C_S$ and $C_F$ and simultaneously quantized per-stage resolution of $B_{eff}+1$ bit through the ADSC function which has the threshold value of $+\frac{V_{REF}}{4}$ and $-\frac{V_{REF}}{4}$. At the end of the track phase, $V_{IN}$ is tracked across $C_S$ and $C_F$ and output of the ADSC is latched. During the hold phase ($\Phi_2=$HIGH), $C_F$ closes negative feedback path around the OTA, the top plate of $C_S$ is switched to the DASC output. The output of ADSC is used to select the DASC output voltage according to the ADSC input. Since the nonlinearity errors present in the MDAC section is the same as THA section nonlinearity errors, the same circuit techniques are employed to reduce the nonlinearity errors in the MDAC section.

$$V_{OUT} = \frac{C_S + C_F}{C_F} V_{IN} - D \frac{C_S}{C_F} V_{REF}; \quad C_S = C_F$$

$$V_{res} = V_{OUT} = 2V_{IN} - DV_{REF} \quad (5.40)$$

### 5.4.1 Selection of the Sampling Capacitors

The minimum size of the capacitor for a MDAC section is selected based on

(i) DNL error due to the capacitor mismatch and

(ii) Thermal Noise consideration
5.4.1.1 Capacitor Mismatch

A precision interstage gain is required to achieve the desired overall ADC linearity. Since the capacitor ratio $\frac{C_S}{C_F}$ determines this interstage gain, capacitor matching is critical. If the capacitors $C_S$ and $C_F$ are not equal, then an error proportional to the mismatch is generated in the residue output (Abo 1999, Yun Chiu et al 2004a). Thus, accurate capacitor matching is required to design a high resolution pipelined ADC. The integrated circuit capacitor value is given by

$$C_1 = \frac{A_1 \varepsilon_{OX}}{t_{OX}} = A_1 C_{OX}$$  \hspace{1cm} (5.41)

where $A_1$ is the area of a capacitor, $\varepsilon_{OX}$ is the dielectric constant of silicon dioxide and $t_{OX}$ is the thickness of oxide. Capacitance value depends on the area and oxide thickness of a capacitor. The main causes of capacitor mismatch are due to over-etching and the oxide-thickness gradient. The relative capacitance error can be expressed by

$$\frac{\Delta C}{C} = \frac{\Delta C_{OX}}{C_{OX}} + \frac{\Delta A_1}{A_1}$$  \hspace{1cm} (5.42)

where $\Delta C_{OX}$ is an error in $C_{OX}$ due to oxide thickness gradient and $\Delta A_1$ is an error in area $A_1$ due to over etching. Since $C_{OX}$ is fixed by a process technology, the accuracy of capacitance can be improved by simply increasing the area. However, in SC circuits the accuracy of a capacitor ratio is of more concern rather than the accuracy of capacitance, because the gain of a MDAC is decided by the capacitor ratio. $\Delta C$ is the difference between $C_S$ and $C_F$. 
\[
\Delta C \equiv C_S - C_F
\]  \hspace{1cm} (5.43)

\[
\Rightarrow C = \frac{C_S + C_F}{2}; \quad C_S = C + \frac{\Delta C}{2} \quad \text{and} \quad C_F = C - \frac{\Delta C}{2}
\]

\[
\frac{C_S}{C_F} \approx 1 + \frac{\Delta C}{C}
\]  \hspace{1cm} (5.44)

The approximation holds if \( \frac{\Delta C}{C} \ll 1 \). Therefore residue transfer function in Equation (5.40) is changed as

\[
V_{\text{res(new)}} = \left(2 + \frac{\Delta C}{C}\right)V_{\text{IN}} - D\left(1 + \frac{\Delta C}{C}\right)V_{\text{REF}}
\]  \hspace{1cm} (5.45)

Therefore, the accuracy of a capacitor ratio can be improved if the difference of the mismatch errors of both capacitors is as small as possible. A mismatch error in the accuracy of a capacitor ratio due to over etching can be minimized by implementing capacitors with an array of small equal sized unit capacitors (Johns and Martin 2004). A mismatch error in the ratio accuracy of capacitors is due to the variation of oxide thickness. This mismatch can be minimized by laying out capacitors in common-centroid geometry. The input-referred DNL error of the ADC should be less than \( \pm \frac{1}{2} \) LSB. In a 10-bit pipelined ADC, considering the input-referred DNL error, the capacitor mismatch should be

\[
\frac{\Delta C}{C} < \frac{1}{2^{B_{ADC}-1}}; \quad \text{i.e.} \quad \frac{\Delta C}{C} < 0.1\%
\]  \hspace{1cm} (5.46)

It is possible to achieve less than 0.1% capacitor mismatch error in modern digital CMOS technology.
5.4.1.2 Thermal Noise consideration

In analog-to-digital converters, quantization noise is equal to the thermal noise. Quantization noise of the 10-bit ADC = $\frac{\Delta^2}{12}$, where

$\Delta = \left( \frac{V_{FS}}{2^{B_{ADC}}} \right)$; in this design $V_{FS} = 2V_{p-p}$.

Variance of the total quantization noise = $\frac{\left( \frac{2V}{2^{10}} \right)^2}{12} = (564\mu V)^2$ (5.47)

Hence total input-referred noise is $564\mu V$. The rms value of the total thermal noise referred to the input can be expressed as (Goes et al 1998).

$$V_{n_1} = \sqrt{\frac{V_{n_1}^2_{\text{THA}}}{1} + \frac{V_{n_1}^2_{\text{stage}_1}}{G_1^2} + \frac{V_{n_1}^2_{\text{stage}_2}}{G_1^2G_2^2} + \ldots + \frac{V_{n_1}^2_{\text{stage}_m}}{\prod_{j=1}^{m-1} G_j^2}}$$ (5.48)

In Equation (5.48), $V_{n_1\text{THA}}$ stands for input-referred thermal noise of THA section and $V_{n_1\text{stage}_i}$ stands for input-referred thermal noise of $i^{th}$ stage. Normally in pipelined ADC $G_1=G_2=\ldots=G=2$. Except the track and hold stage other stage’s total input-referred noise is divided by the gain of the preceded stages as in Equation (5.48). Hence the maximum noise budget allowed for THA is normally 50% of overall noise budget and rest of the noise budget is shared by the MDACs. Maximum input-referred noise allowed for track-and-hold amplifier in both the cycles is $282\mu V$. Rest of the noise budget is shared by the other stages. Transient response of the MDAC section for the differential input signal of 800mV is shown in Figure 5.23. The maximum time period allowed for MDAC to settle is 5ns. But the output
waveform \((V_{od})\) depicts that the MDAC settles within half the hold time period (less than 2.5ns).

![ transient response of MDAC section ](image)

**Figure 5.23** Transient response of the MDAC section

### 5.5 SUMMARY

In this chapter, the design of high-speed, low-power and low-noise THA and MDAC functional blocks are presented. THA and MDAC circuits are realized by using actual transistor switches and capacitors. Hence nonidealities are introduced in these analog blocks. A more detailed investigation on the nonidealities that affect the performance of the switched capacitor ADC is discussed and certain circuit techniques are incorporated to reduce the nonlinearity errors. OTA is the key part of the THA and MDAC sections. The main requirements of OTA design are: high-gain, large-bandwidth, large-signal swing, low-noise and low-power consumption under
low-supply voltage. Besides these, high power supply noise rejection ratio, high common-mode noise rejection ratio and high dynamic range are also desirable. Unfortunately, these factors cannot be improved simultaneously and many trade-offs exist among them. So a good OTA design is the optimization of these factors according to the design specification. The following chapter presents the systematic design approach for operational transconductance amplifier to meet the design specifications.