ABSTRACT

There is a pressing need for low-power circuit design due to explosive growth of portable devices and applications for extending their battery life. Moreover, mobile applications demand increasingly larger caches and throughput at low standby power budget. The supply voltage \( V_{DD} \) is scaled down in order to keep the dynamic power consumption under control. This calls for reduction in threshold voltage to maintain high drive current and performance. However, threshold voltage scaling results in substantial increase in subthreshold leakage current \( I_{sub} \), as \( I_{sub} \) is exponentially dependent on the threshold voltage. As \( V_{DD} \) is reduced, the oxide thickness \( t_{ox} \) needs to be scaled down to maintain electrostatic control over the channel. The reduced \( t_{ox} \) causes gate leakage \( I_g \) due to various leakage mechanisms such as Fowler-Nordheim tunneling, direct tunneling, hot carrier injection etc. Therefore VLSI circuits and systems in sub-45 nm technology need serious attention to curb standby power dissipation.

Manufacturing process parameter variations have emerged as a major bottleneck in the efficient design of VLSI circuits and systems in sub-45 nm technology nodes. Process imperfections due to sub-wavelength lithography and device level variations in small-geometry devices such as random dopant fluctuation (RDF) and line edge roughness (LER) are causing adjacent devices on the same chip to exhibit large variations in their circuit parameters, particularly in threshold voltage \( V_t \).

The memory and the adder are the two main building blocks of any digital system. Therefore, this thesis analyzes various SRAM and adder cells with a special focus on variability and power dissipation and proposes circuit level techniques to reduce both power dissipation and variability.

Amongst the non-classical CMOS structures, FinFET is regarded as a promising alternative device at the nanoscale level because of its improved scalability and the effective suppression of short-channel effects. Recent non-CMOS technology such as CNFET (carbon nanotube field effect transistor) is also a promising technology of choice to replace the classical CMOS for designing nanoscale circuits and systems. This thesis also explores the effectiveness of FinFET and CNFET in reducing variability and power dissipation in these key digital building blocks.
INTRODUCTION

Technology scaling results in reduction of the lateral and vertical dimensions of transistors. The supply voltage ($V_{DD}$) is scaled down to reduce power dissipation and also to maintain device reliability (avoid oxide breakdown). The threshold voltage ($V_t$) is proportionally scaled down in order to maintain the performance. However, narrow oxide thickness and low $V_t$ result in significant rise in gate leakage and sub-threshold leakage currents, respectively. Therefore, leakage power is now a significant contributor to the total chip power (see Fig. 1.1). Hence, both dynamic and leakage power reductions are equally essential for the nanoscale design. Therefore, innovative circuit level techniques must be investigated to reduce both of these power components to extend the battery life for portable applications.

Due to aggressive scaling, the number of dopants in the channel of a MOS transistor have decreased from 1000’s (1-$\mu$m technology) to a few dozen (in 45-nm and below), even though the doping concentration increases with the scaling of dimensions. Considering the fact that there are around 100 dopants in the channel for a present generation (45-nm) devices, the number and position of dopants can make geometrically identical adjacent devices behave in a different way in future technologies.

Variability (defined as standard deviation ($\sigma$) to mean ($\mu$) ratio of a design metric) in device characteristics due to RDF (random dopant fluctuation), LER (line-
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edge-roughness), OTV (oxide thickness variations) affects the reliability of nanoscale circuits. High-K dielectric is used in 45-nm technology to provide thicker gate oxide layers in order to reduce the gate leakage current; however the Si/High-k dielectric interface itself introduces large variability. Static variations in process parameters cause a 20× variation in chip leakage power and a 30% variation in its operating frequency. Hence, the device at the nanoscale has become highly unreliable due to the above mentioned sources of variability. Therefore, it is imperative to explore circuit level techniques to mitigate variability.

In a nutshell, the two major design challenges at the nanoscale are the reduction of power dissipation and the mitigation of variations in design metrics of nanoscale circuits. Hence, this work is aimed at exploring circuit level techniques to reduce dynamic power and leakage power in nanoscale circuits. It also attempts to mitigate variability in design metrics of nanoscale circuits such as critical blocks of a digital system namely SRAM and an adder cells.

THESIS ORGANIZATION

The core chapters of this thesis, from Chapter 3 to Chapter 9, are a collection of manuscripts published in various reputed journals. This thesis focuses on the reduction of power consumption and variability in design metrics of logic circuits such as full adder cells and memory circuits such as static random access memory cells. The outline of this thesis is as follows:

- Chapter 2 starts with a discussion on the sources of power dissipation and various circuit level techniques to reduce it. It then describes the sources and influence of variability in nanoscale design.
- Chapter 3 presents a technique to mitigate the impact of PVT variations on design metrics of transmission gate-based eight transistor (TG8T) SRAM cell. It explores the use of full transmission gate to mitigate variations in design metrics of SRAM cell. It analyzes the impact of PVT variations on its read current, read access time, write access time, static current noise margin, and standby power and compares the results with standard 6T SRAM cell.
- Chapter 4 presents a novel technique to reduce standby power dissipation in SRAM cell. It proposes low-leakage 10-transistor SRAM cell (hereafter called LP10T) and compares its design metrics with standard 6T, 9T and Schmitt
trigger based 10T SRAM cells (hereafter called ST10T). Simulation results show significant savings in standby power compared with these cells.

- Chapter 5 presents DTMOS and CCBB techniques-based deep subthreshold 10T SRAM cell (CCBB10T). The proposed cell exhibits narrower spread in its read current, bitline leakage, read access time, and write access time.

- Chapter 6 presents a variability-aware low-leakage reliable (11T) SRAM cell design technique. The cell achieves low power dissipation due to its series connected transistors driven by bitlines and read buffer which offer stack effect. It achieves significant improvements in RSNM, WSNM, write delay and appreciable savings in write power and leakage power at the expense of read delay, read power and extra silicon area. It exhibits narrower spread in leakage power. This proves its robustness against PVT variations.

- Chapter 7 describes the need for alternative technologies and reviews the models of promising emerging devices, which enables to exploit the potential of systems designed in these upcoming technologies for their rapid commercialization. It also evaluates emerging devices such as FinFET and CNFET (carbon nanotube field effect transistor).

- Chapter 8 explores CNFET-based seven-transistor SRAM cell (CNFET-7T) design strategy at 32-nm technology node. It is observed during the investigation that the CNFET-based 7T SRAM cell is more robust against process variations compared with CMOS-based SRAM cell. This is due to the cylindrical geometry of a CNFET. A variation in the gate oxide thickness that strongly affects the drive current and capacitance of CMOS transistors has a negligible impact on the CNFET’s operation.

- Chapter 9 presents an analysis of a 1-bit full adder cell in emerging technologies like FinFET and CNFET. The full adder cell is operated in the moderate inversion region for energy efficiency, robustness and higher performance. The performance of the adder is improved by the optimum selection of important process parameters like oxide and fin thickness in FinFET and number of carbon nanotubes, chirality vector and pitch in CNFET. The optimized CNFET-based full adder (OP-CNFFT) has higher speed, lower PDP (power-delay product) and lower power dissipation as compared with the MOSFET and FinFET full adder cells. The OP-CNFFT
design also offers tighter spread in power, delay and PDP against PVT variations.

• Chapter 10 presents conclusions and a summary of the thesis and suggests topic for future research.

CONCLUSIONS AND ACHIEVEMENTS

This thesis investigated low-power and variability-aware techniques to design digital and memory circuits. Chapter 2 presented the breakdown of power dissipation in digital circuits. It discussed leakage currents in a nanoscale device. It also outlined the general power reduction techniques.

Chapter 3 proposed a technique for designing a variability-aware SRAM cell (TG8T). The architecture of the proposed cell is similar to the standard 6T SRAM cell with the exception that the access pass gates are replaced with full transmission gates. This work studies the impact of $V_t$ (threshold voltage) variation on most of the design metrics of the SRAM cell. The proposed design achieves 1.4× narrower spread in read current ($I_{\text{READ}}$) at the expense of 1.2× lower $I_{\text{READ}}$ at nominal $V_{DD}$. It offers 1.3× improvement in $T_{RA}$ (read access time) distribution at the expense of 1.2× penalty in read delay. The proposed bitcell offers 1.1× tighter spread in $T_{WA}$ (write access time) incurring 1.3× longer write delay. It shows 180 mV of SNM and is equally stable in hold mode. It offers 1.3× higher RSNM (100 mV) compared with 6T (75 mV). It exhibits improved $SINM$ (static current noise margin) distribution at the expense of 1.6× lower $WTI$ (write trip current). It offers 1.05× narrower spread in standby power. Thus, it can be concluded that the proposed design is capable of mitigating the impact of $V_t$ variation to a large extent. This work has been published in [2].

Chapter 4 presented a technique for designing a low power and variability-aware SRAM cell (LP10T). The cell achieves low power dissipation due to its series connected tail transistor and read buffer which offer stacking effect. This work studies the impact of PVT variations on most of the design metrics of the SRAM cell and compares the results with standard 6T, 9T and ST10T (Schmitt trigger based) SRAM cells. Our bitcell exhibits 41% (9%) penalty in read delay at nominal $V_{DD}$ compared with 6T (ST10T). However, it exhibits narrower spread in read delay at all considered
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In particular, it shows 33% (17%) tighter spread in read delay distribution compared with 6T (ST10T) at nominal $V_{DD}$. It offers higher RSNM compared with 6T (3.11×) and ST10T (1.31×) due to isolation of storage nodes from bitlines. It exhibits 2.33× (1.67×) reduction in standby power compared with 6T (ST10T) at nominal $V_{DD}$. It also proves its robustness by showing 3.18× (2.41×) narrower spread in standby power compared with 6T at nominal $V_{DD}$. This work has been accepted for publication in [1].

Chapter 5 proposed a deep subthreshold 10T SRAM cell (CCBB10T) based on DTMOS (dynamic threshold MOS) and CCBB (cell content body bias) techniques. The architecture of the proposed cell is similar to the conventional 10T SRAM cell with the exception that DTMOS (dynamic threshold MOS) is used for the read/write access FETs and CCBB (cell content body bias) scheme is used for bitline droppers (FETs used to drop bitlines). Moreover, the proposed bitcell utilizes single differential port unlike conventional 10T bitcell (CON10T), which utilizes dual differential ports. The proposed design offers 2.1× improvements in $T_{RA}$ (read access time) and 3.2× improvement in $T_{WA}$ (write access time) compared with CON10T at iso-device-area and 200 mV. It proves its robustness against process variations by featuring narrower spread in $T_{RA}$ distribution (by 1.3×) and in $T_{WA}$ distribution (by 1.2×) at 200 mV. This work has been accepted for publication in [4].

Chapter 6 proposed a variability aware low leakage reliable (11T) SRAM cell that consumes 1.19× lower write power with 1.08× penalty in read power and 1.07× penalty in read delay. Our bitcell also achieves 1.24× shorter write delay due to its tail transistors that disconnect the pull-down path during write mode. Major achievements of our bitcell are leakage reduction (by 2.37×) and RSNM enhancement (by 2.8×). It also proves its robustness by exhibiting 1.10× narrower spread in standby power at nominal $V_{DD}$ compared with 6T SRAM cell. However, it incurs 84% area overhead for realizing these improvements. This work has been accepted for publication in [3].

Chapter 7 discussed the need for alternative devices and reviewed the literature on the architecture and modeling of emerging devices such as FinFET and CNFET. It also evaluated and established the superiority of FinFET and CNFET compared with classical CMOS transistors. The evaluation of FinFET is carried out with a XOR/XNOR circuit, simulation result of which has been published in [17].
The CMOS XOR/XNOR offers bad 0 and wider variation at xor output for input vector “00” compared with FinFET realization. This is clearly observable in simulated waveform presented in [17]. Moreover, a significant improvement in EDP variability is also achieved in FinFET implementation. The CNFET is evaluated with a full adder cell, simulation results of which have been published in [7], [29]. The CNFET realization of full adder offers narrower spread in EDP variability. This is apparent from our published work.

Chapter 8 proposed a variation – tolerant dual-diameter CNFET-based 7T SRAM cell (CNFET-7T) in 32-nm technology. The use of appropriate $D_{CNT}$ (diameter of CNFET) and hence its $V_r$ is a critical piece of our design strategy. In this work, dual-$V_r$ and dual-diameter CNFETs are used with suitable chiral vectors for appropriate transistors. It also investigated the impact of process, voltage and temperature variations on its design metrics and compared the results with CMOS-based 7T SRAM cell. The proposed SRAM cell offers 1.35× (1.25×) improvements in standby power on an average at $V_{dd} = 1$ V (0.9 V) and 30% improvement in SNM over CMOS-based 7T cell. It shows its robustness by offering 1.4× (1.2×) narrower spread in read access time at 1 V (0.9 V) compared with its CMOS counterpart at the expense of 1.6× read delay. The proposed bitcell also exhibits higher performance while writing [takes 1.3× (1.2×) shorter write access time at $V_{dd} = 1$ V (0.9 V)]. It also proves its robustness against process variations by featuring tighter spread in write access time variability [1.4× (1.2×) at $V_{dd} = 1$ V (0.9 V)]. This work has been published in [9], [10].

Chapter 9 proposed a 1-bit full adder cell in emerging technologies like FinFET and CNFET that operates in the moderate inversion region for energy efficiency, robustness and higher performance. The performance of the adder is improved by the optimum selection of important process parameters like oxide and fin thickness in FinFET and number of carbon nanotubes, chirality vector and pitch in CNFET. The optimized CNFET-based full adder (OP-CNFET) has higher speed, lower PDP (power-delay product) and lower power dissipation as compared with the MOSFET and FinFET full adder cells. The OP-CNFET design also offers tighter spread in power, delay and PDP variability against process, voltage and temperature variations. This work has been published in [8].
LIST OF PUBLICATIONS

JOURNAL PAPERS


Abstract


CONFERENCE PAPERS


Abstract


Abstract


Abstract


LIST OF SUBMITTED PAPERS

JOURNAL PAPERS


