ABSTRACT

The development in the field of signal and image processing has motivated the researchers to design and implement various algorithms and mathematical tools in the recent past. Converting a given data in time or space domain to other domains such as frequency with the help of transform technique is considered as a powerful mathematical tool by scientific community. Among various transform techniques wavelet and multiwavelet transforms posses several desirable qualities. They produce a transformed signal whose resolution, say in time or frequency can be controlled by the user. This flexibility made them a potential tool in signal processing applications which deal with a certain class of signals known as non-stationary signals. Multiwavelets can possess properties like symmetry, orthogonality, interpolating property and higher approximation order simultaneously. Multiwavelets are application specific, multiwavelet coefficients should be properly selected from the set of multiwavelet families.

In this research work, a convolution based conventional, systolic array and bit serial architecture for 1-D and 2-D DMWT is implemented at different levels of design abstraction. Conventional architecture has low design complexity, whereas systolic arrays improve speed of operation. The internal structure of the processing element is designed in such a way that, the
DMWT is carried out with minimal time delay. The developed systolic array is then verified and validated for few signal processing applications like image processing, signal de-noising (both 1-D and 2-D) OFDM and watermarking. The suitable multiwavelet coefficients are selected by analyzing their performance measures like PSNR or BER. The selected coefficients are used in the conventional and systolic structures.

The performance of the systolic structure is examined by analyzing the area, speed and power. It is found that the area is reduced because the module for one level of transform is used for the subsequent levels of decomposition. The speed and hardware utilization efficiency of the system are increased by using the recursive pyramid algorithm which utilizes the module with reduced idle time.

The speed analysis showed that systolic structure is 20%, 18% and 16% faster than the conventional architecture for signal de-nosing, OFDM and image compression applications respectively. It is also seen that the overall latency of the systolic structure is roughly halved. The performance of the developed structure and conventional structure is compared and found that the reported module is better in terms of area.

The systolic structure developed in the present work is implemented in a reconfigurable Xilinx Virtex5 (xc5vtx240t-2ff1759) FPGA platform for examining the feasibility for real time applications. The hardware
has been verified for different test signals and the results show that the systolic architecture can be used for a speedy forward and reverse discrete multiwavelet transform modules.