CHAPTER 4

DESIGN OF HIGH PERFORMANCE LOW CURRENT MISMATCH CHARGE PUMP

4.1 PREAMBLE

The simulation results and the mathematical proof discussed in the previous chapter show that, the CP PLL has increased output impedance and hence the gain. The simulation results obtained from cadence for different $I_{UP}$ and $I_{DN}$ fluctuation shows the corresponding VCO tracking voltage fluctuations. But, still there is a mismatch between the CP current and is around 0.2%. So more efforts has been applied for developing a CPPLL with the following objective:

4.2 OBJECTIVE

i) To achieve less than 1% difference of the Up/Down current and to reduce the process variation like pressure, temperatures and operating voltage variations that could be observed during manufacturing.

ii) To design a circuit, in order to avoid the Channel Length Modulation (CLM ) effect and Charge sharing problem.
4.3 INTRODUCTION

Since the conception of phase locking was proposed in the Thirties of the 20th Century, it has been widely applied in electronics and communication fields, Behzad Razavi (2002) especially used in large scale digital circuits. CP-PLLs (CP PLP) are mainly used to generate signals and renew the clock pulses during the data transmission with high speed Mark Van Paemel(1994), Qu Qiang and Zeng Lieguang (2006). As a key model, the CP plays an important role in assuring PLLs stability. It converts the digital signals in PFDs (Phase Frequency Detector) into analog signals of Qu Qiang and Zeng Lieguang (2006) Voltage Controlled Oscillator (VCOs). When the phase-locked loop was locked in a certain frequency, the output voltage of CP is demanded to be a fixed value, and any tiny change of which will result in apparent frequency offset. Therefore, it is very important to design a CP circuit which can send a stable output voltage in CP-PLLs plan.

Phase-locked loops are widely used in clock generators and RF transceivers to ensure the accuracy of the oscillator frequency. The CP is an essential block in PLL. The CP consists of two switched current sources. Any current mismatch between the two current sources (i.e., difference between the source and the sink currents) would cause ripples on the control voltage. Ripples result in large phase noise and would also cause spurs on the PLL output signal (Rhee 1999).
4.3.1 Basic Principle

Figure 4.1 shows the circuit diagram of a conventional CP. In the CP, the digital output signals (UP and DN) of the PFD control the two circuit sources ($I_{UP}$ and $I_{DN}$), and charge the capacitance $CL$ via two switches which generally substituted by two MOSFET to obtain the DC level control voltage ($V_{ctrl}$) needed by the Voltage Controlled Oscillator.

In Figure 4.1 the $I_{UP}$ and $I_{DN}$ should be completely equal in theory, but there are many nonideal effects which will result in their mismatching in practice Kyung-Soo Ha et al (2006). Another ubiquitous problem is the charge sharing in conventional CPs which results from the parasitic capacitance of node A and B. The level in node A will be charged to VDD, and in node B be discharged to Ground (GND) when the signal UP and DN are invalid, whereas the node A level will be falling and the node B level will be rising when the signal UP and DN are valid. The difference between $V_{ctrl}$ (control voltage) and node A will not be uniform to the difference between $V_{ctrl}$ and node B, thus bring on the charge redistribution among $CL$, A and B. Because the $I_{ds}$ (Drain to Source current) will change with $V_{ds}$ (Drain to Source voltage), current source $I_{UP}$ or $I_{DN}$ will share the charge. It will result in current mismatch which make $V_{ctrl}$ jittering, and influence the circuit performance. The output $V_{ctrl}$ would be held if the charge and discharge current are well matched. Generally, the net current generated by the CP is not equal to zero because of the current mismatching, it will make the $V_{ctrl}$ increase a fixed value in every phase comparing time. The control voltage $V_{ctrl}$ should be held in an average value to maintain the loop in a locked status (as shown in Figure 4.2(a)), then the phase-locked loop shall bring on phase error which make the net current of the CP be zero in every period, as shown in Figure 4.2(b) where A1 and A2 have the equal area.
Figure 4.1 Conventional Charge Pump Schematic

The phase error resulted from the current mismatch can be expressed as the following formula where $\Delta t_{\text{on}}$, $I_{\text{cp}}$ and $|I_{\text{UP}} - I_{\text{DN}}|$ respectively represent the dead zone time of the PFD, the period of the reference clock, and the offset between CP current and charge, discharge current.

$$\phi_{\text{e}} = 2\pi \times \frac{\Delta t_{\text{on}}}{T_{\text{ref}}} \times \frac{|I_{\text{UP}} - I_{\text{DN}}|}{I_{\text{cp}}}$$ (4.1)

where

- $I_{\text{UP}}$ is the UP current (Current from pMOS)
- $I_{\text{DN}}$ is the Down current (Current from nMOS)
- $I_{\text{cp}}$ is the charge pump current
- $T_{\text{ref}}$ is the reference time
Figure 4.2 Phase Offset Causation (a) Charge and Discharge Current Mismatch and (b) Conventional Charge Pump Current Mismatch
The Equation (4.1) indicates that, to lower the phase error, the dead zone time $\Delta t_{on}$ and mismatch current $|I_{UP}-I_{DN}|$ should be reduced, but the CP current $I_{cp}$ should be increased while the reference clock period is fixed. Holding a definite dead zone time will be propitious to overcoming the PFD dead zone, and the higher current $I_{cp}$ will increase the power consumption and noise, so lessening the mismatch current $|I_{UP}-I_{DN}|$ is the key to lower the CP phase error.

The CMOS CP usually has two current switches implemented as pMOS and nMOS switches controlled by the UP and DN signals respectively. For a positive phase error, the Up signal has a pulse of width proportional to the phase error. On the other hand, a negative phase error results in similar pulses in the Down signal. The operation the pMOS switch is usually controlled by an inverted version of Up signal (UpB) and the inversion delay should be compensated for the Down signal. Ideally both the Up and DN signals shouldn't be high at the same time. However, at PLL lock conditions both signals can be high for a small period of time, which is the physical delay of the circuits involved. If there is any current mismatch between the pMOS and the nMOS switches, it will result in ripples on the control voltage for the VCO. Current mismatch occurs due to many reasons, the most important factors are:

4.3.2 Transistor Channel Length Modulation

Transistor CLM ($l$), changes the current values according to the source-drain voltage of the current source.

CP shown in the previous section suffers from CLM effect especially for short channel length technologies. High output impedance is
needed at the output node to reduce the effect of CLM. This is achieved with the help of low voltage cascode current mirror, this is shown in Figure 4.3

This current mirror is chosen because it provides high output impedance, and low CLM mismatch (Rania Mekky and Mohamed Dessouky 2007).

![Figure 4.3 Low-voltage Cascode Current Mirror](image.png)

4.3.3 Charge Sharing

A common problem of CP is Charge Sharing. For the CP shown in Figure 4.4(a), a Charge sharing is caused by the parasitic capacitance in node pcs and ncs.
When $I_{Up}$ is active, node pcs is charged to $V_{dd}$. When deactivating $I_{Up}$, some of the charge stored in node pcs will leak through the current source device. Since the parasitic of node ncs and pcs can never be matched and this leads to a static phase offset.

The two transistors $M_P$ and $M_N$ in the type B CP shown in Figure 4.4(b) are used to remove the charge from the nodes pcs and ncs, when Up and down are deactivated. This leads to a large reduction in phase offset.

4.3.4 Process Variations

The nMOS and pMOS can never have identical currents. If current mismatch is reduced in typical conditions through careful choice of transistor sizes, significant mismatch can still be observed specially in the fast-nMOS
slow-pMOS process corner (FNSP) or slow-nMOS fast-pMOS Process Corner (SNFP).

By considering all the above facts, a high performance CP is designed and is shown in Figure 4.5, in which the CLM problem is solved as well as current mismatch. A low voltage cascode current mirror is used, in order to copy $I_{UP}$ and $I_{DN}$ from a single current source to ensure that both currents are being equal and a cascode topology is used at the output node, to get high output impedance.

4.4 DESIGN OF HIGH PERFORMANCE CP CIRCUIT

The high performance CP circuit has greatly improves the circuit performance by enhancing the current match and lessening the charge sharing, and at the same time, possessed the characteristics of high operating speed and low power consumption. In Figure 4.5, the capacitances $C_1$, $C_2$ are fill the role of stabilizing the node E and F’s voltage, to avoid instantaneous grid voltage fluctuation of the current source. The voltage $V_c$ in node C will change with $V_{ctrl}$ by inserting an error amplifier which has the high gain and enough to make $V_c$ equal $V_{ctrl}$. Moreover, M11 is designed to be equal to M9, M8 to be equal to M10, M3 to be equal to M5, and M4 to be equal to M6. So that, if UP, DN signals are at high then the current $I_4 = I_3 = I_1$ and $I_2 = I_1 = I_3$ when UP and DN signals are at low.

Finally the current $I_4 = I_2$, which leads up to the result of almost perfect drain-source current matching. M7 and M12 are named as charge eliminating transistor which are used to remove the space charge stored at node A and node B due to the effect of Charge Sharing. Hence, the Charge Sharing problem is successfully restrained.
The high performance CP circuit which uses error amplifier and reference current source to get good matching characteristic, and the use of charge removal transistor is to restrain the charge sharing. All the design has been simulated with Spectre tools.

A high performance CP circuit is illustrated in Figure 4.5, in which the CLM problem is solved as well as current mismatch. A low voltage cascode current mirror is used to copy $I_{Up}$ and $I_{Down}$ from a single current source to ensure that both currents are equal. Figure 4.5 shows the low-voltage cascode current mirror. This current mirror is chosen because it provides high output impedance, and low CLM mismatch (Behzad Razavi 2002).

As shown in Figure 4.5, the Up and Down controlled switches have been embedded in the low-voltage cascade current mirrors, where M5 and M10 are the UP and DN controlled switches respectively. M13 to M16 are the low voltage cascode current mirror transistors. Transistors M7 and M12 are Charge removal transistors which are used to eliminate the charge sharing problem. Finally, the transistors M17 and M18 are the reference current generators. If the UP and DN signals at lock, then the bias voltage of the low-voltage cascode current mirrors is chosen to be Ground (GND) for the pMOS switched mirror, and $V_{DD}$ for the nMOS switched mirror. This provides better matching.
Figure 4.5 High Performance Low Current Mismatch CP

The output impedance, $R_{out}$, is higher than that is given in Equation (3.5), since there is another cascode transistor, $R_{out}$ is given by

$$
R_{out} = \frac{1}{\left[ \left[ 1 + (g_{m1} + g_{mb1})r_{o1} \right]r_{o2} + r_{o1} \right] \left[ \left[ 1 + (g_{m3} + g_{mb3})r_{o3} \right]r_{o4} + r_{o3} \right]} \quad (4.2)
$$

$$
\approx \left[ 1 + (g_{m1} + g_{mb1})r_{o1} \right]r_{o2} + r_{o1} \quad (4.3)
$$

where $R_{out1}$ is seen from the positive terminal of the opamp circuit.

$$
R_{out2} = \frac{1}{\left[ \left[ 1 + (g_{m13} + g_{mb13})r_{o13} \right]r_{o14} + r_{o13} \right] \left[ \left[ 1 + (g_{m15} + g_{mb16})r_{o15} \right]r_{o16} + r_{o15} \right]} \quad (4.4)
$$
\[ \approx 1 + (g_{m13} + g_{mb13}) r_{o13} | r_{o14} + r_{o13} \]  

(4.5)

where \( R_{out2} \) is seen from the negative terminal of the opamp circuit.

With reference to the Equations (4.3) and (4.5), it is observed that, the \( R_{out} \) is increased by a factor of \( 1 + (g_{m13} + g_{mb13}) r_{o13} | r_{o14} + r_{o13} \).

This value is large, and so large length transistors are not needed for having high output impedance.

### 4.5 SIMULATION RESULTS

The high performance low current mismatch CP circuit, at the 1.8V power source, is simulated with Spectre tools. Figures 4.6 to 4.9 show the simulation result of high performance CP circuit. Figure 4.10 shows the variation of the Up/Down current without a gain-boosting circuit as the CP output voltage sweeps from 0 to 1.8 V. The graph has been plotted for both conventional and proposed CPPLL. The maximum difference of the Up/Down current is less than 0.1%. This high performance CP is designed using 1.8V CMOS transistors, good current matching is observed in addition to a wide compliance voltage range of 0.1-1.7 V, which relaxes the VCO design. The maximum value for the current mismatch is 0.086% which is less than 0.1%. Current mismatch result of high performance CP and gain boosting CP is shown in Table 4.1. Table 4.2 shows the transistor sizes of the high performance CP.
Figure 4.6 Transient Analysis to Prove the Stability of $I_{UP}$ and $I_{DN}$ Currents Plots

From the simulation results shown in the Figure 4.6, it is obvious that the variation in the input voltage will create the fluctuation in the CP node voltage and there after it is converted to the variation in the current.

After this initial transient, the charge pump current variations settle down the VCO voltage and the CP current becomes stable. Finally, the stability is established within 0.8 ns.
Figure 4.7 Charging Voltage Node

Figure 4.8 Discharging Voltage Node
Table 4.1 Current Mismatch

<table>
<thead>
<tr>
<th>High performance CP technique</th>
<th>Gain Boosting Technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>Id1</td>
<td>Id1</td>
</tr>
<tr>
<td>Id2</td>
<td>% Mismatch</td>
</tr>
<tr>
<td>(\Delta Id = Id1 - Id2)</td>
<td>(\frac{\Delta Id}{Id1}) * 100</td>
</tr>
<tr>
<td>3.7201-3.7234=0.0033</td>
<td>8.6021 * 10^{-4}\n\approx 0.086\n\approx &lt;1%</td>
</tr>
</tbody>
</table>

Figure 4.9 \(I_{UP}\) and \(I_{DN}\) Current Plots

Figure 4.10 \(I_{UP}\) and \(I_{DN}\) when Feedback Signal Leads Reference Signal in the Proposed CP
Table 4.2 Transistor Sizes of the Proposed Charge Pump

<table>
<thead>
<tr>
<th>Device</th>
<th>Width (μm), L=0.3 μm (180nm)</th>
<th>Device</th>
<th>Width (μm), L=0.3 μm (180nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP13, MP14, MP16, MP17</td>
<td>7.1</td>
<td>MN1, MN2, MN3, MN4</td>
<td>2</td>
</tr>
<tr>
<td>MP8, MP9, MP10, MP11</td>
<td>70</td>
<td>MN5, MN6, MN7, MN12</td>
<td>100</td>
</tr>
<tr>
<td>MP18</td>
<td>200</td>
<td>MN17</td>
<td>200</td>
</tr>
</tbody>
</table>

The aspect ratio selection based on the above Table, the value of the rise and fall time is kept approximately equal. The different values of ‘W’ enables to have 2L channel length in order to reduce the CLM effect, since \( \text{CLM} = \frac{L}{L} \). So if L increases CLM decreases.

Hence, the proposed design shows the highest gain and more stability.

4.6 MATHEMATICAL PROOF FOR REDUCING THE CURRENT MISMATCH

4.6.1 Shielding Property to Reduce the Mismatch

It is the property by which the cascode transistor structure shields the input devices from voltage variations at the output. It could be proved with an illustration.

Considering the two identical NMOS transistors and are used as a constant current sources as shown in Figure 4.11. However, due to the internal circuitry of the analog system, \( V_x \) is higher than \( V_y \) by \( \Delta V \).

Letting try to calculate the \( I_{D1} \) and \( I_{D2} \), by considering the CLM
Then,

\[ I_{D1} - I_{D2} = \frac{1}{2} \left[ \mu_n C_{ox} \frac{W}{L} (V_b - V_{th})^2 (\lambda V_{DS1} - \lambda V_{DS2}) \right] \]  \hspace{1cm} (4.6)

\[ = \frac{1}{2} \left[ \mu_n C_{ox} \frac{W}{L} (V_b - V_{th})^2 (\lambda \Delta V) \right] \]  \hspace{1cm} (4.7)

As depicted in Figure 4.12 (a) to (c), the change in the applied voltage to the drain affects less at the node \( V_{RS} \) as shown by the equivalent circuit of CS with source degeneration resistor.

\[ \Delta V_{RS} = \frac{\Delta V [1/g_m + g_{mb}] R_s}{[1/g_m + g_{mb}] R_s + r_0} \]  \hspace{1cm} (4.8)
The change in current is,

\[ \Delta I = \Delta V_{RS}/R_s \quad (4.9) \]

\[ = \Delta V \left[ 1/\{1+(g_m+g_{mb})R_s\} \right] r_{0+} R_s \quad (4.10) \]

That is,

\[ \Delta V/\Delta I = [1+(g_m+g_{mb})R_s] r_{0+} R_s \quad (4.11) \]

As discussed above, the cascoding reduces the effect of \( V_x \) and \( V_y \) upon \( I_{D1} \) and \( I_{D2} \) respectively. The difference \( \Delta V \) between \( V_x \) and \( V_y \) translates to a difference \( \Delta V_{PQ} \) between \( P \) and \( Q \) equal to

\[ \Delta V_{PQ} = \Delta V \left[ r_{o1}/\{1+(g_{m3}+g_{mb3})r_{o3}\} \right] r_{o1} + r_{o3} \quad (4.12) \]

\[ \approx \Delta V/(g_{m3}+g_{mb3})r_{o3} \quad (4.13) \]

\[ I_{D1} - I_{D2} = \frac{1}{2} \left[ \mu_n C_{ox} W/L \left( V_b - V_{th} \right)^2 \right] \left( \frac{\Delta V}{(g_{m3}+g_{mb3})r_{o3}} \right) \quad (4.14) \]

So, the cascading reduces the mismatch between \( I_{D1} \) and \( I_{D2} \) by \((g_{m3}+g_{mb3})r_{o3}\).

Similarly, with respect to the high performance CP circuit as shown in Figure 4.5, the voltage variation on the drain node of M3 and M1 is reduced by an amount of \( \Delta V/(g_{m1}+g_{mb1})r_{o1} \) on the drain node of M2 and M4.

The same argument can be made for the other wing of the opamp there by, reducing the subsequent current mismatch in the CP. That is,

\[ I_{Up} - I_{Down} = \frac{1}{2} \left[ \mu_n C_{ox} W/L \left( V_b - V_{th} \right)^2 \right] \left( \frac{\Delta V}{(g_{m1}+g_{mb1})r_{o1}} \right) \quad (4.15) \]
which mathematically proves that, the current mismatch is reduced by an amount of $1/(g_{m1}+g_{mb1}) r_{o1}$.

4.7 DISCUSSION ON RESULTS

By using the gain-boosting and low-voltage cascode current mirrors, a high-performance low-mismatch CP is achieved. The Table 4.1 shows that, there is a good current matching characteristic of 0.08 % difference of the UP/Down current and 1% over all process variations. The CP output compliance voltage range of 0.1-1.8 V is achieved for 1.8-V supply voltage. Charge sharing problem has been eliminated with the help of charge removal transistor. With the help of low voltage cascode current mirror, this CP provides high output impedance and hence high gain. Table 4.2 shows the selection of transistor aspect ratio for the reduction of CLM. This is being done by taking transistor bias and output voltage swing into consideration. The circuit is designed using 0.18um TSMC CMOS technology and simulated by Spectre tools.

4.8 CONCLUSION

The High Performance CP get away from the problem of Charge Sharing with the help of charge removal transistor and this CP is also provides high gain by the increased amount of output impedance and low current mismatch which is achieved with the help of low voltage cascode current mirror.

The aspect ratio selection based on the Table 4.2, the value of the rise and fall time is kept approximately equal. The different values of ‘W’ (Width)
enables to have 2L(Length) channel length in order to reduce the CLM effect, since CLM (λ) = \( \frac{\Delta L}{L} \). So if L increases CLM decreases.

The circuit is designed using 0.18um TSMC CMOS technology and simulated by Spectre tools. Hence, this CP has low current mismatch, high output impedance and more stability.

By constructing the full PLL circuit and from the simulation results shown in Figure 4.13, we understand that, the glitches appear in the final output because of the presence of charge injection and there is instability in the control voltage of the VCO.

![Figure 4.13 PLL Final Output with Glitches](image)

Since the control signal is not constant, the PLL has not been locked properly for the incoming signal and there are glitches (a small spike) in the output.

So, in order to overcome the glitches in the output, a modified gain boosting CP is designed, in which transmission gates are connected in parallel to the nodes. This is being discussed in the next chapter.