CHAPTER 3

DESIGN OF GAIN BOOSTING CHARGE PUMP

3.1 PREAMBLE

The literature survey and the works reported till date shows that there is huge requirement for the mismatch reduction between the CP current which subsequently aim for increasing the lock range. This work starts with an objective of the following

3.2 OBJECTIVE

i) To design a gain-boosting CP with good current matching characteristics and high stability.

ii) To increase its output impedance without adding more cascode devices.

3.3 INTRODUCTION

Charge-Pump based Phase-Locked Loops (CPPLL) is broadly used as clock generators in a most of the applications like microprocessors, wireless receivers, and serial link transceivers and so on. CP in PLL provides the theoretical zero static phase offset, and gives the simple and robust design platforms. The CPPLL also produces large frequency and capture range and it can also be used for discrete time analysis.
A typical implementation of the CPPLL consists of a Phase Frequency Detector (PFD), a CP, a passive Loop Filter (LF), and a VCO. The basic PLL structure is shown in Figure 3.1. The PFD commonly generates a pair of digital pulses corresponding to the phase/frequency error between the reference clock and the VCO output by comparing the positive (or negative) edges of the two inputs. The CP then converts the digital pulses into an analog current that is converted into a voltage via the passive loop filter network and this control voltage drives the VCO. The negative feedback of the loop produces the zero phase/frequency error. Like any other feedback system, a CPPLL has to be designed with a proper consideration for stability (Gardner 1980).

![Figure 3.1 Basic PLL Structure](image)

Phase-Locked Loops (PLLs) consist of a Phase/Frequency Detector (PFD), a CP, a Loop Filter (LF), and a VCO, whose output is fed back to the PFD. The PFD compares an external reference signal and the VCO output signal and produces two digital signals (Up and Down), with the width of these two signals being determined by their frequency and phase. The CP converts the PFD output signal into a current that is fed into the LF, which determines the output LF voltage. The LF output voltage causes the VCO to generate a single frequency signal. Any fluctuation in the LF output voltage due to current mismatch in the CP causes a proportional variation in the VCO signal. The drain to source voltage of the n-channel MOS (nMOS) and
p-channel MOS (pMOS) in the conventional CP can vary depending on the latter one’s output voltage, thereby causing the magnitude of the currents in the pMOS (Up) and nMOS (Down) to differ. The LF output voltage fluctuates due to the current mismatch in the CP when the PLL is in the locking state; this causes the VCO output signal to have a large amount of phase noise with spurs (Arora 2005).

3.4 CLASSICAL APPROACHES

The classical approach to CP employs a cascode (Larsson 1999, Rhee et al 2000) and low-voltage cascode topology (Ahola and Halonen 2003) to reduce the Current mismatch by increasing its output resistance. This CPs shows the current matching characteristics down to 2% of the sourcing/sinking current difference. CPs with operational amplifiers shows good current matching characteristics of less than 1% of the sourcing/sinking current difference; however, these CP circuits require a large and oscillation-prone operational amplifier (Young et al 1992, Lee et al 2000). A differential CP with an active LF and common-mode feedback scheme has been used to reduce the current mismatch (Da Dalt and Sander 2003). However, it requires operational amplifiers, a reference voltage circuit, and an analog adder. A replica CP circuit and a bias generator are added to compensate the current mismatch down to 1% (Huh et al 2004). It makes the locking time longer and requires more complicated circuits. An additional CP with a modified PFD is included to compensate the current mismatch (Pamarti et al 2004). Fabrication mismatches between two CPs can cause the unexpected current mismatch in Pamarti et al (2004).

To reduce peak-to-peak jitter due to VCO noise, it is advantageous to keep PLL bandwidth as high as possible. Traditional worst case design would keep the PLL bandwidth and damping factor sufficiently far away from stability limits under all variations of the input reference frequency, the
manufacturing process, and the division ratio in the feedback Path N. For the conventional CPs, by enlarging the output impedance of the current source, the sourcing/sinking current matching is improved. This method, however, cannot produce perfect current matching characteristics because of the sizable output impedance of the practical devices used in the circuit.

3.5 DESIGN OF GAIN BOOSTING CHARGE PUMP

Phase detectors may exhibit a dead zone, resulting in enlarged jitter. A common design technique to avoid a dead zone is to make sure that both Up and Down output signals are fully activated before shutting them both off. This is implemented by generating a reset signal with an AND operation of Up and Down output and introducing a delay before feeding back this signal to reset the phase detector. If the charge sharing in the CP is not perfectly cancelled or if there is a mismatch of and there will always be some current compensation, leading to phase offset and loop filter ripple. A longer reset delay results in a longer period during which the VCO is running at a different frequency due to the compensation current. Therefore, the reset delay should be minimized under the constraint that it has to be longer than the response time of the PFD with some additional design margin to avoid a dead zone.

Figure 3.2 shows the schematic diagram of a charge-pump PLL. The PFD checks the reference and feedback signals and controls the CP to produce a current Ip, which adjusts the control voltage Vc through a Loop Filter (LF). The Voltage-Controlled Oscillator (VCO) oscillates at a frequency that varies with Vc. The feedback signal is the output of VCO, possibly reduced to a different frequency by a frequency divider. Assume that the PLL’s nominal state is a locked state. At the nominal value of Vc, the VCO oscillates at N times the reference signal frequency. Figure 3.3 shows the up and down signal generated from the Frequency/Phase detector and Figure 3.4 shows the amount of charge that has been pumped to the CP from
the PFD. In both the Figure, time \( t \) is plotted in X axis and Up and Down current is plotted in Y axis. The Up current is compared with reference (ref) signal and the Down current is compared with the feedback signal (div) which is obtained from divider network (N). The amount of charge that is being pumped is given by the following equation:

\[
|Q| = \int_{t}^{t+T_{ref}} I_{p}(\tau) \, d\tau = I_{p} \frac{\Delta \phi T_{ref}}{2\pi} 
\]

(3.1)

\[
I_{M} = \frac{|Q|}{T_{ref}} = I_{p} \frac{\Delta \phi}{2\pi} 
\]

(3.2)

Figure 3.2 Schematic Diagram of a CP PLL

Figure 3.3 Up and Down Signal Generated from the PFD
A current mismatch occurs due to the difference between the drain–source voltages of the pMOS and nMOS when dumping the charge to the LF. CP circuit with a gain-boosting circuit, which requires only a few more transistors than the conventional CP. Figure 3.5(a) and (b) shows the concept of the gain-boosting circuit and the simplified gain-boosting circuit, respectively. The idea is to drive the gate of M2 by an amplifier that forces $V_x$ to be equal to $V_b$. Thus voltage variations at the drain of M2 affect $V_x$ to a lesser extent because A3 regulates this voltage. Due to the smaller variations at node X, the current through $ro_1$ and hence the output current remain more constant, thereby yielding higher output impedance.
The output resistance ($R_{out}$) of the gain-boosting circuit is given as follows:

$$R_{out} = A_3 g_m^2 r_{o2} r_{o1} \quad (3.3)$$

where $A_3$ is the gain of Op-amp (Operational amplifier) and $g_m^2$ is the transconductance of M2.

Therefore $R_{out}$ is boosted substantially without the need to stack more cascode devices on top of M2. The circuit can be implemented with the single transistor amplifier (M3) shown in Figure 3.6, exhibiting an output resistance equal to

$$R_{out} \approx (g_m^2 r_{o2} r_{o1}) (g_m^3 r_{o3}) \quad (3.4)$$

where $r_{o3}$ and $r_{o2}$ are Channel ON resistance of the transistor $A_3$, M2.

![Figure 3.5](image)

**Figure 3.5** (a) Concept of the Gain-boosting Circuit and (b) Simplified Gain-boosting Circuit
Figure 3.6 Gain-boosting Circuit

which is similar to the output resistance of a triple-cascode circuit. By using this gain-boosting circuit, a new CP is designed, in which the CLM effect is lessened. Figure 3.7 is the diagram of CP with gain boosting in which MP4 and MN4 are the current sources for the single-transistor amplifiers MN3 and MP3 respectively. The output resistances of MN1 and MP1 are used as $r_{o1}$ as shown in Figure 3.6. When the DN signal is active, MN2 and MN3 operate in conjunction with MN1 to provide a gain-boosting circuit. This increases the output resistance of the CP circuit and enhances the current matching characteristics. This gain-boosting CP circuit is suitable for a low power supply voltage because it does not require stacking more cascode devices to increase the output resistance.
Since the transconductance and output resistance of the nMOS and pMOS are different, the enhancement of the output resistance of the two transistors cannot be the same, and this can result in current mismatch. Therefore, by using an error amplifier and reference current sources, a new CP is designed in order to achieve good current matching characteristics. Figure 3.8 shows the CP circuit with error amplifier.

3.7 IMPLEMENTATION OF DESIGN

In Figure 3.8, transistors M5-M8 are the current mirror which provides voltage \( V_{\text{ref}} \) at the REF node. Transistors M1 to M4 are the CP which gives the voltage \( V_{\text{cpout}} \) at the CPOUT node. As long as the amplifier maintains a high gain, the voltage \( V_{\text{ref}} \) is equal to the voltage \( V_{\text{cpout}} \). For \( M5 = M1, M6 = M2, M7 = M3 \) and \( M8 = M4 \), if the DOWN and the UP signal are high, then \( I4 = I3 = I2 \), and if the DOWN and the UP signal are low, then \( I3 = I2 = I1 \). So, the sinking current \( I4 \) equal to the sourcing current \( I1 \). In this way,
nearly perfect source/sinking current matching characteristics is achieved regardless of the CP output voltages.

Figure 3.8 Charge Pump Circuit with Error Amplifier

3.8 SIMULATION RESULTS

The CP with error amplifier and the conventional CP are simulated by SPECTRE with 180nm, 1.8-V CMOS parameters. This CP shows the current matching characteristics around 5% of the sourcing/sinking current difference. A Figures 3.9 to 3.12 shows the stability, gain of VCO output and the CP current with reference and feedback signal. The graph has been plotted for both conventional and CP with error amplifier PLL. Good current matching characteristics are observed over the CP output voltage ranges 0-1.8-V CMOS process.
Figure 3.9 VCO Control Voltage when Reference Signal Leads Feedback Signal (Conventional Charge Pump PLL)

Figure 3.10 VCO Control Voltage when Reference Signal Leads Feedback Signal (Proposed Charge Pump PLL)
Figure 3.11  VCO Control Voltage when Reference Signal and Feedback Signal Phase AND Frequencies are Equal (Conventional Charge Pump PLL)

Figure 3.12  VCO Control Voltage when Reference Signal and Feedback Signal Phase and Frequencies are Equal (Proposed Charge Pump PLL)
The locking phenomena of the PLL is designed and verified for its locking range from 75MHz to 275MHz. Whenever the frequencies are below 75 MHz and above 275 MHz, the PLL loses its tracking frequency. This experiment is carried out by varying the different frequency of the incoming signal with the designed value for the VCO frequency. The perfect locking will take place at \( \cos \theta = 90 \) and it moves on both sides by 90 degree. The simulated waveform shows the different locking conditions with the reference voltage are shown in Table 3.1.

### Table 3.1 Different Locking Conditions with the Reference Voltage

<table>
<thead>
<tr>
<th>Input</th>
<th>75MHz</th>
<th>125MHz</th>
<th>150MHz</th>
<th>175MHz</th>
<th>200MHz</th>
<th>275MHz</th>
<th>Above 280MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Square Wave</td>
<td>1.75vpp</td>
<td>1.754vpp</td>
<td>1.753vpp</td>
<td>1.752vpp</td>
<td>1.755vpp</td>
<td>1.756vpp</td>
<td>Goes out of Lock, the amplitude decreases to 5V</td>
</tr>
</tbody>
</table>

### 3.9 MATHEMATICAL PROOF FOR INCREASE IN THE GAIN FOR THE PROPOSED STRUCTURE

#### 3.9.1 Cascode Stage

As shown in Figure 3.14 the input signal of a common gate may be a current and a transistor in a common-source arrangement converts a voltage signal to current signal. The cascade of a Common Source (CS) and a Common Gate (CG) stage is called a “Cascode” topology. It provides many useful properties. In Figure 3.14, M₁ generates a small signal drain current proportional to \( V_{in} \) and M₂ simply routes the current to \( R_D \) (Drain Resistance).
In the above Figure 3.13, the transistor, $M_1$ is the input device and $M_2$ is the cascade device. It can be noted that in this example, $M_1$ and $M_2$ carry equal currents. As per the bias conditions of the cascade, if $M_1$ to operate in saturation then the voltage at node $X$ is, $V_x \geq V_{in} - V_{th}$ (where $V_{in}$ is the input voltage and $V_{th}$ is the thevenin voltage) and both $M_1$ and $M_2$ are in saturation, then $V_x$ is determined primarily by

$$V_b: V_x = V_b - V_{gs2}. \quad (3.5)$$

where $V_b$ is the body bias voltage and $V_{gs2}$ is the gate to source voltage of $M_2$

Thus,

$$V_b - V_{gs2} \geq V_{in} - V_{th1} \quad (3.6)$$

where $V_{gs2}$ is the gate to source voltage of $M_2$

$V_{in}$ is the input voltage

$V_{th1}$ is the thevenin voltage of $M_1$

and hence

$$V_b > V_{in} + V_{gs2} - V_{th1} \quad (3.7)$$
For $M_2$ to be saturated,

$$V_{out} \geq V_b - V_{\text{th}2}, \text{ that is}$$

$$V_{out} \geq V_{in} - V_{\text{th}1} + V_{g2} - V_{\text{th}2} \quad (3.9)$$

**Figure 3.14 Equivalent Cascode Stage**

If $V_b$ is chosen to place $M_1$ at the edge of saturation, the minimum output level for which both transistors operate in saturation is equal to the overdrive voltage of $M_1$ plus that of $M_2$. In other words, addition of $M_2$ to the circuit reduces the output voltage swing by at least the overdrive voltage of $M_2$. Also say $M_2$ is stacked on top of $M_1$.

Now analyze the large-signal behavior of the cascode stage shown in Figure 3.15, as $V_{in}$ goes from zero to $V_{DD}$. For $V_{in} \leq V_{\text{th}1}$, $M_1$ and $M_2$ are off, $V_{out} = V_{DD}$ and

$$V_x = V_b - V_{\text{th}2}. \quad (3.10)$$
As $V_{in}$ exceeds $V_{th1}$, $M_1$ begins to draw current, and $V_{out}$ drops. Since $I_{D2}$ increases, $V_{gs2}$ must increase as well, causing $V_x$ to fall.

![Figure 3.15 Input Output Characteristics of a Cascode Stage](image)

Figure 3.15 Input Output Characteristics of a Cascode Stage

As $V_{in}$ assumes sufficiently large values, two effects occur: (1) $V_x$ drops below $V_{in}$ by $V_{th1}$, forcing $M_1$ into the triode region; (2) $V_{out}$ drops below $V_b$ by $V_{th2}$, driving $M_2$ into the triode region. Depending on the device dimensions and the values of $R_D$ and $V_b$, one effect may occur before the other. For example, if $V_b$ is relatively low, $M_1$ may enter the triode region first. Note that if $M_2$ goes into deep triode region, $V_x$ and $V_{out}$ become nearly equal.

To understand the effect of cascode on $R_{out}$, the following illustration is described and mentioned below.

From the discussion of source degenerated common source (CS) amplifier, a small signal equivalent circuit is developed, which includes the effect of body bias as shown in Figure 3.16.
Since the current through $R_s$ is equal to $I_x$, 

$$V1 = -I_x R_s$$

and the current flowing through $R_o$ is given by

$$I_x = (g_m + g_{mb})V1 = I_x + (g_m + g_{mb}) R_s I_x. \quad (3.11)$$

where $g_m$ is the transconductance, $g_{mb}$ is the transconductance due to body bias transistor and $R_s$ is the source resistance.

Adding the voltage drops across $R_o$ and $R_s$ we have,

$$r_o [I_x + (g_m + g_{mb})R_s I_x] + I_x R_s = V_x. \quad (3.12)$$

It follows that,

$$R_{out} = [1 + (g_m + g_{mb})R_s] r_o + R_s \quad (3.13)$$

$$= [1 + (g_m + g_{mb})r_o] R_s + r_o \quad (3.14)$$

Since typically $(g_m + g_{mb})r_o \gg 1$, we have,

$$R_{out} \approx (g_m + g_{mb})r_o R_s + r_o \quad (3.15)$$

$$= [1 + (g_m + g_{mb}) R_s] r_o \quad (3.16)$$
Indicating that, the output resistance is increased by a factor of

\[1 + (g_m + g_{mb}) R_s\]

Since, \(R_{out}\) increases, the gain will also get increased, because

\[\text{Gain (G)} = - g_m \cdot R_{out}\]

where \(g_m\) is the transconductance and \(R_{out}\) is the output resistance.

Similarly, by considering the small-signal characteristics of a cascode stage and assuming both transistors are operates in saturation. If \(\lambda = 0\), then the voltage gain is equal to that of a common-source stage, because the drain current produced by the input device must flow through the cascode device. As illustrated in the equivalent circuit of Figure 3.17, it is clear that, this result depends on the transconductance and body effect of M2.

![Small Signal Equivalent Circuit of Cascode Circuit](image)

**Figure 3.17 Small Signal Equivalent Circuit of Cascode Circuit**

An important property of the cascode structure is it has high output impedance. Hence, for the calculation of \(R_{out}\) of the final circuit, this is described in Chapter 5 and it is viewed as a common-source stage with a degeneration resistor which is equal to \(r_{o1}\). Thus using an Equation (3.16),
\[ R_{\text{out}} = [1 + (g_{m2} + g_{mb2}) r_{o2}] r_{o1} + r_{o2}. \]  

(3.18)

With reference to the design, this is shown in Figure 5.3. The cascade structure is formed by \( M_1 \) upon \( M_2 \) and \( M_3 \) up on \( M_4 \) in one wing of the opamp input similarly \( M_{13} \) upon \( M_{14} \) and \( M_{15} \) upon \( M_{16} \) in the other wing of the opamp boost the gain of the structure by increasing the \( R_{\text{out}} \) as follows:

\[ R_{\text{out1}} = \left\{ \left[ 1 + (g_{m1} + g_{mb1}) r_{o1}\right] r_{o2} + r_{o1} \right\} \parallel \left\{ \left[ 1 + (g_{m3} + g_{mb3}) r_{o3}\right] r_{o4} + r_{o3} \right\} \]  

\[ \approx \left[ 1 + (g_{m1} + g_{mb1}) r_{o1}\right] r_{o2} + r_{o1} \]  

(3.19)

(3.20)

where \( R_{\text{out1}} \) is seen from the positive terminal of the opamp circuit.

\[ R_{\text{out2}} = \left\{ \left[ 1 + (g_{m13} + g_{mb13}) r_{o13}\right] r_{o14} + r_{o13} \right\} \parallel \left\{ \left[ 1 + (g_{m15} + g_{mb16}) r_{o15}\right] r_{o16} + r_{o15} \right\} \]

\[ \approx 1 + (g_{m13} + g_{mb13}) r_{o13}\right] r_{o14} + r_{o13} \]  

(3.21)

where \( R_{\text{out2}} \) is seen from the negative terminal of the opamp circuit.

With reference to the Equations (3.20) and (3.21), it is observed that, the \( R_{\text{out}} \) is increased by a factor of \( 1 + (g_{m13} + g_{mb13}) r_{o13}\right] r_{o14} + r_{o13}. \)

3.10 CONCLUSION AND DISCUSSION ON THE RESULTS

To be brief, a gain-boosting CP that has good current matching characteristics and stability in the PLL is designed. By using a simple gain-boosting circuit to increase its output resistance, a CP with good current matching characteristics is achieved without the need for stacking more cascode devices, operational amplifiers with current mirror is provided to reduce the current mismatch.

This output impedance is similar to triple-cascode output impedance but with less consumed voltage headroom. That is, if the drain
voltage increases due to any variations in the input, its control over the current extends further towards the source. So the uninverted region expands towards the source, shortening the length of the channel region. This effect called channel-length modulation effect.

Since the resistance is proportional to the channel length, shortening the channel decreases its output resistance.

In order to minimize this effect, a high performance low current mismatch CP is being designed and discussed in the next chapter.