CHAPTER 6

CONCLUSION AND FUTURE ENHANCEMENT

6.1 CONCLUSION

This research has focused on the design and development of CP based PLL with the objective of boosting the gain, reducing the current mismatch of the CP, increasing the output the impedance, reducing the CLM effect and Charge Sharing problem. It is also aimed for the jitter reduction at higher frequency.

The complete circuit has been designed in the Cadence Design Environment (CDE) and the simulation is performed using Spectre Tool which supports the foundry based model file simulation. The hardware set of the simulated circuit has been constructed in the board. Signal generator and CRO are used for hardware setup.

Gain Boosting of this design is achieved by the inclusion of opamp instead of cascade effect. It increases the $R_{\text{out}} = [1+ (g_m + g_{mb}) R_s] r_o$ and thereby the gain has increased to the amount of $g_m R_{\text{out}}$. It has been shown by simulation and the stability of the circuit has been increased.

The idea of low voltage cascode with reference current source in the CP design shows that, the mismatch has been reduced from 0.6% to 0.08% of the UP and DOWN current mismatch. The aspect ratio of the circuit design has been made by taking the biasing voltage and output swing into
consideration. The length of the channel has been kept to minimize the CLM effect. The different values of ‘W’ enables to have 2L channel length is reduced the CLM effect, since CLM \((\lambda) = \Delta L/L\). So if L increases CLM decreases.

The mathematical derivation shows that, the current mismatch has been reduced by a factor of \((1/(g_{m3}+g_{mb3})r_{o3})\)where ‘\(g_m\)’ and ‘\(r_o\)’ are the corresponding transistor transconductance and output impedance.

The simulation results of the proposed technique of transmission gate based CPPLL design, shows that the jitter has been reduced and the hardware set shows the lock range of a complete PLL with higher lock range.

The designed CP has good current matching characteristics and is also suitable for low-power-supply-voltage operation because it does not require stacking more cascade devices. Charge sharing problem has been eliminated with the help of charge removal transistor. The low voltage cascode current mirror is used to provide high output impedance and hence high gain. The circuit is simulated using 0.18um TSMC CMOS technology.

6.2 FUTURE ENHANCEMENT

This Research could be extended by involving the ideas of low power IC design to come up with an ASIC of Low power PLL design. The Range of the PLL could also be extended for very huge range in GHz that could be used for RF based applications.

Since this work have used the cascode circuit which helps in the Rout and gain improvement but at the cost of reduction in the output swing by \(2V_{th}\). So a better technique can be devised to overcome this drawback.
This work can be extended for an efficient VCO and Loop filter
design to make a complete ASIC PLL chip.

The backend of this design is made by custom layout for this design
and its parameter extraction is to be done, which could be back annotated to
fine tune the settling time of the PLL and this will complete the whole design
process.

The same design could be reworked for the upcoming 45nm
technology. PLL can be designed for automatic sizing for increasing the
performance and also even to be planned for a design with wider lock range.
The same design could also be worked with multi Vt for enhancing the power.