CHAPTER 5

MODIFIED GAIN BOOSTING CHARGE PUMP FOR LOW CURRENT MISMATCH AND HIGH PERFORMANCE PHASE-LOCK LOOP

5.1 PREAMBLE

The CP design prepared has high gain, high output impedance with reduced CP current mismatch of 0.08%. But still the PLL shows the jitter in the output during high frequency tracking. Hence, this work aims at designing a modified gain boosting CP with the following objective.

5.2 OBJECTIVE

To design a circuit, in order to minimize the high speed glitches.

5.3 INTRODUCTION

A PLL based on a CP is preferred over other types because it has a wide capture range and no systematic phase offset. In practice, nonidealities of the CP degrade the performance of the entire loop. The mismatch between the charging and discharging current introduces steady-state phase offset and increases the reference spurs in a PLL. The variation of the output current amplitude of the CP due to the change of the output voltage will result in variation of the loop bandwidth. Therefore, glitches in the output current will increase the level of reference spurs in frequency synthesizers.
It will also increase the level of jitter generation in Clock and Data Recovery (CDR) systems, which are widely used in multi gigahertz serial data links. Several single-ended CP structures are proposed in the literature (Rhee 1999, Juarez-Hernandez and Diaz-Sanchez 2001, Bahreyni and Filanovsky 2002, Beek and Vaucher 2004, Parker and Weinlader 2005, Leenaerts and de r Tang 2001). A single-ended CP with positive feedback is proposed in Juarez-Hernandez and Diaz-Sanchez (2001) to boost the operational frequency of the CP. An obvious disadvantage of that technique is that, the positive feedback will result in an undesirable hysteresis effect which swallows narrow input pulses. A new technique is proposed in Bahreyni and Filanovsky (2002) to eliminate the high-frequency glitches, which is done at the price of decreasing the operational frequency of the CP. The CP proposed in Beek and Vaucher (2004) uses wide-swing current mirrors which still suffer from heavy mismatch when the output voltage comes close to the rails. The CP proposed in Parker and Weinlader (2005) uses source-switching, but it is slow to turn off the output current. In high-performance applications with high speed glitches suppression requirements, a CP with matched pair of transmission gate is preferred.

5.3.1 High Speed Glitches

As per the discussion in the previous chapters, the CP is made up of pMOS and nMOS switches. When the switches are on, finite amount of charge is held in the channel. The charge that held during ON time flows partially through both drain and source of the device. The amount that is injected through the load capacitance gives rise to control voltage even the inputs are off. This leads to wrong output signal.

However if the MOS transistor is turned OFF while in saturation, then all channel charge flows into the source leaving the drain terminal unaffected. The gate to drain capacitance of a MOS transistor in triode region is given by,
\[ C_{gs} = C_{gs} = \frac{C_{gg}}{2} = \frac{W}{L}C_{ox}/2 \quad (5.1) \]

where \( C_{gs} \) is the gate to source capacitance and \( C_{gg} \) is the gate capacitance.

At this condition, the gate to drain capacitance of MOS transistor in triode region is larger as compared to the capacitance in saturation. Thus, it is always desirable to keep the output transistor in saturation in order to minimize the glitch current.

In practical application, this is hardly the case; switches are generally operated in triode in order to have small ON resistance. There is constant amount of charge in the channel which is held when the switches are active and this charge is being injected to the output nodes, when the switches are turned off. Therefore, the input voltage of the switches has a transition time of \( \Delta T \) while changing from low to high. Hence, the amount of glitch current is given as,

\[ I_{\text{glitch}} = C_{gd}(V_H - V_L)/\Delta T = C_{gd}K \quad (5.2) \]

where \( C_{gd} \) is the gate to drain capacitance, \( V_H \) is the Higher level of voltage swing, \( V_L \) is the Lower level of voltage swing and \( K \) is the constant.

Thus the equation reveals an interesting property that, the amount of glitch current gets larger with increasing \( C_{gd} \) capacitance and fast transition. The amount of Glitch current can be as large as the CP current or even larger than it but owing in the opposite direction. As a result, charge injection in Charge Pump is a serious problem that should be taken care carefully.
5.3.2 Glitch Suppression

High speed glitches mainly originate from the Charge Sharing effect. There are several techniques for charge injection cancellation. In this work, transmission gates are used for the cancellation of injected charges.

The method to lowering the effect of charge injection incorporates both pMOS and nMOS devices such that, the opposite packets injected by the two cancel each other as shown in below Figure 5.1

\[
W_N L_N \ C_{ox}(V_{ck} - V_{in} - V_{thn}) = W_P L_P \ C_{ox}(V_{ck} - V_{in} - V_{thp})
\]  \hspace{1cm} (5.3)

where \( W_N \), \( L_N \) and \( W_P \), \( L_P \) are the width and Length of nMOS and pMOS respectively. Also, \( V_{thn} \) and \( V_{thp} \) are thevenin voltage of nMOS and pMOS and \( V_{in} \) and \( C_{ox} \) are the input voltage and oxide layer capacitance respectively.

Figure 5.1 Use of Complementary Switches to Reduce Charge Injection

For \( \Delta q_1 \) to cancel \( \Delta q_2 \), we have,
From Equation (5.3), it is seen that, cancellation of charge depends on the accuracy in device sizes, $C_{ox}$ and the threshold voltages of pMOS and nMOS devices.

### 5.3.3 Charge Sharing

Consider the circuit shown in the Figure 5.2, during the precharge phase, the output node is precharged to $V_{DD}$. Assume that all inputs are set to 0 during precharge and that the capacitance $C_a$ is discharged. Assume further that, input B remains at 0 during evaluation, while input A makes a $0 \rightarrow 1$ transition, turning transistor $M_a$ ON. The charge stored originally on capacitor $C_L$ is redistributed over $C_L$ and $C_a$. This causes a drop in the output voltage, which cannot be recovered due to the dynamic nature of the circuit.

![Figure 5.2 Charge Redistribution in MOS Switches](image)

The influence on the output voltage is readily calculated. Under the above assumptions, the following initial conditions are valid: $V_{out}(t = 0) = V_{DD}$ and $V_X(t = 0) = 0$. Two possible scenarios must be considered:
1. $\Delta V_{out} < V_{Tn}$ — In this case, the final value of $V_X$ equals $V_{DD} - V_{Tn}(V_X)$. Charge conservation yields

$$C_L V_{DD} = C_L V_{out}(t) + C_a [(V_{DD} - V_{Tn}(V_X)]$$

(5.4)

Or

$$\Delta V_{out} = V_{out}(t) - V_{DD} = -C_a/C_L [V_{DD} - V_{Tn}(V_X)]$$

(5.5)

2. $\Delta V_{out} > V_{Tn}$ — $V_{out}$ and $V_X$ reach the same value:

$$\Delta V_{out} = -V_{DD} \left( \frac{C_a}{C_a + C_L} \right)$$

(5.6)

Which of the above scenarios is valid is determined by the capacitance ratio. The boundary condition between the two cases is determined by setting $\Delta V_{out}$ equal to $V_{Tn}$

$$\frac{C_a}{C_L} = \frac{V_{Tn}}{V_{DD} - V_{Tn}}$$

(5.7)

Overall, it is desirable to keep the value of $\Delta V_{out}$ below $|V_{Tn}|$.

### 5.4 DESIGN OF MODIFIED CP CIRCUIT

To solve the charge sharing problem, in order to reduce high speed glitches, a modified CP circuit with matched pair of transmission gates is designed. In addition with an error amplifier and reference current source are used to provide the improved characteristic in current matching and reduce the PLL’s phase noise. Simultaneously, the Charge Sharing is effectively restrained by the use of charge removal transistors. So the circuit possesses good current match and high working speed. Current mirrors are then used to
copy currents from the bias cell, and a cascode is used at the output node to get high output impedance in order to reduce current mismatch.

Gain-boosting technique is applied as shown in Figure 5.3 high output impedance is achieved without adding more cascode devices (Behzad Razavi 2002).

![Figure 5.3 Modified Charge Pump](image)

### 5.4.1 Working of Modified CP Circuit

The modified CP circuit greatly improves the circuit performance by enhancing the current match and lessening the Charge Sharing, and at the same time, possesses the characteristics of high operating speed. In Figure 5.3, the capacitances C1, C2 are used to fill the role of stabilizing the node E and F’s voltage, to avoid instantaneous grid voltage fluctuation of the current
source. The voltage $V_c$ in node C will change with $V_{ctrl}$ by inserting an error amplifier which has the gain high enough to make $V_c$ equal $V_{ctrl}$. Moreover, M11 is designed to be equal to M9, M8 to be equal to M10, M3 to be equal to M5, and M4 to be equal to M6. So that, the current $I_4 = I_3 = I_1$ when UP and DN signals are high, and $I_2 = I_1 = I_3$ when UP, DN signals are low.

Finally, the current $I_4$ equals to $I_2$, which leads up to the result of almost perfect drain-source current matching. M7 and M12 are named as charge eliminating transistor which are used to eliminate the spare charge stored at node A and B, when the UP and DN is held at low. Hence, the charge sharing problem is successfully restrained.

The Modified CP circuit which uses error amplifier and reference current source to get good match characteristic and the use of charge removal transistor is to restrain the charge sharing. All the design has been simulated with Spectre tools.

A modification for the gain-boosting CP is illustrated in Figure 5.3 in which the CLM problem is solved as well as current mismatch. A low voltage cascode current mirror is used to copy $I_{UP}$ and $I_{DN}$ from a single current source to ensure that, both currents are to be equal. The low-voltage cascode current mirror is chosen because it provides high output impedance and Low CLM mismatch (Behzad Razavi 2002).

As shown in Figure 5.3, the Up and Down controlled switches have been embedded in the low-voltage cascode current mirrors, where M7 and M8 are the Up and Down controlled switches respectively. The transistors M9 - M16 are the low voltage cascode current mirror transistors. Finally, M17 and M18 are the reference current generators. When Up and down signals at
lock, the bias voltage of the low-voltage cascode current mirrors is chosen to be GND for the pMOS switched mirror, and $V_{DD}$ for the nMOS switched mirror. This provides better matching.

Transistors T1-T8 is matched transmission gates which are used to suppress the high speed glitches. After adding the modified switches, the high speed glitches are almost completely eliminated from the output current. Since pMOs and nMOS transistors in transmission gates are perfectly matched.

The output impedance, $R_{out}$, is higher than that given in Equation (3.5), since there is another cascode transistor, $R_{out}$ is given by

$$R_{out1} = \{[1+(g_{m1} + g_{mb1})r_{o1}]r_{o2}+r_{o1}\} \parallel \{[1+(g_{m3} + g_{mb3})r_{o3}]r_{o4}+r_{o3}\}$$  \hspace{1cm} (5.8)

$$\approx [1 + (g_{m1} + g_{mb1})r_{o1}]r_{o2} + r_{o1}$$  \hspace{1cm} (5.9)

where $R_{out1}$ is seen from the positive terminal of the opamp circuit.

$$R_{out2} = \{1 + (g_{m13} + g_{mb13})r_{o13}r_{o14} + r_{o13}\} \parallel \{1 + (g_{m15} + g_{mb16})r_{o15}r_{o16} + r_{o15}\}$$  \hspace{1cm} (5.10)

$$\approx 1 + (g_{m13} + g_{mb13})r_{o13}r_{o14} + r_{o13}$$  \hspace{1cm} (5.11)

where $R_{out2}$ is seen from the negative terminal of the opamp circuit.

Hence from Equations (5.9) and (5.11), it is seen that the output impedance is increased by a factor of $\{[1+(g_{m1} + g_{mb1})r_{o1}]r_{o2} + r_{o1}\}$ and $\{1 + (g_{m13} + g_{mb13})r_{o13}r_{o14} + r_{o13}\}$. This value is large and therefore, large length transistors are not needed for having high output impedance.
With reference to the Charge Sharing problem, the concept which is discussed in section 5.3.3, for the Modified CP circuit is mentioned below.

where at node B,

Letting the node capacitance be \( C_b \). So, the Voltage variation \( \Delta V_{\text{out}} \) at

\[
\text{Node } 'c' = -V_{dd} \frac{C_b}{(C_b+C_L)} \tag{5.11}
\]

and

\[
\frac{C_b}{C_L} = \frac{V_{tn3}}{V_{DD} - V_{tn3}} \tag{5.12}
\]

Hence, the design is made as per the Equations (5.11) and (5.12), the high speed glitch voltage are minimized at node ‘c’.

The same argument can be done for all cascade node capacitance and thereby reducing the glitches voltage at the node of all cascade points.

**5.5 SIMULATION RESULTS**

The Modified CP circuit at 1.8V power source is simulated with Spectre tools. Figure 5.4 shows the simulation results of CP charge circuit. Figures 5.5-5.8 shows the stability, gain of VCO output and the CP current with reference and feedback signal. The graph has been plotted for both conventional and CP with error amplifier PLL.

Figures 5.9 and 5.10 show the Phase Locking of PLL for conventional and modified CPPLL. The modified gain-boosting CP is designed using 1.8V CMOS transistors, good current matching is observed in
addition to a wide compliance voltage range of 0.1-1.7 V, which relaxes the VCO design. The maximum value for the current mismatch is 0.08 % which is less than 1%.

Figure 5.4 $I_{UP}$ and $I_{DOWN}$ Currents Plots

Figure 5.5 VCO Control Voltage when Reference Signal Leads Feedback Signal (Conventional Charge Pump PLL)
Figure 5.6 VCO Control Voltage when Reference Signal Leads Feedback Signal (Proposed Charge Pump PLL)

Figure 5.7 VCO Control Voltage when Reference Signal and Feedback Signal Phase and Frequencies are Equal (Conventional Charge Pump PLL)
Figure 5.8  VCO Control Voltage when Reference Signal and Feedback Signal Phase and Frequencies are Equal (Proposed Charge Pump PLL)

PHASE LOCKING OF PLL WITH GLITCHES

Figure 5.9  PLL Final Output with Glitches
MODIFIED STRUCTURE OUTPUT

Figure 5.10 Phase Locking of PLL

Since, the control signal remains constant it shows that the PLL has been locked properly for the incoming signal and there is no jitter in the output.

5.6 RESULTS AND DISCUSSIONS

By using the gain-boosting and low-voltage cascode current mirror, a high-performance low-mismatch CP is achieved. Mismatch between the two current sources of the CP is 0.08% for typical Conditions and 1% over all process variations. Moreover, a very wide output compliance voltage range is obtained for 1.8-V supply using 180-nm technology.
5.7 CONCLUSION

A gain-boosting and low-voltage cascode current mirror, a high-performance low-mismatch CP is designed and simulated for its performance. The simulation result shows that the mismatch between the two current sources of the CP is 0.08% for typical Conditions and 1% over all process variations.