8.1 SUMMARY

The deep submicron technologies are challenging test in a number of areas. The fabrication cost of transistors continues to reduce while the cost of testing is not scaling. Geometries shrink while the defect sizes do not shrink in proportion. The increase in wiring levels demands new fault models. Many of the design problems due to deep submicron technology which include distributed delay variations, crosstalk induced delay and logic errors, excessive voltage drop and swing on power nets have become test problems as well. The problem of test generation due to this deep submicron parametric variation belongs to the class of Non deterministic Polynomial (NP) complete problems and it is becoming more complex as complexity of integrated circuit increases. Of the various noise sources signal integrity problems due to increasing cross coupling will have significant adverse effect on the proper functioning and performance of VLSI systems. Development of efficient test generation methodologies for crosstalk delay faults has been an active area of research.

Chapter 1 gives the test challenges in deep submicron technologies and the necessity for test generation for crosstalk faults. In chapter 2 the review of the various crosstalk fault models and test generation algorithms for crosstalk delay faults are discussed.
The number of all possible pairs of crosstalk faults is very large and impossible to test. Hence in Chapter 3, static timing analysis is performed to obtain a reduced list of crosstalk delay faults. A modified FAN based deterministic algorithm is proposed for generating tests for crosstalk delay faults. Experimental results on ISCAS’85 combinational circuits, enhanced scan version of ISCAS’89 sequential circuits and ITC’99 benchmark circuits demonstrate that modified FAN based ATPG gives better results compared to modified PODEM based ATPG. The results obtained using modified FAN based ATPG gives a better fault coverage with reduced number of transitions for almost all the benchmarks compared to results obtained using modified PODEM based ATPG. The CPU execution time of modified FAN based ATPG is also less compared to modified PODEM based ATPG.

Evolutionary algorithms have been investigated as an efficient approach for test generation, as they mimic nature’s evolutionary principles to drive its search towards an optimal solution faster. In chapter 4 Genetic Algorithm is used for test generation of crosstalk delay faults. Tests are generated for ISCAS’85 combinational circuits, enhanced scan version of ISCAS’89 sequential circuits and ITC’99 benchmark circuits. A crosstalk delay fault simulator is used to validate the test patterns generated. Two versions of the crosstalk delay fault simulators are developed. In the first version, gates are assumed to have unit delay and the activated victim is given a delay of one unit. In the second version, gates are assigned a rise/fall delay and activated victim is given a calculated delay. The delay is calculated from coupling capacitance and resistance value derived from 45nm Nangate generic open cell library. Experimental results for four crossover operators namely one-point crossover, two-point crossover, uniform crossover and weight based crossover is detailed. Comparison of the results with modified FAN based ATPG indicate that the GA based ATPG gives a better fault coverage in reduced CPU time for most of the benchmark circuits.
Most of the real world problems involve one or more objectives that are to be maximized or minimized simultaneously. The presence of the conflicting objectives is natural in many test problems and makes the optimization NP hard. The multi-objective optimization techniques are used for optimizing multiple objectives simultaneously that resorts to a number of trade-off optimal solutions called pareto-optimal solutions. Chapter 5 proposes two multi-objective genetic algorithms namely Weighted Sum Genetic Algorithm, Elitist Non-dominated sorting Genetic Algorithm and Elitist Non-dominated sorting Genetic Algorithm with redundancy for test generation of crosstalk delay faults. Tests are generated for ISCAS’85 combinational circuits, enhanced scan version of ISCAS’89 sequential circuits and ITC’99 benchmark circuits. Experimental results for four crossover operators namely one-point crossover, two-point crossover, uniform crossover and weight based crossover is given. Experimental results indicate that ENGA based ATPG with redundancy gives a better fault coverage with reduced number of transitions in reduced CPU time for most of the benchmark circuits compared to WSGA based ATPG.

The accuracy of the crosstalk delay fault simulator depends on the delay models used in the simulation. As design trends move towards nanometer technologies, more number of new parameters affects the delay of the component. Fuzzy delay models are ideal for modeling the uncertainty found in the design and manufacturing steps. In chapter 6, a crosstalk delay fault simulator based on fuzzy delay model is developed for asynchronous sequential circuits. The fault simulator based on fuzzy delay detects unstable states, oscillations and non-confluence of settling states in asynchronous circuits. Random test patterns are validated using unit delay, rise/fall delay and fuzzy delay simulator. Experimental results for SIS benchmark circuits demonstrate the efficiency of the fuzzy delay simulator in comparison to the unit delay and rise/fall delay simulation. The delay for each element is
derived using a 45nm Nangate generic open cell library. The test sequences that cause non-confluence of settling states in asynchronous circuits are identified and invalidated by the fuzzy delay simulator.

In chapter 7, ATPG algorithms in GA, WSGA and ENGA framework is formulated and tested for asynchronous sequential circuits. Results on the SIS benchmark circuits indicate good quality tests in comparison to the random test vectors. A crosstalk delay fault simulator based on fuzzy delay model is used to find the fitness function. Test generator based on ENGA with redundancy reduces the number of transitions with a slight decrease in fault coverage compared to WSGA based ATPG.

8.2 SUGGESTIONS FOR FUTURE RESEARCH

- GA is a powerful search technique that is used to solve complex optimization problems. Optimization refers to finding one or more feasible solutions which correspond to extreme values of one or more objectives (Deb 2002). Multi-objective genetic algorithm is used for simultaneously optimizing several objectives. The multi-objective genetic algorithms discussed in this thesis are used for optimizing two objectives namely the fault coverage and the number of transitions. These multi-objective genetic algorithms can be extended for optimizing more number of objectives namely area and execution time simultaneously.

- The accuracy of timing verification depends on the proper modeling of the gate delays. With the advent of deep submicron technology more parameters affect the delay of the gates. The fuzzy delay model can be used for identifying the critical paths in static timing analysis of VLSI circuits.
Uncertainty implicit in the design and manufacturing flow is handled effectively by this delay model.

- The execution time for serial crosstalk delay fault simulator for larger benchmark circuits is high. CPU time can be improved by using parallel or concurrent crosstalk fault simulator. Parallel implementations can potentially provide significant speedups while retaining good quality results, (Knysh and Kureichik 2010, Klenke et al 1992). The implementation of event driven simulation in parallel environment has been successful (Banerjee 1994). Further the crosstalk fault model can be improved to include resistive bridging faults.
- If layout information is available, the information can be used in static timing analysis to further reduce the set of target crosstalk delay faults.