ABSTRACT

The design automation of complex digital circuits in industry required reduced power consumption and increased throughput. In today’s industry, the electronic equipment such as the microelectronic chip, present in systems ranges variably from cell phones to desktop computers to supercomputers which operate in basically the similar way. A clock that is distributed globally synchronizes the operation of their millions of internal components. Increasingly, higher speed, greater functionality, and better energy efficiency chips can be achieved only by this global clocking which is now becoming a critical design challenge for the designers. Asynchronous or “clockless” design is the apt alternative which precludes the need for global synchronization as a replacement, operations of components are concurrent and synchronize locally based on necessity. This destined work predominantly is dealt with the usage of asynchronous logic which is a novel approach in order to achieve low power design. Mainly in the chosen Sequential circuits, this work aims to make the design and performance analyses of circuits.

Both dual-rail as well as single-rail dynamic data paths are targeted in this design. The new control structures and protocols are employed by the pipelines which aim at the reduction of handshaking delay, which is the paramount impediment to achieve high throughput in asynchronous pipelines.

An increasingly practical alternative is the asynchronous circuits, load, delay and the performance penalty related with supporting
communication between varied clocks domains are also to be considered. There is no common or discrete time in asynchronous which is a binary signal. In order to perform the needed synchronization, communication and sequencing of operations, the circuits employ handshaking between their components. This is the major difference which gives asynchronous circuit’s inherent properties in the areas of reduced power consumption, advanced operating speed and robustness toward at times of variation in supply voltage, temperature and fabrication process parameters, improved modularity, reduced emission of electromagnetic noise, no clock distribution and lack of clock skew problems. One of the most promising directions is the low power consumptions and one of the best examples is the design reported in this study. For some standard logic circuits and medium scale integration (MSI) circuits, this work is a good demonstration of the design of efficient asynchronous pipelines. For different standard logics and MSI circuits, the performance analyses of varied templates are designed, to enhance circuits in accordance with area and power and at the same time maintaining the robustness.

A matrix - vector multiplication core of discrete cosine transforms (DCT) was developed in order to quantify certain advantages by employing nonlinear pipelined templates. 35% higher average throughput is obtained in this proposed asynchronous design when compared with conventional synchronous design with negligible energy overhead used.

The power expended by the synchronous and asynchronous display controllers was being measured, where about 22% less power is consumed in
the asynchronous design when compared to its synchronous counterpart. By reducing the dependency of the clock signal in the design, power can be reduced only by choosing asynchronous logic.

Asynchronous design is increasingly becoming an attractive alternative to synchronous design due to its potential for high performance, low power, and acclimatization to process variations and reduced EMI noise. Nevertheless in asynchronous design there is a need to reduce the overwhelming design style which can be achieved by developing circuits which can easily be verified with mature CAD flows in order to support them. When this prospect is taken into consideration, asynchronous circuits can toughly compete with existing synchronous designs. A template based methodology is proposed in this thesis which facilitates standard cell based design which can easily be proved.

The low latency and high performance benefits of reduced stack pre-charged half buffer (RSPCHB) compared to other asynchronous and synchronous communication protocols by relating their throughput, energy, transistor area, latency and high bandwidth is clearly demonstrated which is the need of the industry.