CHAPTER 7

CONCLUSION

7.1 SUMMARY

The contributions made in this research work are summarized and below. By using asynchronous logic, a novel approach of low power design can be achieved. Due to the emergence of portable systems and their applications, low power design has achieved its pinnacle of importance. There are varied factors like thermal considerations, reliability, and environmental concerns, which made the designers to think and enforce their thought to strenuously look into power reduction techniques even in the preliminary design phase.

The clock signal and clock distribution network consumes about 55% of the overall chip power in synchronous circuits. The main source of power consumption in digital system is the dynamic capacitive switching power. Specifically in high-speed circuits, as the clock frequency increases, the capacitive switching power correspondingly increases consistently.

The clock signal is not completely removed from the design in asynchronous logic. Considering the extensive design complexity of purely asynchronous designs, the best option chosen is GALS design style. Asynchronous systems aim at reducing noise, power consumption, and EMI
unlike clocked circuits. An implicit idle behavior is obviously noticed since they switch only while useful work is being done. Insensitivity in delay and tolerant to power supply variations are noticeable features in asynchronous circuits. The absence of global clock which coordinates the progress of events is the key feature of asynchronous design unlike the synchronous model. In order to trigger the next stage once the current stage is completed, pipeline controller logic is required.

The First trial was done with RS latches that have consumption of few milli watts. RS latch was replaced with D-Latch, this has given an improvement. These two approaches are based on conventional pipelined approach with GALS. In this proposed work, this was replaced with protocol based pipelining with GALS.

So initially it was tested with a Adder circuit which has given dramatic changes in power consumptions of MicroWatts level with improvement in throughput, complexity, latency etc. A trial has been carried out with three approaches PCHB,PCFB and RSPCHB, The output is that this RSPCHB has given the least result, so based on this RSPCHB approach proposed for given for MSI based multiplexer circuit and it is extended for multiplier. In all these circuits achieved, very low energy consumption to level of microwatts using RSPCHB approach and high throughput better latency, improved number of transistor area, high bandwidths with less delay.
7.2 FUTURE SCOPE OF THE WORK

The asynchronous pipeline template Reduced Stack Pre-Charged Half Buffer (RSPCHB) tried with 33nm, same approach can be extended for high complexity VLSI circuits and Ultra LSI circuits with dimension less than 15 nm.

The proposed methods in this thesis can be extended for investigations in the following related areas.

8. Transformations for the synthesis and optimization of asynchronous distributed control (Theobald et al. 2001)