Chapter 5

SWITCHED MULTISTAGE VECTOR QUANTIZER

5.1 SWITCHED MULTISTAGE VECTOR QUANTIZATION

Switched Multistage Vector Quantization (SWMSVQ) technique is the proposed hybrid vector quantization technique which is used to improve the performance of a Multistage Vector Quantization technique. Switched Multistage Vector Quantization technique is a hybrid of Switch Vector Quantization and Multistage Vector Quantization techniques. Switched Multistage Vector Quantization can be implemented in two ways. They are soft decision and hard decision schemes. The concept of hard decision and soft decision schemes is similar to the concept discussed in Switched Split Vector Quantization [54 and in chapter 4]. In Switched Multistage Vector Quantization using hard decision scheme the input vector at each stage is quantized in the selected codebook based on the nearest neighbor criterion between the input vector and the centroids of the initial codebook. In this thesis the performance of a 2-switch 3-stage Switched Multistage Vector Quantization technique using hard decision scheme is examined against the existing vector quantization techniques [86-88]. The generation of codebooks at different stages of Switched Multistage Vector Quantizer is similar to the generation of codebooks at different stages of Multistage Vector Quantizer. The block diagram of a Switch Vector Quantizer is shown in Fig 5.1. It is
similar to Switched Split Vector Quantizer except that there are no splits in a quantizer at each switch.

Fig 5.1 Block diagram of Switch Vector Quantizer

In Fig 5.1 ‘s’ is the input vector to be quantized and $C_i$ corresponds to the centroid or codeword of an initial codebook and $i = 1, 2, \ldots$, $m$ corresponds to the number of switching directions. The block diagram of an $m \times P$ Switched Multistage Vector Quantizer is shown in Fig 5.2 where ‘m’ corresponds to the number of switching directions and ‘P’ corresponds to the number of stages.

In Switched Multistage Vector Quantizer the vector to be quantized is passed through different stages of Multi Stage Vector Quantizer for quantization at each stage as a Switch Vector Quantizer is adapted the vector is quantized by switching among the quantizers connected in parallel at each stage. The input vector ‘s’ to be quantized is passed
through the first stage of the vector quantizer so as to obtain the quantized version of the input vector ‘\( \hat{s}_1 \)’. The quantization error resulting at the first stage of quantization be \( e_1 = s - \hat{s}_1 \) and is given as an input to the second stage to obtain the quantized version of the error vector \( \hat{e}_1 = Q[e_1] \). Likewise the quantization error at the second stage is given as an input to the third stage and this process continues for the required number of stages. Finally the decoder takes the indices, \( I_i \), from each stage and adds them so as to obtain the quantized version of the input vector ‘\( s \)’ given by \( \hat{s} = Q[s] + Q[e_1] + \ldots \) where \( Q[s] \) is the quantized version of the input vector at the first stage, \( Q[e_1] \) is the quantized version of the error vector at the second stage and so on.

(I, denotes the index of the quantizer)

Fig 5.2 Block diagram of Switched Multistage Vector Quantizer
In Switched Multistage Vector Quantization the number of stages and switches must be limited as the number of bits available at each stage of the quantizer is less.

The equations of computational complexity and memory requirements for Switched Multistage Vector Quantizer are derived from the complexity and memory requirement equations of a Switch Vector Quantizer and Multistage Vector Quantizer by combining them.

The computational complexity of Switch Vector Quantizer is given by equation (5.1)

\[
\text{Complexity}_{\text{SWITCH}} = 4n^2 b_m - 1
\]  

(5.1)

where

\( n \) is the dimension of the vector

\( m = 2^m \) is the number of switching directions

\( b_m \) is the number of bits allocated to the switch vector quantizer

The computational complexity of a Multistage Vector Quantizer is given by equation (5.2)

\[
\text{Complexity}_{\text{MSVQ}} = \sum_{j=1}^{p} \left( 4n^2 b_j - 1 \right)
\]

(5.2)

where

\( P \) is the number of stages

\( b_j \) is the number of bits allocated to the \( j^{\text{th}} \) stage
The computational complexity of Switched Multistage Vector Quantization technique using hard decision scheme is given by equation (5.3)

\[
\text{Complexity}_{\text{SWMSVQ HARD}} = \sum_{j=1}^{P} \left( 4n^2 b^m m - 1 + 4n^2 b^j - 1 \right)
\]

\[
= \sum_{j=1}^{P} \left( 4n \left( 2^b m + 2^b j \right) - 2 \right)
\] (5.3)

In SWMSVQ using soft decision scheme quantization is done using all the codebooks connected in parallel at each stage. So a summation term with limits from 1 to \( P_l \) is included in equation (5.4).

The computational complexity of Switched Multistage Vector Quantization technique using soft decision scheme is given by equation (5.4)

\[
\text{Complexity}_{\text{SWMSVQ SOFT}} = \sum_{j=1}^{P} \left( 4n^2 b^m m - 1 + \sum_{k=1}^{P_l} \sum_{j=1}^{b_j} b^k - 1 \right)
\]

(5.4)

where

- \( P_l \) is the number of codebooks connected in parallel at each stage
- \( b_{jk} \) is the number of bits allocated to the \( j^{\text{th}} \) stage \( k^{\text{th}} \) codebook

The Memory requirements of a Multistage Vector Quantizer is given by equation (5.5)

\[
\text{Memory}_{\text{MSVQ}} = \sum_{j=1}^{P} \frac{n^2 b^j}{j}
\] (5.5)
The Memory requirements of Switch Vector Quantizer is given by equation (5.6)

\[ \text{Memory}_{\text{SWITCH}} = n^2 b^m \]  

The Memory requirements of Switched Multistage Vector Quantization technique using hard decision scheme is given by equation (5.7)

\[ \text{Memory}_{\text{SWMSVQ HARD}} = \sum_{j=1}^{P} \left( n^2 b^m + n^2 j \right) \]

\[ = \sum_{j=1}^{P} n \left( 2^b m + 2^b j \right) \]  

The Memory requirements of Switched Multistage Vector Quantization technique using soft decision scheme is given by equation (5.8)

\[ \text{Memory}_{\text{SWMSVQ SOFT}} = \sum_{j=1}^{P} \left( n^2 b^m + \frac{P}{\sum_{k=1}^{P} n^2} b^j \right) \]  

The concept of equation (5.4) applies to equation (5.8) so a summation term with limits from 1 to P_l is included in equation (5.8).

**5.2 RESULTS AND DISCUSSION**

This section deals with comparing the results of 2-switch 3-stage Switched Multistage Vector Quantization using hard decision scheme with 3-part Split Vector Quantizer, 3-stage Multistage Vector Quantizer, 3-part 3-stage Split-Multistage Vector Quantizer, 2-switch
3-part Switched Split Vector Quantizer using hard decision scheme techniques in terms of spectral distortion, computational complexity and memory requirements (ROM) at 24, 23, 22, 21, 20 bits per frame. The spectral distortion is measured in decibels (dB), computational complexity in kilo flops per frame, memory requirements in Floats (1 Float = 4 Bytes and 1 Byte = 8 bits). The frames having average spectral distortion greater than 1 dB are considered as outlier frames, there must be no outlier frames having spectral distortion greater than 4 dB and the number of outlier frames between 2 to 4 dB must be less than 2%.

Table 5.1 Spectral distortion, Complexity and Memory requirements for a 2-switch 3-stage Switched Multistage Vector Quantizer using hard decision scheme

<table>
<thead>
<tr>
<th>Bits / frame</th>
<th>SD(dB)</th>
<th>Percentage of outliers</th>
<th>Complexity (Kflops/frame)</th>
<th>ROM (Floats)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>2-4 dB</td>
<td>&gt;4dB</td>
<td></td>
</tr>
<tr>
<td>24(1+7+1+7+1+7)</td>
<td>0.12007013</td>
<td>0</td>
<td>0</td>
<td>15.594</td>
</tr>
<tr>
<td>23(1+7+1+7+1+6)</td>
<td>0.12677232</td>
<td>0</td>
<td>0</td>
<td>13.034</td>
</tr>
<tr>
<td>22(1+7+1+6+1+6)</td>
<td>0.13356720</td>
<td>0</td>
<td>0</td>
<td>10.474</td>
</tr>
<tr>
<td>21(1+6+1+6+1+6)</td>
<td>0.13804648</td>
<td>0</td>
<td>0</td>
<td>7.914</td>
</tr>
<tr>
<td>20(1+6+1+6+1+5)</td>
<td>0.14132517</td>
<td>0</td>
<td>0</td>
<td>6.634</td>
</tr>
</tbody>
</table>

Table 5.1 shows the spectral distortion measured in decibels, computational complexity measured in kilo flops per frame and memory requirements measured in Floats at various bit-rates for a 2-switch 3-stage Switched Multistage Vector Quantizer using hard
decision scheme. The numbers in the brackets of $24(1+7+1+7+1+7)$ denote the bits allocated to each stage and to the switches at each stage of a 3-stage 2-switch Switched Multistage Vector Quantizer using hard decision scheme. The 1$^{st}$, 3$^{rd}$ and 5$^{th}$ bits in the brackets are the switch bits and the remaining bits are allocated to the quantizer at each stage. The allocation of the bits to the switches at each stage is same as in Switched Split Vector Quantizer and the allocation of the bits to the stages is same as in Multistage Vector Quantizer (as explained in results of chapter 4). In this technique two quantizers are connected in parallel at each stage and the bits are allocated to the quantizer selected.

![Graph](image)

**Fig 5.3** Spectral Distortion for SVQ, MSVQ, S-MSVQ, SSVQ hard decision scheme and SWMSVQ hard decision scheme
The Fig 5.3 gives a plot of the spectral distortion of 3-part Split Vector Quantizer, 3-stage Multistage Vector Quantizer, 3-part 3-stage Split-Multistage Vector Quantizer, 2-switch 3-part Switched Split Vector Quantizer using hard decision scheme, and 3-stage 2-switch Switched Multistage Vector Quantizer using hard decision scheme for 24 to 20 bits per frame. The spectral distortion is measured in dB.

![Complexity for SVQ, MSVQ, S-MSVQ, SSVQ hard decision scheme, and SWMSVQ hard decision scheme](image)

The Fig 5.4 gives a plot of the computational complexity of SVQ, MSVQ, S-MSVQ, SSVQ using hard decision scheme, and SWMSVQ using hard decision scheme for 24 to 9 bits per frame. The computational complexity is measured in kilo flops per frame.
The Fig 5.5 gives a plot of the memory requirements of SVQ, MSVQ, S-MSVQ, SSVQ using hard decision scheme, and SWMSVQ using hard decision scheme for 24 to 9 bits per frame. The memory requirements is measured in Floats (1 Float = 4 Bytes and 1 Byte = 8 bits).

Fig 5.5 Memory requirements for SVQ, MSVQ, S-MSVQ, SSVQ hard decision scheme, and SWMSVQ hard decision scheme
Fig 5.6  Number of outlier frames having spectral distortion between 2 to 4 dB for SVQ, MSVQ, S-MSVQ, SSVQ hard decision scheme and SWMSVQ hard decision scheme

Fig 5.6 gives a plot of the number of outlier frames lying between 2 and 4 dB. In practice for transparent quantization the number of outlier frames lying between 2 to 4 db must be less than 2%. But from Fig 5.6 it can be observed that the number of outlier frames is zero. So one can say the vector quantization is done in a good manner and transparency in quantization is achieved.
Fig 5.7 Number of outlier frames having spectral distortion greater than 4 dB for SVQ, MSVQ, S-MSVQ, SSVQ, hard decision scheme and SWMSVQ hard decision scheme.

Fig 5.7 gives a plot of the number of outlier frames greater than 4 dB. In practice for transparent quantization the number of outlier frames greater than 4 dB must zero. From Fig 5.7 it can be observed that the number of outlier frames is zero. So transparency in quantization is achieved.

From Tables 4.3, 4.5, 4.7, 4.8 & 5.1 and from Figs 5.3 to 5.5 it is concluded that 2-switch 3-stage Switched Multistage Vector Quantizer using hard decision scheme is having less spectral distortion compared to 3-part Split Vector Quantizer, 3-part 3-stage Split-Multistage Vector Quantizer, 2-switch 3-part Switched Split Vector
Quantizer using hard decision scheme and comparable spectral distortion when compared to 3-stage Multistage Vector Quantizer. Its computational complexity is less compared to 3-stage Multistage Vector Quantizer and high compared to 3-part Split Vector Quantizer, 3-part 3-stage Split-Multistage Vector Quantizer, 2-switch 3-part Switched Split Vector Quantizer using hard decision scheme, its memory requirement is less compared to 3-stage Multistage Vector Quantizer, 2-switch 3-part Switched Split Vector Quantizer using hard decision scheme and is high compared to 3-part Split Vector Quantizer, and 3-part 3-stage Split-Multistage Vector Quantizer. The increase in computational complexity and memory requirements is due to quantization of vectors of larger dimensions.

5.3 CONCLUSION

From results it is concluded that 2-switch 3-stage Switched Multistage Vector Quantizer using hard decision scheme is having better performance compared to Multistage Vector Quantizer in terms of spectral distortion, complexity and memory requirements. In terms of memory requirement it is showing better performance compared to 3-stage Multistage Vector Quantizer and 2-switch 3-part Switched Split Vector Quantizer using hard decision scheme. So it can be concluded that 2-switch 3-stage Switched Multistage Vector Quantizer using hard decision scheme has better performance compared to 3-stage Multistage Vector Quantizer. This increase in performance is due to the switch adopted at each stage of the vector quantizer.