Abstract

Usage of inverter has become inevitable in every power range of application. 2-level inverters are popularly used for low and medium power range of applications. But for medium-high and high power applications these 2-level inverters fail due to increased switching stress and THD in the output. This has given rise to introduction of multilevel inverters. In these inverters output is realised as incremental steps of supply voltage and each switch needs to withstand a single step of voltage. This reduces the switching stress and improves the THD. The popular topology among these inverters is Diode clamped multilevel inverters (DCMLI). This inverter envisages the steps in output voltage by splitting the supply voltage into steps with the help of DC-bus capacitors. It is evident that capacitors need to share equal voltage to obtain uniform steps in the output voltage and thereby improved performance. But the voltage across capacitors depends upon load pf and modulation index. The unbalance in capacitors is the worst for unity pf and it decreases towards zero pf. This leads to a low frequency oscillation in three-level inverters. In five-level inverters the inner capacitors completely discharge and outer capacitors share the entire supply voltage equally. This reduces the five-level inverter output to three-level and in-turn increases the output voltage distortion, overburden the switches and the capacitors.

The existing techniques in the literature to balance capacitor voltages can be classified into Inherent and source side balance techniques. For three-level inverter there exists well established Inherent balancing techniques and they can be broadly classified as carrier based PWM, Space vector PWM and Hybrid of the two. The carrier based PWM technique fails at low modulation indices and SVPWM technique incurs more switching losses and is complex in implementation. The same techniques when applied to five-level inverter failed i.e. there exists no inherent PWM technique to solve the capacitor balance problem for DCMLI above five-level.

Consequently research focus was on the use of extra components at source side to balance capacitor voltages. Popular techniques are to use five-level back to back
connected converters, usage of DC-DC converters to feed each capacitor or to use separate DC sources instead of capacitors. All these techniques increased the no of components and consequently the cost of the converter.

Thereby the idea taken up for this thesis is to develop inherent PWM techniques to balance the capacitor voltages of five-level inverter or to reduce the no of components used at the source side to balance the capacitor voltages so that the cost reduces. The thesis proposes and evaluates four new modulation techniques of which two fall under inherent balancing techniques and the other two under source side balancing techniques. The inherent balancing techniques are Modified level shifted carrier PWM (MLSC PWM) and a Improved hybrid PWM. The source side PWM techniques are Source-side capacitance modulation technique (SCMT) and Error hysteresis switched inductor technique (EHS).

These techniques are evaluated in Matlab simulink environment and experimental set-up has been developed to test the techniques for three-level inverter.