Chapter 7

CONCLUSIONS AND OUTLOOKS FOR FUTURE WORK

7.1 Conclusions

Wide spread applications of wireless did not initially emerge and only came with the advent of the personnel cellular phones. Various basics services in the daily life utilize wireless systems operating 1 to 10 GHz bands to communicate important information quickly whether it is in a small office or building. These systems front-end modules such as low-noise amplifier (LNA), power amplifier (PA) and mixer need to perform better from point of view of noise (<3dB), gain (>15dB), linearity (IP3 >1dBm) and consume low power.

In this kind of applications, gate-underlap SOI appears to be strong contender compared to other device technologies. These devices have inherent advantages over bulk devices such as lower junction capacitance, no latchup and lower sensitivity to temperature variation. The SOI technology has been critically reviewed and various SOI MOSFETs structures and their operations have been included in this thesis. Some theoretical aspects of nano-scale FD-SOI MOSFETs such as mathematical expressions for natural length model, threshold voltage $V_{TH}$, drain-source current $I_{DS}$ and transconductance $g_m$ have been presented. Different existing fabrications processes were elaborated and industry perspectives of FD-SOI MOSFETs including the name of companies which are actively involved in development and implementation of this technology and their latest survey (year -2012) have been included.

In this work different nano-scale FD-SOI device design approaches such as thin body, graded channel, halo doped, multiple-gate and gate-underlap also known as source drain extension (SDE) have been explained. Among them, SDE has been studied extensively and found to be very effective new approach to combat SCEs and found its use for low power and high frequency applications.
The basic device physics involved in the designing of the SDE based approach has been discussed. Furthermore, the designed device has been authenticated through process parameters simulation using ATLAS TCAD from SILVACO and variations of $V_{TH}$ as well as $A_v$, $f_T$ and $f_{MAX}$ of the designed device has been carried out.

From the results, it has been observed that with this optimal spacer ($s \approx 0.8 \times L_G$) reduces feedback capacitance sufficiently to enhance intrinsic gain $A_v$ as well as both $f_T$ and $f_{MAX}$ of the device. Gate-underlap MOSFETs operated at low current levels ($\approx 10 \mu A/\mu m$) gives peak value of product of $g_m/I_{DS}$ and $f_T$ i.e., $[(g_m/I_{DS}) \times f_T]$, which is particularly useful for low power analog/RF applications. Due to this both gain and speed of device has been improved.

The small-signal model of optimized underlap device has been developed by accurately accounted NQS effect. The validity of the model has been demonstrated by comparing Y-parameters generated through 2D ATLAS was found excellent matching (with an average error $\leq 5\%$) whereas results from PTM (QS) model and NQS model excluding extrinsic parasitic have significant difference $> 20\%$ and $\approx 22\%$, respectively. The simulated results in this work have been authenticated with limited experimental data which are available in the literature. The results presented in this work show attractive potentialities of gate-underlap technology for GHz range frequency applications (up to 20 GHz).

At circuit level the validity of the proposed NQS model for gate-underlap device has been verified by designing of cascode LNA operating at 5.8GHz. Using proposed FoM$_{LNA}$, it has been found that LNA design based on underlap gives significant (nearly six times) improvement compared to non-underlap (simulated using PTM model, $L_G = 130\ nm$). However, a comparison with limited measured data available for 180nm bulk, it was found that our design performance (in-terms of FoM$_{LNA}$) is nearly three times higher.

In addition, a dual-bands (with target bands of 2.4 GHz and 5.8GHz) cascode mixer has been designed using large-signal SOI-BSIM4 model by incorporating some of the extracted parameters such as $C_{gs}$, $C_{gd}$, $C_{ds}$, $R_{ge}$, $R_{sc}$ and $R_{de}$ of the designed device. It has found that at fixed $f_{IF}$ of 100 MHz, mixer has reasonable LO-to-RF isolation as LO and RF signals are fed from different ports in cascode mixer circuits. The performance of designed mixer in-terms of FoM$_{Mixer}$ is
Conclusions and Outlooks for Future Work

compared with measured results. It was found that FoM\textsubscript{mixer} of our design is higher with previous published non-underlap bulk results of FoM\textsubscript{mixer}.

For the wireless communication system linearity is also an important issue. Therefore, the linearity performance in-terms of (IP3) of cascode LNA has been investigated by varying process parameters such as s, T\textsubscript{si}, d and L\textsubscript{G} of the gate-underlap single and double gate devices for wireless LAN applications. The effect of parasitic is incorporated to investigate to examine their effects on IP3 and (FoM\textsubscript{LNA})\textsubscript{LARGE}. A detailed investigation using mixed mode simulation from ATLAS has been used to illustrate the linearity performance of cascode LNA using new engineered underlap devices. In the mixed mode simulations parasitic effects of contact resistance and overlap capacitance can be incorporated, which combines the merits of device and circuit both and particularly relevant when the frequency of operation is high and more than one transistors are connected. Valuable design insights to optimize the linearity performance of LNA using a new engineered underlap design have been given. The superior performance of LNA using optimal underlap design is due to combined effects of enhanced G and IP3 at low power consumption.

LNA linearity performance can be enhanced by use of an optimal gate underlap profile, which yields both higher gain and better linearity. The LNA input/output matching such as S\textsubscript{11}, S\textsubscript{22} and linearity parameters IP3 have been compared with the available experimental data of the bulk technology and found to be well conformity. The resultant enhancement in overall (FoM\textsubscript{LNA})\textsubscript{LARGE} is almost four times of magnitude when compared to SG-MOSFETs LNA and five times with experimental (FoM\textsubscript{LNA})\textsubscript{LARGE}. The performance enhancement predicted with an optimal DG-SOI LNA compares favourably with experimental results based on bulk technology. With optimized IP3, it has been found that with gate length scaling, LNA performance can continue to improve as long as contact resistance is kept low (R\textsubscript{con} = 2.5Ω).

As we have seen, wireless technologies require high performance transistors and low-loss passive devices. Therefore, it can be concluded that FD-SOI is one of the most promising solutions for low power GHz applications.
7.2 Outlooks for Future Works

A number of improvements in the presented SOI MOSFETs model are possible in this work in future. The first major improvement would be to investigate in detail the effects of body of SOI MOSFETs for RF performance of the transistor. The implementation of these effects in the new model is necessary to increase the accuracy of front-end block of transceiver.

The main purpose of this work was to demonstrate an integrated approach for designing low power GHz range transceiver front-end circuits by using underlap SOI MOSFETs. Traditionally, the gate oxide of a MOSFET has been considered as a perfect barrier for carriers allowing no current flow between the gate and silicon. As CMOS technology scales to smaller dimensions, the gate leakage current (i.e., Fowler-Nordheim tunnelling current and direct tunnelling current) is no longer ignored. How does the gate leakage has an impact of RF performance in gate-underlap SOI can be taken in future.

Scaling CMOS towards the 25nm channel length generation requires innovative device structures to circumvent barriers due to fundamental limitations of device physics in the conventional MOSFETs. These devices are back-gate FET, double-gate FET and FinFET. Fundamental issues for these structures such as the physics of carrier transport in very thin silicon channel need to be further understood.

In this work, only LNA and mixer blocks have been designed and discussed for wireless LAN application. In a wireless system, there are other components, which are critical for the system performance point of view, namely frequency synthesizer and power amplifier etc. Future, effort should be devoted to other blocks of wireless systems by applying similar design approach. A complete transceiver system designed under the same philosophy that interfaces with digital blocks and transmits-receives information would be the ultimate goal of this research and undoubtedly will demonstrate the suitability of the novel design approach presented in this work.