Chapter-2

Literature Review

In this chapter we review previous work which is based on the effect of performance parameters on SRAM cell. The research work has been done over the past several years to design a low power SRAM cell, which affects the other parameters like stability and speed.

2.1 SRAM Cell

Memory is an essential part of any electronic device. There are two types of memory SRAM and DRAM. SRAM is the static in nature, while DRAM is dynamic in nature. We can use both dynamic and static memory in electronic devices, but there is a cost difference between both of them. The structure of both dynamic and static RAM is different, but both can store only one bit information. Dynamic memory is having one capacitor and one transistor, instead of static memory is having a set of flip flop. But there is a drawback by using DRAM, to refresh this again and again due to capacitor [1].

SRAM cell structure consists of two inverters and two pass transistors. The inverters form the feedback loop and the feedback loop stabilizes the state of memory. The pass (access) transistor used for read and write operation to pass the value through/into bitline [2].

The basic SRAM cell consists of 6 transistors. The input of one inverter is a output of another inverter. During read operation the bitlines should be precharged and for write operation bitline passes the data into bistable circuitary, which forms by two inverters. In hold operation access transistors remains in OFF condition. A 6T CMOS SRAM cell is the most popular SRAM cell due to its superior robustness, low power and low-voltage operation [3].

2.2 Low Power Design

Power reduction is one of the most important design objectives. However, power cannot be reduced indefinitely without compromising with other parameters like cell area and speed of operation. Power dissipation in CMOS circuits can be categorized into two main components - dynamic and static power dissipation. Dynamic dissipation occurs due to switching transient current (referred to as short-circuit current) and charging and discharging of load capacitances
(referred to as capacitive switching current). Static dissipation is due to leakage currents drawn continuously from the power supply. There are various modes which contribute to leakage current, such as sub threshold leakage, reverse-biased PN junctions, drain-induced barrier lowering (DIBL), gate induced drain leakage, punch-through currents, gate oxide tunneling, and hot carrier effects. However, the main contributor of leakage is the sub-threshold leakage current [4].

### 2.3 Performance parameters of SRAM cell:

#### 1. Stability:

The fast growth of battery operated devices has made low power SRAM designs a necessity in recent years. The SRAM performance is limited by the cell stability during low power subthreshold operation. By adding extra transistor to the conventional 6T-cell, hold, read and write static noise margin (SNM) can be improved in the sub-threshold SRAM. Milad Zamani proposed a new 9T-cell SRAM that shows 80% and 50% improvement in read and write SNM respectively in comparison to the conventional 6T SRAM. Using stack transistors in the leakage current path, the new structure shows lower bitline leakage assisting the sense amplifier to easily read the bit line current [5]. Some observations of literature [5] are as follows:

- Many other effects such as process variation, bitline leakage and transistors mismatches challenge the proper operation of SRAMs that need a precise design. In sub-threshold region, conventional 6T-cell SRAM experiences poor read and write ability.
- Noise margin becomes worse at the time of read and write operations compared to hold operation which the internal feedback operates independent of other transistors
- 6T-cell shows poor stability in read SNM in subthreshold region.
- 6T, 9T and l0T are the different configurations designed to improve the stability
- In this work a novel scheme is proposed by authors that use dynamic mechanism for cutting the feedback to improve the write SNM and lowering the write time.
- The 6T cell fails to operate in subthreshold because of process variation and reduced voltage level.

Hailong Jiao et.al, Introduced a new asymmetrically ground-gated nine-transistor SRAM cell. The MTCMOS technique is used in their paper. The data stability is decreased as scale down
CMOS technology node. From the figure 2.1 shows that the data stability is higher at 90nm technology and degraded afterwards. 9T SRAM Cell for Reliable Ultralow-Power Applications and Solving Multi-Bit Soft-Error Issue Energetic cosmic rays or alpha-particles can induce soft error easily in subthreshold region compared to super threshold region, because the critical charge ($Q_c$) in subthreshold region is reduced with $V_{dd}$ scaling in nanometer regime. Hence, soft-error rate (SER) increases in subthreshold region compared to super-threshold region. Hazucha et al. in [6] reported that SER increases by 18% for each 10% reduction in $V_{dd}$. As the technology advances, the storage node capacitance of an SRAM cell is reduced [7].

This soft-error issue in multiple cells can be reduced by the use of bit-interleaving architecture and ECC (error checking and correction) technique. Bit-interleaving architecture is necessary because ECC technique cannot be applied to WL sharing architecture. When bit-interleaving architecture is used, stored data of most of the above mentioned cells' unselected cells are affected during write operation, which is called half-select issue. The proposed cell uses separate path for read operation. Therefore, it is read-disturb free during read operation [7].

![Figure 2.1 Read and Write static noise margin on different technology](image)

Ground gated circuits are also presented in their paper. In Conventional 6T SRAM cell for low power application centralized high threshold voltage (HVT) sleep transistor is used. This sleep transistor disconnected the memory array from the ground during sleep mode. An 8T SRAM cell is described in [9]. As compared to conventional 6T SRAM cell, two extra transistors added. By
adding these extra transistors read port is separated. The data stability of read operation is increased compared to the conventional 6T SRAM.

The structure of SRAM cell consists of nano-wire transistor. Simulations are done for static noise margin. The static noise margin evaluates on different operating voltages and threshold voltage. The performance benefits of undoped nanowire-transistor-based SRAM are measured in terms of the read stability for low voltage and low off leakage current operation [8]. Stability of the proposed SRAM has improved due to the reduction in swing voltage. Simulation results of power dissipation, access time, current leakage, stability and power delay product of the proposed SRAM cell have been determined and compared with those of some other existing models of SRAM cell. Simulation has been done in 45 nm CMOS environment [9].

The Word Line Voltage Margin (WLVM), defined as the maximum allowed word-line voltage drop during write operations, as a metric for the experimental characterization of write stability of SRAM cells. Their experimental measurement can be attained with minimal design modifications, while achieving good correlation with existing write ability metrics. To demonstrate its feasibility, the distribution of WLVM values has been measured in an SRAM prototype implemented in 65 nm CMOS technology. The dependence of the metric with the width of the transistors has been also analyzed, demonstrating their utility in post-process write stability [10].

The 12T SRAM bit cell is more robust in static and dynamic noise margin as compared to the conventional 6T SRAM cell, 8T SRAM bit cell and 10T SRAM cell from the Monte-Carlo (MC) simulation results. The area overhead of the 12T SRAM cell is enhanced by 1.96 times and 1.74 times as compared to the 6T SRAM cell and 8T SRAM cells, respectively [11].

2. Delay

Two ground-gated memory circuits are presented in this paper. Multi-threshold CMOS (MTCMOS) is a variation of CMOS chip technology which has transistors with multiple threshold voltages ($V_{th}$) in order to optimize delay or power. The asymmetrical 9T SRAM cell provides larger read current and shorter read delay. The Half-select technique is used in 9T SRAM cell for higher [7].

3. Power Consumption
Hailong Jiao et.al, proposed a new asymmetrically ground-gated seven-transistor SRAM cell. This new cell introduce for providing a low leakage current and high data stability in sleep mode. The 65 nm CMOS technology is used for simulation. In their paper the 7T SRAM cell compared with previously work on 6T and 8T SRAM cell. A special write circuitry is used for write operation in this 7T SRAM cell. The ground-gated technology is used to break the connection between power supplies to ground in idle mode, so that leakage current can reduce in sleep mode. A sleep transistor is connected between sources of access transistor to ground under the ground-gated technology. This sleep transistor works on high threshold value and ensures that no connection between power supply $V_{dd}$ to ground in sleep mode. For read the output single-ended sense amplifier is connected at read port. In conventional 6T SRAM the read and write operation performs on same bitline. So again and again bitlines have to recharge at $V_{dd}$ after every write operation .Therefore in 7T SRAM cell does not need to be recharged to $V_{dd}$ after write operation, because in this write bitline is used only for write operation. Due to this difference power consumption by memory array is higher in 6T SRAM cell compared to 7T SRAM cell [12].

SRAM Bit-Cell Sleep technique is widely used in processors to reduce SRAM leakage power. However, significance of leakage power savings from SRAM bit-cell sleep technique is dependent on process technology and various design parameters. Their paper evaluates the effects of design parameters on performance of 7T SRAM bit-cell sleep technique [13].

Their paper presents the design and evaluation of a new SRAM cell made of nine transistors (9T).The 9T SRAM cell achieves improvements in leakage current, power dissipation performance and read stability compared with 6T SRAM cell for low power operation. This paper compares the performance of two SRAM cell topologies, which includes the conventional 6T cell and 9T cell. In particular the leakage current, leakage power and static noise margin (SNM) of each cell is designed and examined. Compared to a conventional 6T SRAM cell, the 9T SRAM cell reduces the power consumption by 62.45% and enhances the read stability by 43.37% [8]. Some observations of literature [14] are as follows:

- **SRAM** stands static random access memory. **SRAM** is volatile in nature; it means that it holds the data as long as power supply is not cut off.
Lowering the supply voltage ($V_{dd}$) for SRAMs may reduce the leakage and switching power consumptions.

SRAM plays an important role in modern mobile phones, microprocessors, microcontrollers, and computers etc.

SRAM does not need to be refreshed as the transistors inside would continue to hold the data as long as the power supply is not cut off.

There are multi-threshold voltage devices and various circuit techniques for power reduction and performance improvement. The energy efficiency improvement of $6.24\times$ is achieved on 65 nm CMOS technology. The power reduction and performance boosting techniques both used together with the optimal device combination to enhance the energy efficiency further up to $33\times$ [15].

The author has been proposed new write assist technique for SRAM arrays. In this technique, to improve the write features of the SRAM cell, a negative voltage is applied to one of the bitlines in the SRAM cell while another bitline is connected to a boosted voltage. This technique is applied to a 10T-SRAM cell with transmission-gate access devices. The design gives $2.7\times$, $2.1\times$ faster write time, 82% and 18% improvement in write margin compared with the standard 8T-SRAM cell with and without write assist, respectively. The write assist technique enables 10T-SRAM cell to operate with 24% lower supply voltage compared with standard 8T-SRAM cell with negative bitline write assist. Due to the improved supply voltage scalability a 33% leakage power reduction is achieved [16].

The 12T SRAM cell structure uses two voltage sources, one connected with the bit line and the other one connected with the bitbar line in order to reduce the swing voltage at the output nodes of the bit and the bitbar lines, respectively. Reduction in swing voltage reduces the dynamic power dissipation when the SRAM cell is in working mode. Low threshold voltage (LVT) transmission gate (TG) and two high threshold voltage (HVT) sleep transistors are used for applying the charge recycling technique. The charge recycling technique reduces leakage current when the transistors change its state from sleep to active (OFF to ON condition) and active to sleep (ON to OFF condition) modes. Reduction in leakage current causes the reduction in static power dissipation [9]. Measured read and write functionality is demonstrated with $V_{dd}$ down to
0.35 V (~100 mV lower than the threshold voltage). Data is held down to 0.325 V with 2.53 µW standby power. The measured maximum operation frequency is 375 kHz with total power consumption 5.43 µW at 0.35 V [17].

The main reason of power dissipation is Bit line toggling of SRAM cell in write operations. To reduce this amount of power loss and achieve power efficient memory, we propose a new SRAM design that integrates charge pump circuits to harvest and reuse bit line charge. In this work, a power-efficient charge recycling SRAM is designed and implemented in 180 nm CMOS technology. Post-layout simulation demonstrates an 11% of power saving and 3.8% of area overhead, if the bit width of SRAM is chosen as 8. Alternatively, 22% of power reduction is obtained if the bit width of SRAM is extended to 64. Compared with existing charge recycling SRAM schemes, this proposed SRAM is robust to process variation, demonstrates good read/write stability, and illustrates better trade-off between design complexity and power reduction [18].

Leakage power increases dramatically in the scaled devices, becomes a significant component of total power consumption in both modes of operation. Reduction in leakage current can be achieved by using both process and circuit level techniques. At process level, leakage reduction can be achieved by controlling the dimensions (length, oxide thickness, junction depth, etc.) and doping profile in transistor. At circuit level, several techniques to reduce leakage consumption have been proposed in the literature. To reduce leakage currents, these techniques explore supply and threshold voltage leakage dependence, as well as the concepts of stacking effect and body biasing. Some of such are briefly presented below. To improve the reliability of devices leakage current should be as small as possible [19].

2.4 MTCMOS Techniques

Multi-threshold CMOS is the most widely used circuit technique for suppressing sub threshold leakage currents in idle circuits. In an MTCMOS circuit, high threshold voltage (high-\(|V_{\text{th}}|\)) sleep transistors (header and/or footer) are used to cut off the power supply and/or the ground connections to an idle low threshold voltage (low-\(|V_{\text{th}}|\)) circuit block. Hailong Jiao and Volken Kursun [20, 21] proposed power and ground gated circuits. In a power-gated MTCMOS circuit, a high-\(|V_{\text{th}}|\) header is attached between the chip power distribution network (directly connected
to the power supply) and a virtual power line (connected to the low threshold voltage circuit block) as shown in Figure 2.2

![Power gated MTCMOS circuit](image1)

**Figure 2.2 Power gated MTCMOS circuit**

In a ground-gated MTCMOS circuit, high-$|V_{th}|$ footer is inserted between the chip ground distribution network and a virtual ground line (connected to the low threshold voltage circuit block) as shown in Figure 2.3

![Ground Gated MTCMOS circuit](image2)

**Figure 2.3 Ground Gated MTCMOS circuit**

In a power and ground gated MTCMOS circuit, both a high-$|V_{th}|$ header and high-$|V_{th}|$ footer are utilized to block access to the chip power and ground distribution networks, as illustrated in Figure 2.4. In SLEEP mode, the header and footer are cut off to lower the sub threshold leakage
currents in an idle circuit block. Alternatively, in ACTIVE mode, the header and footer are activated to resume normal circuit operation with high performance.

![Figure 2.4 Power and Ground gated MTCMOS circuit](image)

A specialized low-noise MTCMOS circuit technique with three operational modes (tri-mode) is described in this section.

**1. Power and Ground Gated Tri-mode MTCMOS**

A zero-body-biased high PMOS sleep transistor is connected in parallel with a high NMOS sleep transistor. A tri-mode MTCMOS circuit operates in three modes: SLEEP, PARK, and ACTIVE. When a tri-mode MTCMOS circuit is idle, the sleep transistors (footer and parker) are cut off to place the circuit into low-leakage SLEEP mode as shown in Figure 2.5. The virtual ground line is raised to approximately the power supply voltage Vdd during SLEEP mode. The sub threshold leakage currents that are produced by the low-\(|V_{th}|\) circuit block are thereby suppressed in SLEEP mode.

Prior to the activation of the circuit, the circuit transitions to the intermediate PARK mode. The virtual ground line is discharged to the threshold voltage of parker (\(|V_{tp}|\)). The first wave of activation noise is produced during the transition from SLEEP mode to PARK mode. Subsequently, the circuit transitions from PARK mode to ACTIVE mode in order to complete the activation process. Footer is turned on to discharge the virtual ground line to ~0V as shown in Figure 2.5. The tri-mode MTCMOS circuit thereby resumes normal high performance ACTIVE mode of operation.
An alternative power-gated MTCMOS circuit with three modes of operation is illustrated in Figure 2.6. A high-Vth NMOS sleep transistor (parker) is connected in parallel with a high-|Vth| PMOS sleep transistor (header) to implement a power gating structure with three distinct modes of operation.

In SLEEP mode, both header and parker are cut off to suppress the sub-threshold leakage currents in a power-gated tri-mode MTCMOS circuit. The virtual power line is discharged to ~0V by the leakage currents produced by the low-|Vth| circuit. At the end of the idle mode, the power-gated tri-mode MTCMOS circuit is activated in two steps. Before the power-gated tri-mode MTCMOS circuit is awakening, the circuit initially transitions from SLEEP mode to the intermediate PARK mode. The parker is activated while the header is maintained cut-off. The first wave of activation noise is produced during the transition from SLEEP mode to PARK.
With the subsequent second step of activation, the circuit transitions from PARK mode to ACTIVE mode. Header is turned on to charge the virtual power line to approximately the power supply voltage $V_{dd}$. The tri-mode circuit is thereby fully activated and operates with high performance. The second wave of activation noise is produced during the transition from PARK mode to ACTIVE mode. The voltage swing on virtual power line and the current surge through sleep transistors are reduced during both SLEEP mode to PARK mode and PARK mode to ACTIVE mode wake-up steps. The activation noise is thereby suppressed in a power-gated tri-mode MTCMOS circuit.

2. Circuit Description of 6T, 7T, 8T and 9T SRAM cell with MTCOMOS Technique
Conventional 6T SRAM cell are characterized on different cell ratio with three different threshold voltage levels: low, high and dual. Figure 2.7 shows the conventional 6T SRAM cell with ground-gated technique. In this ground-gated technique, two transistors are connected (SLEEP and HOLD) between bistable circuitry and real ground line. In active mode, the SLEEP transistor is activated while the HOLD transistor is in OFF condition. In sleep mode, SLEEP transistor is in OFF condition while HOLD transistor is activated. There are two purpose of this technique, at first to minimize the leakage current in sleep mode and second is to maintain a sufficient voltage difference between $V_{dd}$ and $VGND$ [20]. Here we are using traditional structure of 6T SRAM cell as shown in figure 2.7 with different threshold configuration.
Figure 2.7 Conventional 6T SRAM cell with ground gated technique. (a) LVT 6T SRAM cell. (b) HVT SRAM cell (c) DVT 6T SRAM cell [7]

The asymmetrical 7T SRAM circuit is illustrated in figure 2.8 storing information in the cross coupled inverters. The read and write ports are separated from each other in this circuitry. The read port consists of access transistor N₄ and a NMOS transistor N₅. The ground-gated technique is used in this circuit to suppress the leakage current [12].
The Asymmetrically ground-gated 8T SRAM circuit is shown in Figure 2.9. This cell consists of two extra transistors compared to 6T SRAM cell. The simulations have been done on 65nm CMOS technology. The MTCMOS technique is used for suppressing the leakage current. The sleep transistor is connected between sources of read transistor to ground in sleep mode. A new transistor is added in this circuitry to increase the write ability. The target is that to separate read port with write port [7].
The circuit is shown in Figure 2.10, simulating on the 65nm low power multi-threshold voltage CMOS technology. In this cell three transistors are extra added with conventional 6transistor SRAM cell. Compared to 8transistor SRAM cell one extra PMOS transistor is added between power supplies to PMOS transistor of first inverter [7].

![Figure 2.10 The Asymmetrical 9T SRAM cell [7]](image)

### 2.5 Summary

From the above description it is clear that lot of research has been done and still going on in the area of low power SRAMs. It is necessary to maintain the performance parameters. In view of this, investigations have been carried out to arrive at a memory cell structure which is simple and energy efficient with acceptable performance parameters. Some research gaps are describes as below:

- Less Studies toward Optimization: There is a need to develop a computational optimization model in order to enhance the design performance of SRAM.

- Simulation not done on different cell ratio and threshold voltage.

- In the previous research, whether work on low power or higher speed. Till now these two things not combined into one SRAM.

- There is no research work existing upto Layout level of circuit and optimization at this level.

- There is no steps (circuit level, physical level, Fabrication of selected and finalized circuit) followed by a one SRAM design.