Chapter-1

Introduction and Motivation

1.1 Introduction

We have seen many technological changes in last few years and it is still going on. Before the computer age, the computation was the toughest work. After resolving this problem, new challenges began to come. More Challenges increasing day by day like speed, power consumption, delay and many more. At the time of desktop PC, design era mainly focused on optimizing speed.

Minimum-energy-driven circuit design is highly required in numerous emerging applications such as mobile electronics, wireless sensor nodes, implantable biomedical devices, etc. Due to high computing capability requirements in such applications, SRAMs play a critical role in energy consumption, because it uses the transistors.

During the desktop PC design era, VLSI design efforts have focused primarily on optimizing speed to realize computationally intensive real-time functions such as video compression, gaming, graphics etc. As a result, we have semiconductor ICs that successfully integrated various complex signal processing modules and graphical processing units to meet our computation and entertainment demands. While these solutions have addressed the real-time problem, they did not address the increasing demand for portable operation, where mobile phone needs to pack all this without consuming much power. The strict limitation on power dissipation in portable electronics applications such as smart phones and tablet computers must be met by the VLSI chip designer while still meeting the computational requirements. While wireless devices are rapidly making their way to the consumer electronics market, a key design constraint for portable operation namely the total power consumption of the device must be addressed. Reducing the total power consumption in such systems is important since it is desirable to maximize the run time with minimum requirements on size, battery life and weight allocated to batteries. So the most important factor to consider while designing system-on-chip (SoC) for portable devices is 'low power design'.
Six transistor static random access memory (SRAM) cell is one of the most widely used circuit elements in the current SoC solutions. Its integrability with CMOS digital circuits, high speed, and robustness has made it the most popular choice in on chip memory implementations.

1. Memory

What is memory?

Memory is any physical device which can store information. Memory is just like human mind which can write data, hold this data and then read out data. Memory device connected with computer, laptop, mobile or any storage capable devices. It is capable of storing information temporarily or permanently. Memory is the best essential element of a computer. The performance of computer mainly based on memory and CPU.

2. Types of memory

Memory is major part of computers that categories into several types. Memory is best storage part to the computer users to save information, programs and etc, The computer memory offer several kinds of storage media some of them can store data temporarily and some them can store permanently. Memory consists of instructions and the data saved into computer through Central Processing Unit (CPU).

Memory majorly categorized into two types, Main memory and Secondary memory as depicted in figure 1.1.

(i) Primary Memory / Volatile Memory.

(ii) Secondary Memory / Non Volatile Memory.

(i) **Primary Memory / Volatile Memory**: Primary Memory also called as volatile memory because the memory can’t store the data permanently. Primary memory select any part of memory when user want to save the data in memory but that may not be store permanently on that location. It also has another name i.e. RAM.
Random Access Memory (RAM):

The primary storage is referred to as random access memory (RAM) due to the random selection of memory locations. It performs both read and write operations on memory. If power failures happened in systems during memory access then you will lose your data permanently. So, RAM is volatile memory. RAM categorized into following types.

- DRAM
- SRAM

(ii) Secondary Memory / Non Volatile Memory:

Secondary memory is external and permanent memory that is useful to store the external storage media such as floppy disk, magnetic disks, magnetic tapes and etc cache devices. Secondary memory deals with following types of components.
Read Only Memory (ROM): ROM is permanent memory location that offers huge types of standards to save data. But it work with read only operation. No data lose happen whenever power failure occurs during the ROM memory work in computers. Types of ROM memory described below:

a. **PROM**: Programmable Read Only Memory (PROM) maintains large storage media but can’t offer the erase features in ROM. This type of RO maintains PROM chips to write data once and read many. The programs or instructions designed in PROM can’t be erased by other programs.

b. **EPROM**: Erasable Programmable Read Only Memory designed for recover the problems of PROM and ROM. Users can delete the data of EPROM thorough pass on ultraviolet light and it erases chip is reprogrammed.

c. **EEPROM**: Electrically Erasable Programmable Read Only Memory similar to the EPROM but it uses electrical beam for erase the data of ROM.

3. Why choose SRAM instead of DRAM

SRAM stands for Static Random Access Memory and DRAM stands for Dynamic Random Access Memory. Both are the part of secondary or RAM and holds data but in a different ways.

The main difference is in terms of circuit diagram and technique which is used to hold data. DRAM circuit diagram consists of single transistor and capacitor for each memory cell. So DRAM requires the data to be refreshed periodically in order to retain the data. Whereas circuit diagram of SRAM consists of an array of 6 transistors. This array can perform read, write and hold operation without refreshing again and again. It does not need to be refreshed as the transistors inside would continue to hold the data as long as the power supply is not cut off.

1.2 Motivation

SRAM is a type of memory and memory is an essential part of high performance microprocessor design. Mostly cell Area covers by the memory. So, mostly research done to reduce the area and memory area can be reduced by using scaling technique. The scaling is a main factor to disturb
the parameters of SRAM. Doping is also the main factor which affects the memory performance [2]. There is a many parameters, which is to be considered during, design. Main parameters are Delay, Leakage current and Stability. Stability directs relates to the Static Noise Margin (SNM) [8]. Many topologies are applied to enhance the system performance. Different asymmetric and symmetric SRAM cells have been proposed to improve the performance of memory.

1.3 Contributions and Outline of the Thesis: There are two main contributions for this thesis in addition to the measurement results that confirms these contributions:

1. Optimized the design constraints: stability, speed, leakage current and delay.
2. Simulation done on different SRAM cell to find better configuration.

Next chapter discusses the operation of an SRAM unit. The architecture of the SRAM Unit and different peripheral circuits that are involved in the operation of the unit is explained. Chapter 4 introduces the design of constraints, which affects the performance of SRAM cell and also introduces the various approaches to find out the data stability. Chapter 5 describes the Application of MTCMOS Technique on Conventional and Ground–Gated SRAM cell Topologies and Analyzed the Low Power SRAM Cell topologies on 65 nm technology by using various parameters. A comparison is made against the recently reported low-power SRAMs. Experimental results are also presented in the same chapter. Finally, chapter 6 concludes the thesis.

1.4 Summary

This chapter explained the importance of embedded SRAM units in current VLSI SoCs. It had been shown that the wide range of applications that need a low-power SRAM has Compelled SRAM designers to come up with innovative circuits that reduce the power consumption of this unit. On the other hand, as the technology scales, low-power design becomes a more challenging task. The limitations of a number of the recently reported schemes for power reduction are identified. Finally the outline of the thesis is presented.