ABSTRACT

All electrical signals in nature are analog and since most of the signal processing is done in the digital domain, Analog to Digital (ADC) and Digital to Analog (DAC) converters have become a necessity. Flash ADC makes all bit decisions in a single go while Successive approximation ADC makes single bit decision at a time. Flash ADCs are faster but area increases exponentially with bit length while successive approximation ADC is slow and occupies less area. Between these two extremes, many other architectures exist, deciding a fixed number of bits at a time such as pipelined and multistep ADCs. They balance circuit complexity and speed. For medium speed and with high resolution, pipelined ADCs are promising.

Although many pipelined ADC architectures are discussed in literature, the number of bits/stage was always seen to be a designer’s choice. More than 100 papers on pipelined ADCs of reputed journals are referred and conclude that many designers preferred a stage resolution of 3 bits to reduce the design complexity and time. Some others preferred 1.5 bits/stage to allow incomplete settling of op-amp and then removed the error by extra digital hardware. This made the author to probe into the various options of implementing the pipelined ADC and find the optimum stage resolution considering various performance parameters.

The objective of this work is to study and implement six different 10 bit, 50MS/sec, pipelined ADCs using 1, 1.5, 2, 3, 4 and 5 bits/stage
conversion techniques, compare and identify the optimum stage resolution. Since area, speed, power and nonlinearity are critical issues in any chip design; the author discusses the various implementation options of number of bits/stage conversion techniques in pipelined ADCs and models their effect on area, speed, power dissipation and nonlinearity. The design is implemented in 0.18μm CMOS technology and uses a 3.3V supply. To reduce the lambda effect, the channel length of MOSFETs must be at least 2 to 5 times the minimum possible. Hence a channel length of 0.5μm is chosen for analog circuits. But for digital circuits, the minimum channel length is used to save area and power. The design takes care of power optimization at every level of design. Noise and temperature analysis is done. The design is proven to be scalable and suitable for different technologies. The design is simulated using spice tool using BSIM 3V3 model files and the level of simulation is 49.

The basic building blocks required for implementing a pipelined ADC Viz. op-amp, comparator, sub converter, DAC and digital logic are all designed and well characterized. The folded cascode op-amp designed has an open loop gain of 80dB at a unity gain frequency of 250 MHz at a phase margin of 90°. The fully differential switched capacitor S/H Amplifier designed is capable of sampling at even 100MS/sec. The high speed comparator implemented has a delay less than 2.5ns.

The effect of stage resolution on different performance parameters is modeled. The simulation results convey that with pipelining, the maximum conversion frequency is seen to be almost independent of the
number of stages. This allows the bits/stage to be chosen for fulfilling other requirements. Minimizing the bits/stage also minimizes the power dissipation and area requirements. The effect of bits/stage on nonlinearity is seen to be small but the linearity is seen to improve a bit if we can increase the number of bits/stage. Therefore, confining the bits/stage to two, we get optimum results with respect to Area, Speed, Power dissipation and nonlinearity. The design also functions when properly scaled to suit different technologies. It also works for different supply voltages but at different sampling frequencies.

The designed 1-bit/stage, 50 MS/sec, Pipelined ADC has an SNR of 54.6 dB and SFDR of 69 dB at 20MHz input. The Integral nonlinearity (INL) is seen to be ±0.4 and has a Differential nonlinearity (DNL) of ±0.22. The effective number of bits is 8.8 and the design works fine for temperatures from 0 to 80°C. The design consumes 110 mW of power.