CHAPTER 3

BASIC BUILDING BLOCKS OF PIPELINED ADC
3.0 INTRODUCTION

The basic building blocks required to implement a pipelined ADC include analog blocks like Operational amplifier, Comparator and S/H amplifier. The digital logic requirements are in Digital error correction, encoders in sub-converters, shift registers and clock generation. This chapter is devoted to study the different op-amp architectures, Comparators, S/H circuit configurations, D/A Converter architectures and the digital logic.

3.1 REQUIREMENTS OF OP-AMPS IN DATA CONVERTERS

The magnitude and phase response curves of a typical op-amp are shown in Fig. 3.1.

![Fig. 3.1 Magnitude and Phase response of an op-amp](image-url)
The gain, bandwidth requirements of an op-amp must be carefully selected if it is to be used in an N-bit A/D converter. The op-amp is assumed to have 90° phase margin over full load conditions by compensating it with a load capacitance $C_L$. If phase margin is 90° then we get a response similar to an RC circuit, and hence avoid overshoot and ringing. This reduces the settling time of op-amp.

### 3.1.1 Gain requirements

The op-amp in data converter must amplify the signals to $\pm \frac{1}{2}$ LSB of its ideal value. If the open loop gain of the amplifier of Fig. 3.2 is $A_{OL}$, then, its closed loop gain can be expressed as

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}}$$  ----- Eq. (3.1)

![Fig. 3.2 Non-inverting amplifier using op-amp](image)

and the feedback factor is

$$\beta = \frac{R_1}{R_1 + R_2}$$  ----- Eq. (3.2)
Or if capacitors \( C_i \) and \( C_f \) are used then

\[
\beta = \frac{C_f}{C_i + C_f}
\]  

----- Eq. (3.3)

And the closed loop gain \( A_{cl} \) is

\[
|A_{cl}| = \frac{C_i}{C_f}
\]  

----- Eq. (3.4)

If the maximum deviation in gain is \( \Delta A \), then using equation ( )

\[
|A_{cl}| = \frac{C_i}{C_f} - \Delta A = \frac{A_{ol}}{1 + A_{ol}} \frac{C_f}{C_i + C_f}
\]  

----- Eq. (3.5)

In data converters, the maximum variation should be within \( \frac{1}{2} \) LSB of the ideal value. Therefore

\[
\Delta A = \frac{C_i}{C_f} \frac{1}{2} \frac{LSB}{Full\text{-}Scale\text{output}} = \frac{C_i}{C_f} \frac{1}{2^{N+1}} \frac{V_{ref}}{V_{ref}} = \frac{C_i}{C_f} \frac{1}{2^{N+1}}
\]  

----- Eq. (3.6)

The minimum DC open loop gain required is

\[
|A_{ol}| \geq \frac{1}{\beta} 2^{N+1}
\]  

----- Eq. (3.7)

If \( C_i = C_f \) then \( \beta = \frac{1}{2} \) and

\[
|A_{ol}| \geq \frac{1}{\beta} 2^{N+2}
\]  

----- Eq. (3.8)

i.e., for a 10-bit ADC, the op-amp must have a gain greater than 4K.

### 3.1.2 Unity gain frequency requirements

The architecture used decides the speed of an op-amp [84]. The op-amp must settle to with \( \pm \frac{1}{2} \) LSB in the least time possible. The output of an op-amp can be expressed as
\[ V_{out} = V_{out\text{final}} (1-e^{-t/\tau}) \]  \hspace{1cm} \text{----- Eq. (3.9)}

For output equal to \( \frac{1}{2} \) LSB,

\[ \frac{1}{2^{N+1}} = 1 - \frac{V_{out}}{V_{out\text{final}}} = e^{-t_{\text{settling}}/\tau} \]  \hspace{1cm} \text{----- Eq. (3.10)}

Where \( t_{\text{settling}} = \tau \ln 2^{N+1} \) and \( f_{\text{clk}} = 1/t_{\text{settling}} \)

The time constant of the circuit is

\[ \tau = \frac{1}{2 \pi \beta f_u} \]  \hspace{1cm} \text{----- Eq. (3.11)}

The minimum unity gain frequency of op-amp is then given by

\[ f_u \geq \frac{f_{\text{clk}} \ln 2^{N+1}}{\beta} \]  \hspace{1cm} \text{----- Eq. (3.12)}

If \( \beta = \frac{1}{2} \) then

\[ f_u \geq 0.22 (N+1) f_{\text{clk}} \]  \hspace{1cm} \text{----- Eq. (3.13)}

Therefore a 10bit, 50MS/sec ADC, the op-amp must have a minimum unity gain frequency of 120MHz.

### 3.2 SINGLE STAGE OP-AMPS

There are several architectures available in single stage Op-Amps viz. the simple op-amp, cascode op-amp, folded cascode op-amp and triple cascode op-amp. They can be single ended or differential.

#### 3.2.1 Simple op-amp

Fig. 3.3 (a) shows a simple single ended CMOS op-amp while Fig. 3.3 (b) shows differential op-amp.

The low frequency small signal gain of both these circuits is
A = \frac{g_{mN}}{r_{oN} + r_{oP}} \quad \text{----- Eq. (3.14)}

Where \( r_{oN} \) = output resistance of NMOS
\( r_{oP} \) = output resistance of PMOS
\( g_{mN} \) = Transconductance of NMOS.

The gain achievable is about 20 and the bandwidth is determined by the load capacitance \( C_L \).

Fig. 3.3 Simple op-amp topologies

### 3.2.2 Cascode op-amp

To achieve high gain, cascode topologies may be used. Fig. 3.4 (a) shows the single ended and Fig. 3.4 (b) shows the differential cascode op-amps or telescopic cascode op-amps. Such circuits will have a gain \( A \), given by

\[
A = g_{mN} \left( \frac{1}{r_{oN}} \right) \left( \frac{1}{r_{oP}} \right) \quad \text{----- Eq. (3.15)}
\]
Here, the gain is seen to be much higher than that of simple op-amp of Fig. 3.3. However, additional poles result in the transfer function which affects the phase margin and \( f_u \). Also the output swing is reduced and is given by

\[
V_{out} = 2[V_{DD} - (V_{D1} + V_{D3} + V_{CSS} + V_{D5} + V_{D7})] \quad \text{----- Eq. (3.16)}
\]

where \( V_{Di} \) denotes the effective gate voltage or the overdrive voltage of MOSFETs and \( V_{CSS} \) denotes the drop across the current source.

Fig. 3.4 Cascode op-amp architectures

In switched capacitor circuits, we need to short input and output of op-amps for some duration. But the severe drawback of telescopic cascode is that the output cannot be shorted back to input to realize unity gain buffers.
3.2.3 Folded cascode op-amp

A folded cascode op-amp can be used to overcome the drawbacks of telescopic cascode op-amps [85]-[87].

In Fig. 3.5 (a), the NMOS cascode amplifier is converted to a folded cascode amplifier, by replacing the input NMOS by PMOS. Also in Fig. 3.5 (b), a PMOS cascode amplifier is converted to a folded cascode amplifier by replacing the input PMOS by NMOS. In all the above circuits, the current generated by M1 flows through M2 and hence through the load to produce an output voltage.

\[ V_0 = g_m r_{out} V_{in} \]  ----- Eq. (3.17)

This idea can be applied to differential pairs also and hence the differential op-amps as shown in Fig. 3.6. A folded cascode op-amp with input NMOS driving PMOS cascode transistor provides a higher gain than a PMOS driving NMOS. This is because the mobility of charges in NMOS devices is greater. The voltage swing of folded
cascode is seen to be higher compared to that of telescopic cascode structure by the threshold voltage $V_t$, but, at the cost of higher power dissipation, lower voltage gain and lower $f_u$.

Fig. 3.6 Differential folded cascode op-amp

3.2.4 Triple cascode op-amp

Fig. 3.7 Triple Cascode op-amp
To achieve still higher gains, we can cascode more number of devices as shown in Fig. 3.7. A triple cascode typically provides a gain by \((g_m r_0)^3 / 2\) but, it further reduces the output swing as six effective gate voltages must be subtracted from \(V_{DD}\). This op-amp cannot be operated at low voltages.

### 3.3 TWO STAGE OP-AMP

This op-amp uses two stages and hence provides a larger gain. Here the first stage provides a high gain and the second stage is for providing large output swing. The individual stages can use any of the single stage op-amps discussed in previous sections. The two stage differential op-amp is shown in Fig. 3.8.

The gain of first stage is

\[
A_1 = g_{m1} (r_{o1} \parallel r_{o3}) = g_{m2} (r_{o2} \parallel r_{o4}) \quad ----- \text{Eq. (3.18)}
\]

and the gain of second stage is

\[
A_2 = g_{m6} (r_{o6} \parallel r_{o7}) = g_{m5} (r_{o5} \parallel r_{o7}) \quad ----- \text{Eq. (3.19)}
\]

To obtain still higher gains, the first stage can use cascoding of devices. In two stage amplifiers, each stage introduces at least one pole in the transfer function making it more unstable. The unity gain frequency also reduces. Hence a third stage is almost never used.

### 3.4 GAIN BOOSTING IN OP-AMPS

Single stage op-amps have the drawback of less gain while the two stage op-amp provides more gain but at reduced speeds. This made the designers to think about new approaches. In single stage op-amps,
output resistance is increased to get higher voltage gain [88] [89]. The idea of using gain boosting technique is only to increase the output resistance further.

Fig. 3.8 Simple Two stage op-amp

Fig. 3.9 Gain boosting technique
Simple cascode circuit is shown in Fig. 3.9 (a). The output impedance of this circuit is

\[ R_{\text{out}} = g_{m2} r_{01} r_{02} \]  ---- Eq. (3.20)

From Fig. 3.9 (b), it is clear that the small signal voltage produced across \( r_{01} \) is proportional to output current. If this voltage is subtracted from \( V_b \), then the output impedance will increase. The \( R_{\text{out}} \) value now modifies to

\[ R_{\text{out}} \approx A_1 g_{m2} r_{01} r_{02} \]  ---- Eq. (3.21)

Therefore, \( R_{\text{out}} \) is ‘boosted’ by a good amount without cascoding more devices on top of M2.

### 3.5 COMPARISON OF OP-AMP TOPOLOGIES

The comparison of telescopic cascode, folded cascode, two stage op-amps and the gain boosted op-amp is shown in Table 3.1.

<table>
<thead>
<tr>
<th>Op-amp type</th>
<th>Gain</th>
<th>Output swing</th>
<th>Speed</th>
<th>Noise</th>
<th>Power Dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Telescopic cascode</td>
<td>Medium</td>
<td>Low</td>
<td>Highest</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Folded cascode</td>
<td>Medium</td>
<td>Medium</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>Two stage</td>
<td>High</td>
<td>Highest</td>
<td>Low</td>
<td>Low</td>
<td>Medium</td>
</tr>
<tr>
<td>Gain Boosted</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
<td>High</td>
</tr>
</tbody>
</table>

From Table 3.1 it is clear that for low voltage and high speed applications, a folded cascode op-amp is a preferred choice.
3.6 COMPARATOR

Comparators can be classified broadly into two categories. They are Static Comparators and Dynamic Comparators.

3.6.1 Static comparators

The basic symbol and operation of a comparator is shown in Fig. 3.10. If the positive input of a comparator (Vin+) is greater than its negative input (Vin-), then the output of a comparator = logic ‘1’ and if Vin+ < Vin-, then output = logic ‘0’. A comparator inherently has three basic blocks viz. preamplifier, a decision making circuit and an output buffer.

![Comparator diagram]

**Fig. 3.10 Basic Comparator operation**

3.6.1.1 Preamplifier

A differential amplifier with active loads can be a preamplifier as shown in Fig. 3.11. The sizes of M1 and M2 are set by the currents required and their transconductance and hence the stage gain [90]-[93].
The input voltages and output currents can be related by

$$i_{0+} = \frac{gm}{2} (v_{i+} - v_{i-}) + \frac{I_{ss}}{2} = I_{ss} - i_{0-} \quad \text{&} \quad gm = \sqrt{2 \beta I_D} \quad \text{----- Eq. (3.22)}$$

Increase the size of M5/M6 with respect to M3 and M4 for increasing the gain of this circuit.

### 3.6.1.2 Decision circuit

Decision circuit, as shown in Fig. 3.12, is a crucial part used to identify the difference in signals $i_{0+}$ and $i_{0-}$ and make a decision. The circuit provides positive feedback using cross coupled inverters M6 and M7. If $i_{0+}$ is greater then $i_{0-}$, M5 and M7 are ON while M6 and M8 are OFF. If all transistors have equal ‘$\beta$’ values, and if $\beta_5= \beta_8= \beta_x$ and $\beta_6=\beta_7=\beta_y$, then

$$v_{0+} = \sqrt{\frac{2i_{0+}}{\beta_x} + V_N} \quad \& \quad v_{0-} = 0V \quad \text{----- Eq. (3.23)}$$
Fig. 3.12 Decision circuit with positive feedback

If \( i_0^- \) increases and \( i_0^+ \) decrease, then switching takes place when \( V_{DS} \) of M7 equal to \( V_{IN} \) of M6. Now, M6 starts to take current away from M5 to make M7 OFF. MOSFET M7 enters saturation when current through it is

\[
\frac{i_0^-}{2} \left( V_{o_+} - V_{IN} \right)^2 = \frac{\beta_y}{\beta_x} i_0^+ 
\]

----- Eq. (3.24)

Switching takes place when \( i_0^+ = i_0^- \). A similar analysis for increase in \( i_0^+ \) and decreasing \( i_0^- \) gives the switching point of

\[
\frac{i_0^+}{\beta_y} = \frac{i_0^-}{\beta_x} 
\]

----- Eq. (3.25)

Relating equation Eq. (3.24) with Eq. (3.25) and using Eq. 3.22, we get the switching point voltage as
MOSFET M17 is added in series with decision circuit to increase voltage out of decision circuit.

### 3.6.1.3 Output stage

Output buffer is the final circuit in comparator and is used to convert the output of decision circuit into a logic signal i.e., 0V or V\text{DD}.

![Fig. 3.13 Self-biased differential amplifier as output buffer](image)

The circuit is a self biasing differential amplifier [2] as shown in Fig. 3.13. An output inverter is added to provide additional gain and for isolation of C\text{L} from self bias differential amplifier circuit.

The overall comparator is shown in Fig. 3.14.
The important characteristics of a comparator are gain, offset voltage, transient response, propagation delay etc.

3.6.2 Dynamic comparators

The digital error correction mechanisms can be used to relax the design of comparators used in sub ADCs. Even though they have high offsets, dynamic comparators can be used to save power in pipelined ADCs and then remove the error by digital error correction.

3.6.2.1 Lewis and Grey comparator

This comparator compares \((V_{ref+} - V_{ref})\) and \((V_{in+} - V_{in})\) as shown in Fig. 3.15. For implementing 1.5-bit/stage design, the threshold levels will be \(-\frac{V_{ref}}{4}\) and \(\frac{+V_{ref}}{4}\) and for 2-bit/stage, the thresholds are \(\frac{+V_{ref}}{2}\)
and $-\frac{V_{\text{ref}}}{2}$. These thresholds can be set by adjusting the $(\frac{W}{L})$s of MOSFETs. The transistors M1 to M4 are the differential transistors operating in triode region while the remaining transistors are used for providing positive feedback for decision making.

![Lewis and Grey Comparator](image)

Fig. 3.15 Lewis and Grey Comparator

The equivalent conductance of M1 and M2 can be expressed as

$$G_1 = \mu C_{ox} \left[ \frac{W}{L} (V_{\text{ref}+} - V_i) + \frac{W_2}{L} (V_{\text{in}+} - V_i) \right] \quad \text{----- Eq. (3.27)}$$

$$G_2 = \mu C_{ox} \left[ \frac{W_1}{L} (V_{\text{ref}+} - V_i) + \frac{W_2}{L} (V_{\text{in}+} - V_i) \right] \quad \text{----- Eq. (3.28)}$$

If circuit is symmetric then the conductance $G_1$ and $G_2$ will be equal at the thresholds and this occurs when $W_2 = W_3$ and $W_1 = W_4$.

If $V_{\text{in}} = V_{\text{in}+} - V_{\text{in}+}$ and $V_{\text{ref}} = V_{\text{ref}+} - V_{\text{ref}+}$ then $V_{\text{in}} = \frac{W_1}{W_2} V_{\text{ref}}$
For \( \frac{+V_{\text{ref}}}{4} \) as threshold, \( W_2 \) must be equal to \( 4(W_1) \) and by interchanging \( V_{\text{ref}} \) and \( V_{\text{ref}}^- \), we get \( \frac{-V_{\text{ref}}}{4} \) as the threshold. Also, for \( \frac{+V_{\text{ref}}}{2} \) as threshold \( W_2 = 2(W_1) \) and so on. The draw back of this architecture is that the threshold value is a function of device symmetry. Therefore, the layout of this comparator must be done carefully.

### 3.6.2.2 Charge distribution comparator

This comparator has lower offset but consumes more power and the circuit is shown in Fig. 3.16.

![Fig. 3.16 Charge Distribution Comparator](image)

Here, the comparator threshold is a function of capacitor ratios and not the device symmetry. The capacitors \( C_{\text{in}} \) and \( C_{\text{ref}} \) are charged to
(\(V_{in^+} - V_{in^-}\)) and (\(V_{ref^+} - V_{ref^-}\)) during the first clock phase and this charge is redistributed between the capacitors during the next clock phase.

### 3.7 S/H CIRCUITS

The most crucial circuit in an A/D converter is the sample and hold circuit. During sampling mode, the input signal charges a capacitor and during hold mode, the charge on capacitor is held constant (until the next sampling) for the converter to complete conversion.

![Fig. 3.17 Output of an ideal (a) S/H circuit and (b) Track and Hold](image)

Ideally, a S/H circuit must have an output waveform as shown in Fig. 3.17 (a). During sampling, the analog input may vary and hence the need for another circuit called track and hold circuit. Here during sampling, the analog input is tracked and the value is maintained during hold mode as shown in Fig. 3.17 (b).

Fig. 3.18 shows the major errors that can result in S/H circuit. The time required for the S/H circuit to track the input signal within tolerable limits is called “Acquisition time”. If amplifier is undercompensated (phase margin <90°) then an overshoot occurs and
op-amp takes some time to settle within $\pm 1/2$ LSB. This is called “Settling Time”. During hold mode, the pedestal error results due to charge injection and clock feedthrough. The charge leakage from capacitor results in droop.

Fig. 3.18 Errors associated with S/H circuit

3.7.1 Basic S/H circuit

The simplest form of S/H circuit is shown in Fig. 3.19.

Fig. 3.19 Basic S/H circuit

During sampling, switch $S$ is closed and the input is sampled onto capacitor $C$. During hold mode $S$ is opened, so that the capacitor
retains the value. The small signal bandwidth for the circuit is decided by the capacitor C and the ON resistance ($R_{ON}$) of the switch.

$$f_{3,db} = \frac{1}{2\pi R_{ON} C} \quad \text{----- Eq. (3.29)}$$

### 3.7.2 S/H circuit with input and output buffers

To avoid loading onto the source input and output buffers can be added as shown in Fig. 3.20 [94] [95].

![S/H circuit with input and output buffers](image)

Fig. 3.20 S/H circuit with input and output buffers

If the source current is $I_{in}$, the slew rate of the S/H circuit is given by

$$\frac{dV}{dt} = \frac{I_{in}}{C} \quad \text{----- Eq. (3.30)}$$

For better slewing, $I_{in}$ must be large and this is provided by the input buffer. The overall accuracy is dictated by the op-amps used in buffer.

### 3.7.3 Switched Capacitor S/H circuit

The sample and hold circuit using switched capacitor is shown in Fig. 3.21.
The switch positions shown in Fig. 3.21 are for sampling mode. All the switches change their positions during hold mode. The circuit functionality is similar to Fig. 3.20. The switches must be carefully designed. Otherwise, they introduce charge feed through and aperture uncertainties. The S/H circuits with gain can also be implemented using switched capacitor circuits and is shown in Fig. 3.22. The circuit has three switches $S_1$ to $S_3$ and two capacitors $C_i$ and $C_f$. Fig. 3.22 shows the circuit in sampling mode. During sampling phase, the input is sampled onto $C_f$ and $C_i$ and the op-amp works like a buffer. The switches change their positions during hold mode so that $C_i$ is connected between ground and input of op-amp while $C_f$ is connected in the feedback path of the op-amp. Now the op-amp works like an inverting amplifier with a gain of $(1+C_i/C_f)$. If $C_i = C_f$ then a gain of two is achieved.
The accuracy of this circuit is decided by the ratio of capacitances. The offset errors and common mode noise can be effectively removed if differential S/H circuits are used as shown in Fig. 3.23.

At $t=t_0$, $S_1$ and $S_2$ are closed while $S_3$ is opened. The analog input is now sampled onto capacitors. At $t=t_1$, $S_1$ opens while $S_2$ is still closed. Now the op-amp is in open loop mode. As the top plate of ‘C’ is at ground, the capacitive feedthrough and charge injection because of $S_1$ going OFF becomes independent of input signal. At $t=t_2$, when $S_2$ goes OFF, the charge injection flows into the $V^+$ and $V^-$ and not onto capacitors as op-amp input impedance is very high. Therefore, the sampled charge on capacitor is unaffected. This sequence of turning OFF of switches is called “Bottom plate sampling” [96]. At $t=t_3$, the circuit goes into hold mode, with op-amp again in closed loop configuration and acts as a buffer to hold the value of capacitor. By
adding additional capacitors and switches, we can realize fully differential S/H circuit with gain.

![Diagram of Fully differential sample and hold circuit](image)

Fig. 3.23 Fully differential sample and hold circuit

### 3.7.4 Error sources in S/H circuits

The likely deviations in S/H circuit output are shown in Fig. 3.18 and the sources for these errors [97] [98] could be switch errors, kT/C noise, charge injection and capacitive feedthrough.

#### 3.7.4.1 kT /C Noise:

The output RMS noise of a simple RC circuit is equal to \( \sqrt{\frac{kT}{C}} \). This can be treated as equal to a voltage sampled onto a capacitor through an ON switch with a resistance R [99]. Substituting the values of k and T we see that the RMS noise equals 64μV for a capacitor C of 1pF and increases to 200μV for 0.1pF. Therefore, larger the capacitance value, smaller is the RMS noise. But for high speeds, the capacitor
value must be small to result in fast charging/discharging. Therefore a trade off is to be made between high speed and low noise. The dynamic power consumption is also seen to be proportional to C. Therefore, a careful selection of the value of ‘C’ is to be made.

3.7.4.2 Switch errors:

The various switch configurations and their characteristics are shown in Fig. 3.24. If NMOS transistor is used as a switch, the maximum voltage it can pass is \((V_{DD}-V_{thN})\) and if a PMOS is used as switch, then the lowest voltage it can pass is \(V_{thP}\).

![Fig. 3.24 (a) NMOS switch (b) PMOS switch (c) CMOS transmission gate (d) Characteristics of switches](image)

If CMOS transmission gate is used as a switch, it can pass a logic high or logic low without any threshold drop. The non-idealities
associated with these switches limits their usage for some applications like switched capacitor circuits [100]. The two well known non-idealities are charge injection and clock feed through.

### 3.7.4.3 Charge injection

The principle of charge injection can be explained with Fig. 3.25.

![NMOS switch illustrating charge injection](image)

When the MOSFET is ON, a charge $Q_{ch}'$ is built into the channel and when the MOSFET is made OFF, this charge is injected on both sides into $V_s$ and also the load capacitance $C_L$. Since $V_s$ is of low impedance, the injected charge will not have much effect. However, the injected charge onto $C_L$ results in a change in voltage across it. The charge/unit area induced in the channel is

$$Q_{ch}' = C_{ox} (V_{GS} - V_{in})$$

----- Eq. (3.31)

Then, the total charge in the channel is

$$Q_{ch} = C_{ox} W_L (V_{GS} - V_{in})$$

----- Eq. (3.32)
If the clock signal on the gate turns OFF fast, then this charge distributes equally on either sides of the switch [101]-[103]. Therefore, the change in voltage across \( C_L \) is

\[
\Delta V_L = \frac{-C_{ox}W.L(V_{gs} - V_m)}{2C_L} = \frac{-C_{ox}W.L(V_{dd} - V_m)}{2C_L} \quad ---- \text{Eq. (3.33)}
\]

The change in voltage across load is nonlinear since \( V_t \) is in the equation and hence results in non-linearity error in S/H circuits.

### 3.7.4.4 Capacitive feedthrough

The capacitances between Gate-Source and Gate-Drain are shown in Fig. 3.26. When Gate input goes high, the clock signal feeds through the Gate-Source capacitance and Gate-Drain capacitances. Also, since MOSFET is ON, \( V_{in} \) is also connected to \( C_L \). Therefore, \( C_L \) is charged to \( V_{in} \) and capacitance feedthrough will not have any effect [101]-[103].

![Fig. 3.26 Illustration of capacitive feedthrough](image)

When Gate input goes low, MOSFET is OFF and portion of clock signal appears across \( C_L \) given by
$$\Delta V_L = \frac{C_{gd} (V_{DD} - V_{ss})}{C_{gd} + C_L} \quad ---- \text{Eq. (3.34)}$$

Where \( C_{gd} \) is the overlap capacitance formed by the overlap of Gate and Drain areas and is given by

$$C_{gd} = C_{ox} \cdot W \cdot LD \quad ---- \text{Eq. (3.35)}$$

Where LD is overlap area of Gate/Drain or Gate/Source.

### 3.7.5 Minimization of charge injection and clock feedthrough

One of the most widely used techniques to reduce the errors due to switch non-identities is to use a dummy switch [103] [104] as shown in Fig. 3.27. Here, we add another MOSFET switch \( M_2 \), whose Drain and Source are shorted and the \((W/L)\) of this dummy switch must be \( \frac{1}{2} \) \((W/L)\) of the other MOSFET \( M_1 \). The two MOSFETs are driven by alternate clock phases. When \( M_1 \) goes OFF, half of the channel charge is injected towards the dummy switch.

![Fig. 3.27 Dummy switch used to minimize charge injection](image)

Even though drain and source of \( M_2 \) is shorted, it can still induce a charge. Therefore the charge injected by \( M_1 \) is stored in channel \( M_2 \) and hence doesn’t change the charge on \( C_L \). When \( M_2 \) goes OFF, \( M_1 \) is
ON and the charge in M2 goes towards low impedance $V_i$ and not onto $C_L$. Using transmission gates also reduces charge injection but the complementary clocks on PMOS and NMOS gates must be precisely controlled. Another method is to use fully differential circuits to cancel these effects as these non-idealities appear as common mode signal to the amplifier.

### 3.8 D/A CONVERTER

Digital to Analog converters (DAC) forms part of sub-converter logic in ADCs. The general block diagram of a DAC is shown in Fig. 3.28.

![Fig. 3.28 General Block Diagram of DAC](image)

The digital input controls the binary switch to connect different combinations of scaling network elements to $V_{\text{ref}}$. The output amplifier converts this signal to a voltage signal that can be taken out without
affecting the scaling network. A wide variety of DAC architectures exist. Major categories of DAC architectures are voltage scaling DACs, current steering DACs and charge scaling DACs.

### 3.8.1 Voltage scaling DACs

Based on the combination of resistance used they are classified into resistor string DACs and R-2R ladder DACs.

#### 3.8.1.1 Resistor string DAC

Fig. 3.29 (a) shows the architecture of a resistor string DAC [105] [106]. It consists of a string of resistors comprising $2^N$ switches and resistors, where $N$ is the bit length of the DAC.

![Resistor string DAC diagram](image)

**Fig. 3.29 (a) Simple resistor string DAC (b) Binary switch array DAC**

The resistor string is connected to $V_{\text{ref}}$ and the analog output is simply the voltage division of the resistors at the selected switch position.
This architecture is guaranteed to be monotonic as only resistors are used. Here, the converter is always connected to $2^{N-1}$ switches that are OFF and one switch which is $N$. For higher resolutions, a large parasitic capacitance is seen at the output node resulting in low conversion rates.

### 3.8.1.2 Binary switch array DAC

Fig. 3.29 (b) is a better alternative [107]. Here the array of $2N$ binary switches ensures that at the most only $N$ switches are ON and the other $N$ switches are OFF. This reduces the loading onto output and hence increases the conversion rates. For large resolutions, the number of resistors becomes large and hence occupies a large area and power. The relative accuracy of resistors is also very important. To reduce area, decrease the value of $R$. But this increases the current and hence power dissipation.

### 3.8.2 R-2R Ladder DACs

This architecture uses reduced number of resistors and switches and is a shown in Fig. 3.30. Also, only two values of resistors are required $R$ and $2R$. Looking from the right end of the resistor network, we see that the resistance to ground of any node is $2R$. The digital input controls the switches. Each node voltage is related to the reference voltage and the value decided by the switch positions. The total current through $V_{ref}$ is always constant, as the node voltages do not change with bit positions [108]-[113].
The output voltage of inverting amplifier is

\[ V_{\text{out}} = -I \cdot R \]

Where \( I \) is the total current flowing in the network because of the digital input and is given by

\[
I = \sum_{i=0}^{N-1} D_i \frac{V_{\text{ref}}}{2^{N-i}} \cdot \frac{1}{2R} \quad \text{----- Eq. (3.36)}
\]

Here, \( D_i \) is \( i \)th bit of the input digital word which is either ‘1’ or ‘0’. Matching of resistors is crucial for this architecture. Addition of dummy switches with half the resistance of real switch reduces the effects of voltage drops across resistors.

### 3.8.3 Current steering DACs

In resistor string DACs, voltage is first converted to a current which finally result in an output voltage. However, current steering DAC
uses current sources which are combined in various ways depending on the digital input. Fig. 3.31(a) shows a basic current steering DAC. This circuit needs a set of current sources of value \( I \). The MSB bit is \( D_2^{N-2} \) instead of \( D_2^{N-1} \) since the current \( I=0 \) for digital input of all zeros. i.e., a 3-bit converter needs only 6 current sources \( D_0 \) to \( D_5 \). One digital input decides whether a current source contributes to the total output current or not.

![Current steering DACs](image)

Fig. 3.31 current steering DACs (a) Generic (b) Binary weighted

The digital input to the switches must be thermometer coded as \( 2^{N-1} \) current sources exist. Another architecture of current steering DAC is shown in Fig. 3.31 (b). This circuit needs only \( N \) current sources. The current sources are binary weighted hence doesn’t need thermometer encoder. Since, output buffers are not required these DACs are suitable for high speed applications. CMOS has the capability of providing matched current mirrors and hence current steering DACs can be realized using CMOS logic. In a 10-bit DAC if the minimum
value of current is 5μA, then the maximum value will be \((2^{N-1} \times 5μA) = 2.56mA\) generating large current ratios using current mirror is a problem. Since all current sources are connected in parallel, glitches can occur due to switching of the sources. Maximum glitch occurs when binary input varies from 0111111111 to 1000000000 i.e. when all bit positions change.

### 3.8.4 Charge scaling DACs

This is a very widely used architecture in CMOS. Here, an array of binary weighted \(2^N\) parallel capacitors is used as shown in Fig. 3.32. The digital switches connect each capacitor to either \(V_{\text{ref}}\) or ground, resulting in an output voltage \(V_{\text{out}}\).

![Charge scaling DAC architecture](image)

Fig. 3.32 Charge scaling DAC architecture

The expression for \(V_{\text{out}}\) produced by \(K^{\text{th}}\) bit can be written as

\[
V_{\text{out}} = \frac{2^K C}{2^N C} V_{\text{ref}} = 2^{K-N} V_{\text{ref}} \\
\text{----- Eq. (3.37)}
\]
i.e., when $K$th bit, $D_K=1$ and all others are zero. The expression for $V_{out}$ for any digital input word is

$$V_{out} = \sum_{k=0}^{N-1} D_k 2^{k-N} V_{ref}$$

----- Eq. (3.38)

3.8.5 Cyclic DAC

The cyclic DAC uses minimum number of components. The input digital word is first converted to serial form and given as input to Digital to Analog converter as shown in Fig. 3.33. If $D_K=1$, then $V_{ref}$ is connected as input and if $D_K=0$, ground is connected to the circuit.

![Cyclic DAC Architecture](image)

The process repeats for $N$ clock cycles to complete the conversion. The output of this converter after $N$th cycle can be expressed as

$$V_{out}(n) = [D_{n-1}V_{ref} + \frac{1}{2}V_x(n-1)] \frac{1}{2}$$

----- Eq. (3.39)
The amplifier must provide an accurate gain of \( \frac{1}{2} \). Also, the S/H and summer needs to be N-bit accurate.

### 3.9 ERRORS IN PIPELINED ADCs AND SOLUTIONS

The errors that can occur in Pipeline Analog to Digital converters, their effects and probable solutions are listed in Table 3.2.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Error</th>
<th>Effect</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample and Hold</td>
<td>Offset</td>
<td>offset</td>
<td>Auto-Zero</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Nonlinearity</td>
<td>Digital correction</td>
</tr>
<tr>
<td>DAC</td>
<td>Nonlinearity</td>
<td>Nonlinearity</td>
<td>Trimming</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Calibration</td>
</tr>
<tr>
<td>Sub ADC</td>
<td>Offset</td>
<td>Offset</td>
<td>Auto-Zero</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Nonlinearity</td>
<td>Digital correction</td>
</tr>
<tr>
<td>Amplifier (interstage)</td>
<td>Offset</td>
<td>Nonlinearity</td>
<td>Auto-Zero</td>
</tr>
<tr>
<td></td>
<td>Gain error</td>
<td>Nonlinearity</td>
<td>Trimming</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Calibration</td>
</tr>
</tbody>
</table>

Auto zeroing, trimming and calibration techniques are discussed extensively in literature. Digital error correction techniques also solve the problem in situations where one stage creates error and the next stage cannot solve it. The error can be removed by adding redundancy
(extra bits). However, these extra bits will not increase the resolution of the Analog to Digital converter. The mismatches in sampling capacitors also result in an error. To overcome this, capacitor error averaging technique may be used.

3.10 DIGITAL LOGIC

Error correction, shift register bank, clock generation and encoding logic in sub-converters forms the digital logic in pipeline A/D Converters. As the design is implemented in 0.18 μm CMOS process, the minimum channel length of 0.2 μm is used for all devices used in digital logic.

3.11 CLOCK GENERATION

The switched capacitor S/H amplifier circuit of Fig. 5.4 requires two phase non-overlapping clock signals. If a simple inverter is used then the waveforms will be as shown in Fig. 3.34. There is an overlap of two waveforms for a small duration. A slightly more complex circuit is used to generate two phase non-overlapping clock as shown in Fig. 3.35, with a non-overlap time of at least one gate delay (Δ) for each clock change. If inverter and NOR gate delays and are equal, then the waveforms will be as shown in Fig. 3.35(b).
To speed up system operation and to minimize the rise and fall time we use buffers in clock circuitry.

Fig. 3.34 (a) Inverter generating two phase clock  (b) Waveforms

Fig.3.35 2-Φ Clock generation with NOR gates (a) circuit (b) waveforms
Fig. 3.36 shows the circuit generating three phase non-overlapping clock. The amount of non-overlapping time is set by the delay in series with the output or NOR gates.

Fig. 3.36 Generation of 3-phase non-overlapping clock signals

The inputs to the circuit of Fig. 3.36 are generated from the clock signal by the circuit shown in Fig. 3.37.