CHAPTER 1

INTRODUCTION

The Integrated Circuit (IC) technology is tremendously growing day by day to improve the performance of the CMOS technology in a compact and high-density form. The traditional CMOS technology faces some of the limitations, such as short channel effects and quantum effects, etc. Therefore, there is a necessity for alternate devices to CMOS as well as to build the digital circuits at Nano-scale. Hence, a new tiny IC arena introduced by Lent et al., is the Quantum-dot Cellular Automata (QCA) to overcome the pitfalls of conventional CMOS technology. With the advent of a new form of IC design brings a new way of binary computing using QCA for high-performance digital circuits compared to the existing nano-computing devices. An optimized logic circuit can be designed by using the majority gates, inverter and binary wires using QCA cells in an appropriate combination. In this thesis, the implementation of optimized logic circuits using QCA is explained in detail.

This chapter consists of five sections. The first section outlines the motivation and problem statement of the proposed research work. The research aim and objectives of the research are explained in the second and third sections. The fourth section presents the research contributions of the proposed research work. In the fifth section, the organization of proposed research work is presented.

1.1 Motivation and Problem Statement

In the VLSI domain, the CMOS created a new era IC technology with an optimized form of digital circuits. However, it has a few limitations to create nanoscale devices, such as short channel effects, doping fluctuations, and expensive lithography, etc. A major problem in CMOS technology is the power dissipation since the circuit capacitances are charged to a potential and discharged to the ground, which dissipates nearly all the energy contained in the logic signal. The device density, power dissipation, and performance are vital in different IC technologies that provide innovative solutions to integration and computations. In Nanotechnology, especially
QCA offers new enhancements for computing with its unique properties. QCA relies on fresh physical phenomena since its logic states are stored in a position of the pair of electrons instead of voltage levels. The main advantage of QCA is that there is no requisite to dissipate most of the signal energy repeatedly and it has extremely small feature size.

Recently many researchers have been developing different efficient digital circuits using QCA. Hence, the proposed research work is motivated to design efficient digital circuits with an optimized performance in terms of the number of cells, area, and clock cycles. The proposed research work started with conventional CMOS digital structures using QCA and extended to arithmetic circuits to construct with high performance in a cost-efficient manner. This research work focused on designing the different nanocircuits, such as parity generator, a parity checker, equality byte comparator, serial bit stream magnitude comparator, single and multi-digit BCD adders.

1.2 Research Aim

The key motive of the proposed research work is to design an optimized digital circuit using an emerging nanodevice called QCA with high-performance. To exploit the capability of QCA the conventional 2’s complement adder and subtractor, Baugh-Wooley multiplier using Carry Save Adder (CSA) are implemented for the first time in QCA. XOR gate and its applications using QCA are constructed in a single layer structure. New techniques are proposed to construct high-performance serial bit stream cascading magnitude comparator, single-digit BCD adder and multi-digit BCD adder in an optimized manner for digital circuits at the Nano-scale.

1.3 Research Objectives

1. To design digital arithmetic circuits with a reduced amount of complexity, fewer delays, a minimum number of cells and increased speed.
2. To construct the layout for conventional 2’s complement adder and subtractor, Baugh-Wooley multiplier using CSA for better performance.
3. To implement XOR gate and its applications in a single layer structure for reducing the cost function with the absence of crossovers.
4. To design a high-speed serial bit stream cascading magnitude comparator for performing the serial bit stream data comparison with higher speed.
5. To propose a new logic for designing the single and multi-digit BCD adders which can achieve the high performance.

1.4 Research Contributions

The main contributions of the research work with the proposed methods are as given below:

- The digital arithmetic circuits are designed with various benefits, such as reduced amount of complexity, reduced number of cells in the layout, simplified connections to decrease the delays and to achieve higher processing speed.
- To explore the QCA benefits, conventional structures like 2’s complement adder and subtractor, Baugh-Wooley multiplier using CSA are implemented.
- To reduce the cost of QCA structures, XOR gate and its applications are carried out in a single layer.
- Additional logic is proposed in addition to the n-bit magnitude comparison algorithm to design a serial bit stream cascading magnitude comparator to perform the serial bit stream data comparison with higher speed.
- An optimized single and multi-digit BCD adder is designed by combining the hybrid structure of Carry Flow Adder (CFA) type-II binary adder with the 2:1 multiplexers.
- A new correction logic is proposed for single and multi-digit BCD adders to achieve high performance.

All the above circuits are evaluated using various parameters such as a number of cells (cell count), area, latency, and clock zones and showed the performance of the proposed designs are better compared to the existing methods in QCA. The proposed research work is an attempt to know the possible strategies and trade-offs in the QCA circuits for high-level circuit designers.
1.5 Organization of Thesis

The thesis comprises of seven chapters. Figure 1.1 shows the organization of the thesis. Chapter 1 presents introduction and overview of the thesis. Literature review and realization of conventional structures using QCA is presented in chapter 2. Chapters 3 to 6 describe the contributions of the proposed research work. Chapter 7 presents conclusion and future research work. Details about each of these chapters are described as follows:

Chapter 1 Presents the introduction, the problem statement, aim of the work, research objectives, research contributions and overview of the thesis.

Chapter 2 Describes the literature review associated with QCA. This Chapter also presents existing conventional structures such as 2’s complement adder/subtractor and Baugh-Wooley multiplier using CSA implemented with QCA. QCA fabrication using hetero structure in III-V domain and Technical gaps are also presented.

Chapter 3 Presents the XOR gate structures in a single layer structure and its applications in detail. Implementation and performance evaluation results of the proposed structures are also presented in this chapter.

Chapter 4 Presents the implementation of the serial bit stream cascading magnitude comparator and its simulation results in detail.

Chapter 5 Presents the detailed implementation of single-digit BCD adders and its simulation results. Also, the performance parameters are evaluated with various performance parameters such as area, the number of cells, clock zones and the latency.

Chapter 6 Presents the detailed implementation of high-speed multi-digit BCD adders and its simulation results. Further, the performance parameters are evaluated such as area, the number of cells, clock zones and the latency by comparing with the conventional digital circuits.

Chapter 7 Presents the summary, conclusion of the research work and a brief discussion on the future scope.
CHAPTER 1
Motivation and Problem Statement, Research Aim, Research objectives,

CHAPTER 2
Literature Survey
- Prerequisites of QCA
- Conventional Structures Implemented with QCA
- 2’s complement adder/subtractor and Baugh Wooley multiplier
- Fabrication and Technical gaps

CONTRIBUTIONS

CHAPTER 3
XOR GATE AND ITS APPLICATIONS IN A SINGLE LAYER STRUCTURE

CHAPTER 4
SERIAL BIT STREAM CASCADING MAGNITUDE COMPARATOR

CHAPTER 5
ENHANCED SINGLE-DIGIT BCD ADDERS

CHAPTER 6
AN OPTIMIZED HIGH-SPEED MULTIDIGIT BCD ADDERS

CHAPTER 7
Summary, Conclusion and Future scope

Fig. 1.1 Organization of the Thesis