ABSTRACT

In the last two decades, contemporary Complementary Metal Oxide Semiconductor (CMOS) circuits dominated the Integrated Circuit (IC) technology in a rapid manner. However, CMOS circuits suffer from short channel effects and quantum effects, which limit the IC technology to progress further in Nanotechnology devices design. In order to overcome these existing CMOS limitations, a new technology named Quantum-dot Cellular Automata (QCA) is introduced in the nanodevice design. The key benefits of this emerging nanodevice are high device density, low power dissipation, and higher clocking speed. Even though, many efficient arithmetic circuits are designed using QCA; still, there is a lot of improvement required to fulfill the design requirements of the nanocircuit structures. Hence, new methodologies are proposed to overcome the existing pitfalls of a QCA structures to design the optimized digital circuits, in order to meet the nanocircuit library requirements. The proposed design methodology improves the speed of the circuit and minimizes the circuit area significantly, which are vital in the nano design technology.

The proposed research work uses the QCA technology to design digital circuits in an optimized manner at the nano level. Initially, the conventional structures such as 2’s complement adder and subtractor, Baugh-Wooley multiplier is presented to exploit the advantages of QCA. Afterwards, various existing XOR gate structures are analyzed. It is identified that there is a possibility to optimize the XOR gate layout. So, an enhanced XOR gate layout structure is presented in a single layer. The XOR gate structure is more significant in many applications such as a Half Adder, Full Adder, Equality Byte Comparator, Parity generator and checker, etc.,. All these applications are implemented by enhanced XOR gate layout structure. The proposed structures are implemented without using crossovers, which reduces the number of cells required and performs the functionality in a cost efficient manner with higher speed.

In the case of serial data communication, speed is a major limitation. Hence, this thesis presents a cascading serial magnitude comparator to perform the serial data
comparison in a faster manner. The proposed cascading comparator is designed by introducing an additional logic in addition to the n-bit magnitude comparison algorithm. The proposed design improves the speed of the serial data comparison compared to the existing designs with the overhead of area.

Further, the proposed research work is concentrated on the design of efficient single-digit and multi-digit BCD adders to perform the decimal addition in an optimized fashion. For this, two innovative designs are proposed, in which the first design is the combination of Carry Flow Adder (CFA) type-II binary adder and 2:1 multiplexer. The second design is implemented with a new correction logic to anticipate the carry propagation in the conventional BCD adder.

The performance of the proposed digital circuit designs is evaluated with the existing designs by comparing the various parameters such as the number of cells, area, delay, cost, etc. From the obtained results, it is noticed that the proposed designs yield significantly better results compared to the existing designs. The layouts and functionality of the proposed designs are analyzed using QCADesigner tool version 2.0.3.