Chapter 4

ERROR CORRECTIONS

4.1 Introduction

A large number of analog to digital converters (ADC) are now commercially available. Such ADC’s differ from each other in mechanism used to convert the analog signal into digital data and thus resulting in variations of speed, accuracy and cost. The ADC types popular in process control applications are:

(i). Dual Slope Integration Type,
(ii). Successive Approximation Type and
(iii). Parallel Comparator Type.

The Dual Slope Integration Type is cheaper and slower. Parallel type, on the other hand, is fastest but expensive. The choice of the type is obviously determined by the requirements of the application. In applications where the variation of the original analog signal is slower than the speed of conversion of the slowest ADC, there is no point to choose the fastest ADC having the highest cost. Rather it will be wise to choose the slowest ADC with higher resolution.

Process Signals are normally slow in nature. Dual Slope ADCs have comparatively larger conversion time. Even then they are popular in process control applications because of their low cost and their speed match well with the process requirements. INTERSIL 7109 is a dual slope ADC and is popular in process control applications because of the following reasons [4.1]:

(i) Low cost
(ii) High resolution (12 bit data + Polarity + Over Range Indication)
(iii) High Accuracy (typically within ±3 counts)
(iv) Up to 30 conversions per sec
(v) Byte organized, TTL compatible three state outputs and UART handshake mode for simple parallel or serial interfacing with microprocessor systems
(vi) True Differential Input and Reference
4.2 **Sources of Errors**

The two most common sources of errors that directly affect the performance of the integrating type A/D Converters are as follows:

1. *50 Hz noise pick-up on the signal lines in industrial environment and*

2. *Integrating non-linearity arising during analog to digital conversion process in dual slope analog to digital converters.*

4.3 **50 Hz Noise Reduction**

50 Hz line frequency pick-up is the major source of disturbance in analog data acquisition system in industrial environments. Extensive shielding and filtering are normally required to overcome such pick-up. However, its effect on the output of a Dual-Slope ADC can be easily minimized by proper choice of clock frequency. Unfortunately, the commonly used crystal (14.318 MHz.) in 8088 microprocessor based analog data acquisition systems with ICL 7109 ADC makes the system most susceptible to 50 Hz noise as discussed in section 4.4.2 below. The problem is studied for different system clock frequencies and the most suitable crystal frequency for working in 50 Hz environments is determined. The work [4.2] is described below:

4.3.1 **Principle of Operation**

In a Dual Slope A/D Converter, the input voltage is first integrated for a fixed period of time (2048 clock cycles in case of ICL7109 ADC) and then it is replaced by a reference voltage of opposite polarity until the integrator output reaches zero. The first and the second phases are normally referred to as integrate and de-integrate phases respectively. The integrator outputs in integrate and de-integrate phases are shown in Fig. 4.1 for two different input voltages (Vin1 & Vin2).

Integrator output (Vo) at the end of integrate phase (T_I), depends upon the area (Vin x T_I) traced out by the input voltage and is proportional to the input voltage as T_I is constant. In de-integrate phase, as the integrator integrates the reference voltage of opposite polarity, the output moves up at a constant rate irrespective of the integrator output at T_I. However, the time taken (T_D) by the integrator output to cross zero depends upon its value at T_I and hence upon the input voltage. As in Fig. 4.1, the de-integration times are T_{D1} & T_{D2} for
input voltages Vin1 & Vin2 respectively. Thus de-integration time (TD) is a measure of converted output. This time is used as the gate pulse to a counter which produces the converted output. The counter output is latched internally after the zero crossing is detected and gives the digital output.

4.3.2 Noise Elimination

In presence of a sine wave interfering signal superimposed on the input dc voltage, the modified waveforms of the integrator are shown in subsequent figures.

Fig. 4.2 plots the input/output waveforms of the integrator in absence and in presence of the ac interfering noise. Since the interfering signal is random in nature, it can occur in any phase with respect to the beginning of the integrate phase of the ADC. Two such situations are demonstrated in the waveforms in Fig. 4.2 and Fig. 4.3.

In Fig. 4.2, integration starts with zero phase of the interfering signal. The part of the interfering signal above the dc traces out more area than that traced out by the part below the dc. Therefore, the net area under the resultant input curve is greater than that without

![Fig. 4.1: Input & Output Waveforms of the Integrator in Dual Slope AD Converter for two different input voltages.](image-url)
the interfering signal. This causes a greater output voltage resulting in a longer de-
integration time $T_{Da}$ with respect to $T_{D0}$.

![Fig. 4.2: Integrator Input/Output Waveforms for an ac interfering signal superimposed on the dc input. Integration starts with the zero phase of interfering ac.](image)

On the other hand, in Fig. 4.3, integration starts at some other phase of the interfering signal. The area contributed by the ac signal alone is negative producing a lesser area under the resultant input signal than that traced out by the input signal in absence of the interference. This ultimately causes a lesser de-integration time $T_{Db}$ than $T_{D0}$.

![Fig. 4.3: Integrator input and output waveforms for an ac interfering signal superimposed on the dc input. Integration starts with some phases of the interfering signal.](image)
Therefore, the interfering signal causes a random variation of output even if its frequency remains the same. One way to eliminate such noise is to use a filter circuit at the input of ADC and/or to give extensive care for input signal cabling which often becomes expensive.

A simpler solution, however, is to make the integration time $T_I$ equal to an integral multiple of interfering signal time period $T_P$ (20 ms for 50 Hz noise). Fig. 4.4 and 4.5, depict the input and output waveforms of the integrator in presence of interfering ac signal having time period $T_P$ equal to the integration time $T_I$ with different initial phases of the interfering signal. The resulting area contributed by the interfering signal alone will be zero irrespective of the phase of the interfering signal at the start of integration. The integrator output reaches exactly the same value as that due to the dc input alone. This causes no change of the de-integration time $T_{D0}$ irrespective of the phase of the interfering signal at the start of integration phase.

![Diagram](image)

*Fig. 4.4: Integrator waveforms for a sine wave ac interfering signal having time period equal to the integration time. Integration starts at zero phase of the interfering signal.*
4.3.3 Clock Consideration and Implementation in 8088–Based System

In the previous section it has been shown that 50 Hz noise can be eliminated during analog to digital conversion itself using dual slope AD Converter, provided the ADC clock frequency is such that the integration time is an integral multiple of 20 ms. The clock of an 8088 based system is generated by the dedicated clock generator 8284A. This chip contains an on-chip oscillator whose frequency is controlled by an external crystal. The 8284A generates the microprocessor clock (CLK) with required 33% duty cycle at one-third the crystal frequency. It also generates another clock (PCLK) at one-sixth the crystal frequency with 50% duty cycle for operating peripheral devices. The peripheral clock (PCLK) is fed to the ICL7109 which is further subdivided inside the ADC chip by a factor of 58 to generate its operating frequency ($f_{\text{ADC}}$). The integrating period of the ADC is 2048 cycles of this internal clock. Therefore, the integrating time $T_I$ in terms of crystal frequency ($f_{\text{XTL}}$) is given by:
\[
T_i = 2048 \times \frac{1}{f_{ADC}(\text{inHz})} (s) = 2048 \times \frac{1}{f_{XTL}(\text{inHz})/6 \times 58} (s) = \frac{712.704}{f_{XTL}(\text{inMHz})} (ms) \ldots \quad (2.1)
\]

The requirements for the integration period \(T_i\) of 20, 40, 60 ms, therefore, sets the crystal frequency of the microprocessor based system and are given in Table 4.1.

**Table 4.1: Crystal frequencies for 20, 40 and 60 ms integration time.**

<table>
<thead>
<tr>
<th>Integration Period (T_i) (ms)</th>
<th>No of full cycles of 50 Hz noise</th>
<th>7109 internal clock Freq. (f_{ADC} = (2048/T_i)) (kHz)</th>
<th>8284A PCLK Freq. (f_p = f_{ADC} \times 6) (MHz)</th>
<th>CPU Clock Freq. (f_x = 2 \times f_p) (MHz)</th>
<th>8284A Crystal Freq. (f_{x} = f_p \times 6) (MHz)</th>
<th>conv/sec (each taking 8192 ADC clock cycles)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>1</td>
<td>102.4000</td>
<td>5.9392</td>
<td>11.878</td>
<td>35.6352</td>
<td>12.5</td>
</tr>
<tr>
<td>40</td>
<td>2</td>
<td>51.2000</td>
<td>2.9696</td>
<td>5.9392</td>
<td>17.8176</td>
<td>6.2</td>
</tr>
<tr>
<td><strong>60</strong></td>
<td><strong>3</strong></td>
<td><strong>34.1333</strong></td>
<td><strong>1.9797</strong></td>
<td><strong>3.9594</strong></td>
<td><strong>11.8784</strong></td>
<td><strong>4.2</strong></td>
</tr>
</tbody>
</table>

Since 8088 CPU can operate at a maximum frequency of 5 MHz, the choice of crystal frequency is 11.8784 MHz which generates the microprocessor clock at 3.96 MHz, causing nearly 17% loss in processing speed. This loss in processing speed can be tolerated because microprocessor based system dedicated for process control application can hardly utilize the full power of the 8088 processor. The higher clock frequencies indicated in Table 4.1, however, are usable for faster CPU and peripheral chips.

Schematic connection of the ADC with the 8088 based system is shown in Fig. 4.3. The same was designed and fabricated by the author. As seen in the figure, the System Clock is generated by the 8284A Clock Generator. The crystal (Xtal) of frequency “f” is attached to the 8284A which produces system clock of frequency “f/3” as well as the peripheral clock of frequency “f/6” to run the ADC. The ADC data lines are connected directly to the system data bus. Conversion control, on the other hand, was done by the on board 8255A programmable peripheral interface. Data reading of the ADC is controlled by suitable address decoding.
4.3.4 Experimental Set-Up

The experimental set-up consisted of the microprocessor based system described earlier which was controlled by a Personal Computer through an In-circuit Emulator as shown in Fig. 4.7. The in-circuit emulator is used to download the machine language monitor program (Intel HEX file) into the onboard RAM of the system as well as to upload the results stored in system RAM into computer’s memory for viewing and verification.
4.3.5 Experiment

The most commonly used microprocessor crystal of frequency 14.31818 MHz in 8088-based system gives an integration time of 49.8 ms. This is nearly two and a half 50 Hz cycles leading to the worst 50 Hz noise susceptibility. On the other hand, the prescribed crystal of frequency 11.8784 MHz having 60 ms integration time eliminates the 50 Hz noise totally. The following experiments were carried out to demonstrate the improvements of system noise rejection using the prescribed crystal over the others:

Experiment – 1:

In the first set of experiments, 50 Hz sine wave noise of known amplitudes are added on a nominal dc input of nearly 1V and applied to the ADC for three different crystals as given below to see their relative rejection capabilities.

(i). 11.8784 MHz (the prescribed crystal)
(ii). 14.31818 MHz (the commonly available crystal)
(iii). 10.245 MHz (another arbitrary crystal)
Experiment -2:
Another set of data were also taken with 11.8784 MHz crystal in presence of a known interfering sine wave voltage with slightly varying frequency around 50 Hz to see the capability of noise rejection of the system. This was done to study the stability of the design under a maximum of 5% line frequency variation which is the acceptable limit.

In both the experiments a set of 100 data for the same input signal was recorded so that the effect of noise on the output could be determined from the spread in the converted value.

4.3.6 Software to Run the ADC
Assembly language program to run and control the ADC was developed which was then converted (using cross assembler and linker) into machine language and downloaded into the onboard RAM of the microprocessor based system. Assembly language source codes are given in Appendix 1. The flow chart of the assembly language program is presented in Fig. 4.8 and Fig. 4.9 below.

![Flow Chart](image)

*Fig. 4.8: Flow Chart for reading and storing ADC data for 100 successive conversions.*
4.3.7 Experimental Results

Experiment – 1

Data were taken for different experimental setups and recorded in Appendix 2. Histograms of the recoded data are presented below:
Exp No – 1.1

![Bar graph showing ADC data and % occurrence for Exp No – 1.1](image)

**Fig. 4.10:** Plot of % Occurrence Vs ADC Output (Hex) for $f_{\text{xtl}} = 10.245 \text{ MHz}$, $|V_{\text{dc}}| = 0.9926V$, $V_{\text{ac}} = 100 \text{ mV}$

Exp No – 1.2

![Bar graph showing ADC data and % occurrence for Exp No – 1.2](image)

**Fig. 4.11:** Plot of % Occurrence Vs ADC Output (Hex) for $f_{\text{xtl}} = 14.31818 \text{ MHz}$, $|V_{\text{dc}}| = 1.0035V$, $V_{\text{ac}} = 99.9 \text{ mV}$

Exp No – 1.3

![Bar graph showing ADC data and % occurrence for Exp No – 1.3](image)

**Fig. 4.12:** Plot of % Occurrence Vs ADC Output (Hex) for $f_{\text{xtl}} = 11.8784 \text{ MHz}$, $|V_{\text{dc}}| = 0.9950V$, $V_{\text{ac}} = 100.0 \text{ mV}$
Observations

Histograms in Fig. 4.10 – 2.12 demonstrate the occurrence of the ADC outputs for different set of 50 Hz noise and crystal frequency. They also display the span of variation of the ADC outputs. From Fig. 4.12, it is also observed that the count spread in case of 11.8784 MHz crystal converges to ±1 count (regretting the 2% occurrence of 07B3 count in comparison with others) which is within the inaccuracy limit of the ICL7109.

Integration Times ($T_I$) for the three crystals, the number of 50 Hz cycles contained in $T_I$ and the probable and experimental variation of ADC counts due to 100 mV 50 Hz signal injection are listed in the Table – 4.2 for different crystal frequencies.

<table>
<thead>
<tr>
<th>Crystal Frequency $f_{XTL}$ (MHz)</th>
<th>Integration Time</th>
<th>No of 50 Hz cycles in $T_I$</th>
<th>Worst Case errors (mV)</th>
<th>Max ADC count spread due to 50 Hz signal injection.</th>
<th>Experimentally observed spread (Decimal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.245</td>
<td>69.566</td>
<td>3.478</td>
<td>± Max Av value of the noise over 0.478T</td>
<td>± 172 counts – 100 mV noise</td>
<td>56</td>
</tr>
<tr>
<td>11.8784</td>
<td>60.000</td>
<td>3.000</td>
<td>0.000</td>
<td>-</td>
<td>3 (regretting 07B3 count)</td>
</tr>
<tr>
<td>14.31818</td>
<td>49.776</td>
<td>2.489</td>
<td>± Max Av value of the noise for 0.489T</td>
<td>± 176 counts – 100 mV noise</td>
<td>137</td>
</tr>
</tbody>
</table>

The experiment was repeated for 50 mV ac signal injection. The statistical analysis of the experimental data for 50 mV and 100 mV ac interfering signal, are presented in Table 4.3, from which the improvement on using the 11.8784 MHz crystal can be seen. The small deviation observed in the 11.8784 MHz case is attributed to the inherent 1 count fluctuation in analog to digital conversion.
Table 4.3: Statistical Presentation of Experimental Data (DC signal Value = 1V)

<table>
<thead>
<tr>
<th>AC input (mV)</th>
<th>Crystal Frequency (MHz)</th>
<th>Standard Deviation (mV)</th>
<th>Maximum Deviation from Mean Value (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>14.31818</td>
<td>11.7</td>
<td>17.0</td>
</tr>
<tr>
<td></td>
<td>11.8784</td>
<td>0.026</td>
<td>0.7</td>
</tr>
<tr>
<td>100</td>
<td>14.31818</td>
<td>23.45</td>
<td>34</td>
</tr>
<tr>
<td></td>
<td>10.245</td>
<td>6.073</td>
<td>21.5</td>
</tr>
<tr>
<td></td>
<td>11.8784</td>
<td>0.042</td>
<td>0.7</td>
</tr>
</tbody>
</table>

Experiment – 2
Experimental data were recorded in Appendix 2. Histograms of the recorded data are presented below:

Exp No – 2.1

Fig. 4.13: Plot of % Occurrence Vs ADC Output for $f_{xil} = 11.8784$ MHz, $|V_{dc}| = 0.9980V$, $V_{ac} = 0.0$ mV
Exp No – 2.2

![Graph showing % Occurrence Vs ADC Output for $f_{xtl} = 11.8784 \text{ MHz}$, $|V_{dc}| = 0.9980\text{V}$, $V_{ac} = 100.0 \text{ mV/47 Hz}$]

**Fig. 4.14:** Plot of % Occurrence Vs ADC Output for $f_{xtl} = 11.8784 \text{ MHz}$, $|V_{dc}| = 0.9980\text{V}$, $V_{ac} = 100.0 \text{ mV/47 Hz}$

Exp No – 2.3

![Graph showing % Occurrence Vs ADC Output for $f_{xtl} = 11.8784 \text{ MHz}$, $|V_{dc}| = 0.9980\text{V}$, $V_{ac} = 100.0 \text{ mV/48.2 Hz}$]

**Fig. 4.15:** Plot of % Occurrence Vs ADC Output for $f_{xtl} = 11.8784 \text{ MHz}$, $|V_{dc}| = 0.9980\text{V}$, $V_{ac} = 100.0 \text{ mV/48.2 Hz}$

Exp No – 2.4

![Graph showing % Occurrence Vs ADC Output for $f_{xtl} = 11.8784 \text{ MHz}$, $|V_{dc}| = 0.9980\text{V}$, $V_{ac} = 100.0 \text{ mV/48.8 Hz}$]

**Fig. 4.16:** Plot of % Occurrence Vs ADC Output for $f_{xtl} = 11.8784 \text{ MHz}$, $|V_{dc}| = 0.9980\text{V}$, $V_{ac} = 100.0 \text{ mV/48.8 Hz}$
Exp No – 2.5

Fig. 4.17: Plot of % Occurrence Vs ADC Output for $f_{xtl} = 11.8784$ MHz, $|V_{dc}| = 0.9980V$, $V_{ac} = 100.0$ mV/50 Hz

Exp No – 2.6

Fig. 4.18: Plot of % Occurrence Vs ADC Output for $f_{xtl} = 11.8784$ MHz, $|V_{dc}| = 0.9980V$, $V_{ac} = 100.0$ mV/51 Hz

Exp No – 2.7

Fig. 4.19: Plot of % Occurrence Vs ADC Output for $f_{xtl} = 11.8784$ MHz, $|V_{dc}| = 0.9980V$, $V_{ac} = 100.0$ mV/51.9 Hz
Exp No – 2.8

Fig. 4.20: Plot of % Occurrence Vs ADC Output for $f_{xt} = 11.8784$ MHz, $|V_{dc}| = 0.9980$ V, $V_{ac} = 100.0$ mV/53 Hz

Observations

It is observed from the above plots that there are no errors in case of

a) no ac interfering signal and

b) 50 Hz ac interfering signal (20 ms cycle time)

The absence of errors in case of 50 Hz. interfering signal is due to the fact that integrating time which is 60 ms (11.8784 MHz crystal) contains equal number of opposite half cycles of the interfering noise.

The above experimental results also show that the rejection is incomplete in cases of other slightly varying noise frequencies. Table 4.4 lists % deviation of the output as a function of % deviation of noise frequency from 50 Hz.

Table 4.4: Deviation of System Accuracy for Noise Frequency Variation

<table>
<thead>
<tr>
<th>Frequency Deviation from 50 Hz (%)</th>
<th>Deviation of output (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>± 2</td>
<td>± 0.085</td>
</tr>
<tr>
<td>± 4</td>
<td>± 0.122</td>
</tr>
<tr>
<td>± 6</td>
<td>± 0.2</td>
</tr>
</tbody>
</table>
A plot of the spread of ADC output on either sides of the central point with the variation of noise frequency around 50 Hz is presented in Fig. 4.21. It is seen that the spread is minimum at 50 Hz and is increased symmetrically on either sides.

![Fig. 4.21: Plot of ADC output spread with noise frequency](image)

### 4.4 Integrating non-linearity

The performance of a microprocessor based analog data acquisition system is primarily determined by the accuracy of analog to digital converter (ADC). Accuracy of the ADC is affected by both the external noise (like 50 Hz pick-up in signal line as discussed in the previous section) and also by internal causes. Integrating analog to digital converters, suffer from the integrating non-linearity which is an internal problem caused by the improper selection of the analog components. ADC chip manufacturers studied the problem arising due to (i) dielectric absorption in the integrating capacitor and (ii) stray charge pick-up on the integrating and auto-zero capacitors in details. Their experiments revealed that the effect of dielectric absorption can be minimized by the use of polypropylene capacitors [4.1] having low dielectric absorption. The effect of stray charge pick-ups can be minimized by connecting the outer foil of auto-zero capacitor to RC summing junction and the inner foil to pin 31 of the ADC chip. In India, manufacturers of metalized polypropylene capacitors do not indicate the leads connected to the inner and outer foils. Thus non-availability of such information itself makes it
difficult to maintain quality in a manufacturing environment. Besides, users in Indian face the problem of working in high humidity and high temperature conditions, where board level leakage also produces significant effect. Experiments performed by us [4.3] revealed that the input output relation of ICL7109 ADC is non-linear though the components are selected properly. It also revealed that commonly suggested remedy of using epoxy green mask on the printed circuit board (PCB) can not remove the problem totally. A software correction routine was contemplated and has subsequently been implemented to determine the deviation of output for a known reference and outputs are then modified accordingly. The work [4.3] is described in details in the next section.

4.4.1 Experimental Setup
A series of experiments were carried out with an ICL7109 ADC based data acquisition board to illustrate the effects of atmospheric humidity on the analog to digital conversion accuracy for the circuits fabricated on PCBs with and without green masking. A procedure is suggested that can be used in a microprocessor based system for dynamic compensation of this effect. The experiments were performed on the Intel 8088 microprocessor based system with onboard ICL7109 designed by the author. The system block diagram of the 8088 based system is shown in Fig. 4.22.
Fig. 4.22: Block Diagram of the 8088 based system with the arrangements for the correction of AD Conversion Non-Linearity. Input dc and ADC’s own reference voltages are selected through the multiplexer for conversions. The conversion error is determined from the deviation of the converted data for the reference voltage from its actual value (2048 counts) from which the correction factor is determined and then applied for other inputs.
4.4.2 Principle of Operation

As already discussed, in a dual slope ADC, the input voltage is integrated for a fixed period of time ($T_i$) after which the input is replaced by a known reference voltage of opposite polarity until the output crosses zero. The ideal input/output waveforms of the Integrator as shown in Fig. 4.1 are redrawn in Fig. 4.23.

When the circuit is working under high humidity condition, the water molecules coming in contact with the board creates a surface leakage path. Under this condition, the integrating capacitor loses some charge through surface leakage during integrate as well as de-integrate phases. The leakage of the integrating capacitor ($C_f$) can be represented by a resistance ($R_f$) placed parallel to it as shown in Fig. 4.24. The magnitude of this resistance of course depends on the humidity and temperature.

*Fig. 4.23: Integrator’s ideal input/output waveforms.*
The effect of this leakage resistance on the integrator output can be determined for a step input as follows:

Frequency domain network equation for the above circuit can be written as,

\[ \frac{V_o(s)}{V_i(s)} = Z_f \left( \frac{1}{R_i} \left( \frac{R_f}{R_f + \frac{1}{sC_f}} \right) \right) = \frac{R_f}{R_i \left( 1 + sR_fC_f \right)} = \frac{1}{R_iC_f} \left( \frac{1}{s + \frac{1}{R_fC_f}} \right) \]  \hspace{1cm} (4.2)

For step input \( V_i(s) = \frac{V}{s} \), equation 4.2 then reduces to,

\[ V_o(s) = \frac{V}{R_iC_f} \left( \frac{1}{s + \frac{1}{R_fC_f}} \right) \]  \hspace{1cm} (4.3)

Taking inverse Laplace Transform of equation 4.3, the time domain network equation can be obtained as,

\[ v_o(t) = \frac{VR_f}{R_i} \left( 1 - e^{-\frac{t}{R_fC_f}} \right) \]  \hspace{1cm} (2.4)
The exponential term in equation (4.4) indicates that after a finite time (like $T_I$ or $T_D$), the output always reaches a lower voltage (solid line) than expected (dotted line) in absence of the leakage in the capacitor, as shown in Fig. 4.25. During integrate as well as de-integrate phases, the leakage causes quicker discharge of the capacitor. The two effects thus add up to produce a lower converted output ($T_D'$). It is evident from the figure that the amount of data loss ($\Delta T_D$) is dependent on the integrator output at the end of the integrate phase or in other words determined by the value of the input voltage.

![Integrator Output](image)

*Fig. 4.25: Integrator output in presence of board leakage (solid line) and for ideal case (broken line).*

### 4.4.3 Correction Procedure

The ICL7109 is designed to produce an output of $07FF_{16}$ (2048) counts when the input voltage is equal to the ADC reference and $0FF_{16}$ (4096) when the input is double this value. The ADC reference voltage thus provides the means for checking the correctness of the converted data. All that is needed is to convert the ADC reference voltage and compare it with the standard value ($07FF_{16}$), which gives us a measure of the error due to leakage. In our system, a multiplexer (Fig. 4.22) is used to switch between the unknown input signal and the reference voltage alternately for conversion by the ADC. The converted data ($R$) for reference input is first noted and stored in memory. The error corresponding to this conversion ($07FF - R$) is thus calculated. For software error correction, the exponential variation of error with input voltage is approximated to a linear one as indicated by the straight line intersecting the error curve of Fig. 4.26(a) at the reference point. The slope of this approximate error line is then easily computed from
the measured error at the reference point from which the error corresponding to any measured input can be evaluated and corrected accordingly. The error curve after the proposed correction is implemented and is shown in Fig. 4.26(b). As evident from the figure, the compensation is complete when the input voltage is equal to Vref. But it is over-compensated and under-compensated for inputs below and above this value respectively.

![Error vs Input voltage](image)

(a) Before compensation  (b) After compensation

Fig. 4.26: (a) Conversion error versus input voltage (solid line) and the linear approximation of the software error correction scheme (broken). (b) Error becomes minimized after the software error correction is invoked. Error correction is complete at Vref, over corrected below Vref and under corrected beyond Vref.

### 4.4.4 Experiment

The experiments were carried out in a controlled environment on two boards, one with green masking and the other without masking, to study the variation of ADC output for different values of temperature and humidity. A switch is interfaced to let the system display either the uncorrected or the corrected value in a display unit. The flow chart of the assembly language program running at the back end is outlined in Fig. 4.27. Assembly language source codes are given in Appendix 1.
4.4.5 Experimental Results and Data Analysis

Experiments in three different environmental conditions ($35^\circ\text{C}/85\%\text{RH}$, $35^\circ\text{C}/95\%\text{RH}$, $45^\circ\text{C}/95\%\text{RH}$) are performed and a set of uncorrected and corrected data for both the green masked & unmasked boards for different input voltages are taken. The data are presented in Appendix 3.

---

Fig. 4.27: Flow Chart of the system monitor program.
The error (without correction implemented) versus the input voltage for the three different ambient conditions for both the green masked and unmasked boards are plotted in Fig. 4.28 and Fig. 4.29.

The error as seen in Fig. 4.28 and 2.29 is significantly larger for the unmasked board. Also the error increases, as expected, with humidity and temperature.
The results are also plotted in Fig. 4.30 to Fig. 4.32 with and without error correction technique implemented for both the boards under all the three environmental conditions for comparison.

![Graph showing conversion error before and after correction for the two boards measured at 35°C, 85% RH.](image)

**Fig. 4.30:** The conversion error before and after correction for the two boards measured at 35°C, 85% RH.

![Graph showing conversion error before and after correction for the two boards measured at 35°C, 95% RH.](image)

**Fig. 4.31:** The conversion error before and after correction for the two boards measured at 35°C, 95% RH.
It is seen that for values of the input voltage less than the reference, the errors are over corrected by the proposed scheme whereas the results are under corrected for higher inputs. This is because of the linear approximation of the quadratic error curve as shown in Fig. 4.26. It is also observed from the results that even after the correction, the results obtained from the unmasked board are still quite large but for the board with green mask, it is within ±3 counts which is less than ±0.1% for a 12-bit data, an acceptable result in most situations. It may however be noted that even better results can be achieved by considering more than one reference points, all derived by suitably scaling the same ADC reference source, and approximating the quadratic curve by a piece-wise linear one.

4.4.6 Conclusion

After getting correct digital data from analog to digital converter, linearization is necessary (as sensor outputs are mostly non-linear) for proper calculation of process value. Two such linearization techniques are presented in the next chapter.

Fig. 4.32: The conversion error before and after correction for the two boards measured at 45°C, 95% RH.