Chapter 1

Introduction

1.1 Motivation

Wireless communication is assuming an undeniably huge part in regular day to day existence. Both settled and portable remote frameworks empower individuals and gadgets to exchange data without the requirement for wiring, which decreases execution expenses of communication systems and makes the use of wireless devices more convenient.

As wireless systems turn out to be increasingly well known, the interest for higher data rates, new services and functionality of wireless devices increases. In addition to fundamental communication abilities, present day wireless terminals join different extra innovations like digital camera, audio and video recorder and player and also different software applications like clock, calculator etc. With a specific end goal to implant these advances into wireless devices, factors like minimal cost, low power utilization and reduction
in dimensions of various blocks utilized for manufacturing of mobile devices become critical.

Because of recent advancements, there has been a developing pattern to decrease the quantity of parts involving the handset area of the wireless devices. Specifically, direct conversion architectures have increased expanding consideration due to their potential for a high level of integration and low power utilization [1-7]. Further, advances in semiconductor innovations, most eminently in CMOS technology, have made the way for the System On-Chip (SOC) design, in which radio and baseband modem and in addition application elements of a cell phone are embedded in a single chip.

The number of wireless standards has developed astoundingly, starting an enthusiasm for multi-standard and multi-band systems. To serve multiple systems, remote terminals should be reconfigurable. As the required adaptability is moderately simple to accomplish in the digital domain, research endeavors have centered in the later past on moving the analog to-digital conversion stage towards the antenna and performing more and more signal processing tasks, such as down-conversion, demodulation and distortion removal in digital domain. The multi-band operation requires evacuation of RF filtering as much as possible. This inclination is fortified by the pressure to reduce component count and board size.

Despite the fact that a huge advance has been made, the analog segment remains a bottleneck of the entire wireless system, particularly on the receiver side. As a result of reduced RF selectivity, solid blocking signals
might be available at the receiver input and cause its desensitization, impeding the reception of the desired signal. Despite of very small section of analog processing left, there is still place for analog imperfections, for example, crosstalk, nonlinearities creating inter-modulation and cross-modulation distortion, DC offset and gain/phase quadrature imbalances deteriorate the quality of the desired signal.

In direct conversion receiver (DCR), significant kinds of interferences are second-order Intermodulation distortion (IMD2), I/Q mismatch and DC offset. These distortions result from circuit nonlinearities combined with hardware layout asymmetries and unavoidable device parameter mismatches due to fabrication process variations. Because of random nature of device mismatches, the amount of distortion is itself random. Therefore, sufficient distortion rejection might not be guaranteed during the design stage.

Nevertheless, the receiver dynamic range must not degrade as a result of distortions. Accordingly, many methods of overcoming the problem have been proposed. Since the Low Noise Amplifier (LNA) and down-conversion mixer is the main contributor to distortions, most techniques focus on improving their performance by introducing certain post-production corrections. However, an issue of the sensitivity of these corrections to changes in the operating conditions becomes apparent.

The availability of DSP processing power in modern integrated receivers opens up new possibilities. Most importantly, the inherent lack of mismatches of digital circuits can be exploited in order to cancel imbalances in the analog
section and improve the distortion rejection. Moreover, cancellation of distortion can be carried out automatically, reducing production testing burden and allowing maintaining the improved performance over time.

Consequently, exploration of efficient on-chip distortion cancellation methods supported by digital signal processing is of interest. In conclusion, distortion removal method should not increase the component counts in the RF section of receiver, as well should not occupy large amount of resources in DSP back-end section. These stringent requirements can be fulfilled only by the computationally less complex method implemented fully in DSP back-end section. The method proposed in this thesis fulfills all this requirements.

1.2 Research Contribution

In the area of distortion removal methods, one innovative method has been proposed and implemented. The proposed method is based on a cascaded structure of multiplier and adder. A procedure to calculate multiplier coefficient also called as calibration constant for distortion removal is presented. A self calibration technique is also presented here. The Self calibration technique adapts calibration constants during the life of the system, rejects the distortion and regenerate the I/Q signals with minimum error. Multiplier and adder structure can be easily implemented in DSP back-end section. The self calibration technique does not require high computational complexity and therefore proposed method with self calibration technique can be easily implemented in DSP back-end section without requiring many
resources on DSP back-end. No hardware change in RF section of receiver is required to implement this method, as it is implemented in DSP back-end. This results into a cost-effective upgrading solution. In addition, there is no constraint regarding modulation scheme and power level in the proposed method. These features make the proposed method very attractive. The proposed distortion cancellation scheme is evaluated using advanced computer simulation tool. A corresponding hardware demonstrator has been designed and implemented.

1.3 Organization of the Thesis

The thesis is organized as follows. Chapter 2 introduces receiver design considerations. Various types of receiver architecture, their comparison, test parameters, working principle of direct conversion receiver and types of distortion in DCR are discussed. Particular stress is put on the origins of the distortions and factors affecting the distortions in DCR.

Chapter 3 provides an overview of methods that can be applied to improve reduction of distortions in DCR, including layout and circuit techniques as well as compensation and calibration schemes. Lastly, architectural methods are explored.

In chapter 4, a detailed mathematical analysis of proposed method is presented. The distortion removal ability of proposed method is also represented analytically.
Chapter 5 provides analysis and results for the proposed method. A hardware prototype is designed to evaluate the proposed scheme and measurement results of the proposed method are presented.

Conclusions of the research work carried out are presented in chapter 6. A brief performance comparison between the proposed method and other methods published in literature are also presented. At the end, suggestions for further work in the area of the distortion removal technique in DCR are also discussed.