ABSTRACT

Analog to Digital Converter (ADC) is the most essential interface between the analog and digital systems for advanced electronic applications. There are different ADC architectures designed for high-speed data conversion in image processing, digital video broadcasting system, wireless and communication related applications. Among the various ADC architectures, pipelined ADC can achieve a good balance between accuracy and conversion rate with low complexity and low power consumption. However the power consumption achieved using conventional techniques was not up to the expected level as required in wireless and video applications. Hence techniques to reduce power consumption in pipelined ADCs are essential to have efficient integrated circuits for wireless, wired and mobile systems. In the present work, five novel techniques are designed and analyzed for better linearity and power reduction in 10-bit pipelined ADC.

In this first technique, a Split Capacitor Sharing Correlated Double Sampling (SCS-CDS) technique is designed in first four stages to improve the performance of CDS. In order to reduce the memory effect problem and the number of op-amps, op-amp sharing technique is incorporated in remaining stages to improve the performance of pipelined ADC. The proposed ADC is carefully designed to reduce the accumulation of predictive error of Multiplying Digital-to-Analog Converter (MDAC) due to the finite gain of
op-amps, without additional switches and capacitors at the input. The 10-bit pipelined ADC is designed in an 180nm CMOS process, achieves 56.15 dB Signal-to-Noise-and-Distortion Ratio (SNDR) and 62.9dB Spurious-Free Dynamic Range (SFDR). The pipelined ADC has an active area of 0.50mm² and consumes 7.629mW with a 1.8V supply. In the proposed ADC the double loading problem caused in the first stage of 10-bit pipelined ADC is avoided by integrating Programmable Gain amplifier (PGA) in the first stage. Switched capacitor topology based programmable gain amplifier with the integration of 10-bit pipelined ADC consumes 25.54mW of power at 100 MSPS from a 1.8V power supply. This ADC was designed for wireless receiver application.

Double sampling and op-amp sharing techniques are used to reduce power consumption for video applications. Double sampling is to enhance the sampling speed. A 10 bit 165 MSPS pipelined ADC which consumes 22mW of power is designed. The ADC is designed in a 180 nm CMOS process and achieves 64 dB SFDR, 56.1 dB SNDR, 9.02 Effective Number of Bits (ENOB) and 0.25PJ/step Figure of Merit (FOM) for a 1.6 Vpp differential input signal and 9 MHz input frequency from a 1.8V supply voltage.

Power reduction techniques such as parallel sampling and op-amp sharing technique with low-power gain boosting amplifiers have been used. In op-amp sharing technique, the number of amplifiers used is halved and parallel sampling technique processes a full-scale large input signal range and the desired SNDR is achieved with a smaller sampling capacitors.
The reduction in capacitors results in less area and power consumption with parallel sampling MDAC. Simulation results of a 10-bit 200MSPS low power pipelined ADC showed 62.9dB SFDR, 55.90 dB SNDR and ENOB of 8.99 bits respectively, with 18mW power consumption at a supply voltage of 1.8V.

To further save power and die space, the front-end Sample-and-Hold Amplifier (SHA) is eliminated and aperture error is minimized by matching the RC delays between the comparators and input sampling networks. A pipelined ADC suitable for low power applications incorporating Merged Capacitor Switching (MCS) technique is designed. The ADC achieves an SNDR of 55.67dB SFDR of 62 dB and exhibits an FOM of 0.49 pJ/conversion-step while drawing 9.77mW from a 1.8V power supply. Also SHA-less pipelined ADC using a combination of simultaneous capacitor sharing and variable $g_m$ op-amp is used to reduce the power consumption and memory effects. Simulation results show that the required SFDR of 70dB, SNDR of 56.1dB and 9.02 ENOB have been achieved with a 2MHz input signal while consuming only 7.3mW power from 1.8V supply for the System-on Chip (SoC) Digital Television (DTV) application. Several power reduction techniques such as SCS-CDS and op-amp sharing, double sampling and op-amp sharing technique, parallel sampling and op-amp sharing technique, SHA less architecture using MCS and op-amp sharing and simultaneous capacitor sharing and variable $g_m$ op-amp are implemented in this work. The results are analyzed in terms of performance measures of an ADC.