CHAPTER 8

CONCLUSIONS AND RECOMMENDATIONS

8.1 CONCLUSIONS

- The pipelined ADC employs split capacitor sharing CDS technique and op-amp sharing technique for power reduction. The sub circuits of various stages were integrated to form the single bit stage which was then cascaded to form the 10-bit pipelined ADC. A 2-bit Flash ADC which is used as the last stage of the 10-bit pipelined ADC was designed using a resistor divider branch and three clocked dynamic comparators. To correct the output of analog chain which generates 18 bits, delay elements and full adders are included, as the digital correction which generates the final 10-bit output. Also, switched capacitor based PGA was integrated with the proposed pipelined ADC to avoid double loading problem in the first stage. The average power consumption of Programmable Gain Amplifier with the integration of 10-bit pipelined ADC was 25.54mW. The INL and DNL were calculated to be +0.74/-0.74 LSB and +0.31/-0.31 LSB. Positive value of DNL shows the ADC to be monotonic and an SNDR of 56.15 dB shows that it is noise resistant. Simulation results show that this Pipelined ADC achieves a 62.9 dB SFDR and 0.133pJ/step FOM for a 1.6V 20 MHz differential input signal. Since this ADC achieves a very good FOM and conversion time this ADC is very suitable for other applications like wireless receiver applications.
A 10-bit 165MSPS pipelined analog to digital converter is used for HDTV and high frame rate video applications. This architecture employs both double sampling and operational amplifier sharing techniques in the MDAC circuits for power reduction. The sub circuits of various stages were integrated to form the single bit stage which was then cascaded to form the 10-bit pipelined ADC. A 2-bit Flash ADC which is used as the last stage of the 10-bit pipelined ADC was designed using a resistor divider branch and three clocked dynamic comparators. To correct the output of analog chain which generates 18 bits, delay elements and full adders are included, as the digital correction which generates the final 10 bit output. The INL and DNL were calculated to be -1/+ 0.41 LSB and -1/+0.6 LSB. Positive value of DNL shows the ADC to be monotonic and an SNDR of 56.1dB shows that it is noise resistant. Simulation results show that this pipelined ADC achieves a 64 dB SFDR and 0.25pJ/step FOM for a 1V 9MHz differential input signal. Since this ADC achieves a very good FOM and conversion time, this ADC is very suitable for high performance video applications.

A 10-bit 200MSPS pipelined analog to digital converter was designed for HDTV and high frame rate video application. This architecture employs both parallel sampling and operational amplifier sharing techniques in the MDAC circuits for power reduction. The sub circuits of various stages were integrated to form the single bit stage which is then cascaded to form the 10 bit pipelined ADC. A 2-bit Flash ADC which is used as the last stage of the 10 bit pipelined ADC is designed using a resistor divider branch and three clocked dynamic comparators. To correct the output of analog chain which generates 18 bits, delay elements and full adders are included, as the digital correction which generates the final 10 bit output. The INL and DNL were calculated to be +0.74/-0.74 LSB and +0.31/-0.31 LSB. Positive value of DNL shows the ADC to be monotonic.
monotonic and an SNDR of 55.90 dB shows that it is noise resistant. Simulation results show that this pipelined ADC achieves a 62.9 dB SFDR and 0.177pJ/step FOM, consumes 18.0mW power and also occupies an area of 0.32 mm² for a 1.6V 9MHz differential input signal.

- The pipelined ADC with merged capacitor switching and op-amp sharing technique is implemented in 180nm CMOS technology and occupies a die area of 1.3mm². The obtained Differential Non-linearity (DNL) and the Integral Non-linearity (INL) are +0.32/-0.32 LSB and +0.67/-0.67 LSB respectively. The obtained Signal to Noise Distortion Ratio (SNDR) for the input frequency of 2MHz at 40MSPS is 55.67dB and Effective Number of Bits (ENOB) is 8.95 and consumes 9.77mW from 1.8V supply and have been designed for SoC DTV application.

- In simultaneous capacitor sharing and variable $g_m$ op-amp a low power 10-bit 40 MSPS pipelined ADC suitable for SoC DTV is designed. By removing the front-end SHA, considerable power saving is obtained. The capacitor and variable $g_m$ op-amp is used to reduce the power consumption of pipelined ADC. The variable $g_m$ operational transconductance amplifier used in the design have been designed with a gain of 86 dB. Dynamic comparator is also designed and the same is used to build sub-ADC’s which generates the LSB and MSB of the each single stage. The third and fourth stages have also been designed and finally the 3-bit Flash ADC which is used as the last stage of the 10-bit pipelined ADC is designed. The Simulation results of the pipelined ADC in a 180nm CMOS process shows an SFDR of 70 dB, SNDR of 56.12 dB, ENOB of 9.02 bits and FOM of 0.35pJ/step while consuming only 7.3mW power for a 2 MHz input signal that confirms the effectiveness of these techniques in reducing the power, while maintaining the proper dynamic performance which makes the pipelined ADC suitable for SOC Digital TV application.
8.2 SCOPE FOR FUTURE WORK

As an extension of this work, the 10-bit pipelined ADC can be designed by using 45nm/90nm technology for further reduction in the power consumption. Also the conversion rate can be increased to GSPS suitable for space applications. The pipelined ADC can be designed by using TSMC libraries and can be fabricated.