CHAPTER 4

DESIGN OF PIPELINED ADC USING DOUBLE SAMPLING AND OP-AMP SHARING TECHNIQUE

4.1 INTRODUCTION

Double sampling and amplifier sharing techniques for video applications, are discussed in this chapter. To reduce power consumption more efficiently, the stage scaling technique has been applied to the ADC and dynamic comparators are used in sub-ADCs.

4.2 ARCHITECTURE OF PIPELINED ADC USING DOUBLE SAMPLING (DS) AND OP-AMP SHARING TECHNIQUE

The architecture of a 10-bit pipelined ADC with 1.5-bit per stage is presented in Figure 4.1.

Figure 4.1 Architecture of 10-bit pipelined ADC with double sampling and op-amp sharing technique
The front-end sample and-hold (SH) and the first two stages use the Double Sampling (DS) technique and the remaining stages op-amp sharing technique has been used. Same sizes of the sampling capacitors are used to meet the noise and matching characteristics. Therefore, an amplifier can be shared between the two consecutive stages optimally. The specification of pipelined ADC for video application is considered while designing the ADC (Martin Trojer et al. 2008).

4.2.1 Description of sub-circuits

The designed pipelined ADC uses double sampling technique for the front end sample and hold circuit to increase its sampling rate. The various sub-circuits needed to realize the circuits are sample-and hold circuit, two-stage class A/AB OTA, dynamic comparator, double sampling and op-amp sharing MDAC, sub ADC and 2-bit Flash ADC.

4.2.2 Double Sampling MDAC

Double sampling is a technique used to enhance the sampling speed. Double sampling technique takes the advantage of the fact that the op-amp is not active during sampling phase where the sampling capacitors play the major role. So the two parallel paths are created with inverse timing which makes it possible to take advantage of the op-amp in both of two phases. Two parallel sets of capacitors are used to enhance the speed (Takuji Miki et al. 2012, Furuta M. et al. 2006). These capacitors are switched alternatively between the sampling and holding phase (S. Haider et al. 2005). Double sampling technique not only reduces the power consumption of the amplifier due to its reduced unity-gain-bandwidth but also makes it possible to use the optimum amplifier in each stage. Figure 4.2 shows the double sampling MDAC configuration used in 1.5-bit per stage. Opposite phase clocks are used to control the two parallel paths. During the first phase capacitor $C_{S1^+}, C_{F1^+}$ and $C_{S1^-}, C_{F1^-}$ are charged to the input voltage
and $C_{F2}^+$ and $C_{F2}^-$ are connected in feedback (Shylu D.S., et al. 2014). $C_{S2}^+$ and $C_{S2}^-$ are connected to a reference voltage generated by sub-DAC which in turn is determined by the digital output of sub-ADC. Figure 4.3 shows the timing diagram of double sampling MDAC.

![Figure 4.2 Circuit diagram of double sampling MDAC](image)

![Figure 4.3 Timing diagram of double sampling MDAC](image)

As shown in timing diagram, when clock phase $\Phi_1$ is in the sampling phase, the op-amp is used in the second stage which is in MDAC mode. When clock phase $\Phi_2$, the second stage samples its input signal and the first stage uses the op-amp.
4.2.3 Amplifier sharing MDAC

Amplifier sharing technique involves sharing the amplifiers between two successive stages along a single pipeline ADC (Mohammad Reza Ashraf et al. 2011). In the designed Pipelined ADC the optimum unit capacitor for stage 3 is same as that of stage 4 and the same is true for stage 5 and stage 6, stage 7 and stage 8 of the pipeline ADC. Hence, an op-amp can be shared between two adjacent conversion stages. Thus the amplifiers in the last stages of the pipeline ADC are shared between two adjacent conversion stages instead of double sampled. Figure 4.4 describes the amplifier sharing technique for stage 4 to stage 8 of pipelined ADC. Since the amplifier is not needed during the sampling phase, it will be active during the half clock period. Op-amp can be used for stage N when first clock is high, otherwise it can be used for stage N+1. Figure 4.5 shows the timing diagram of amplifier sharing MDAC. As shown in timing diagram, the two sets of capacitors, $C_{S_{13}}$-$C_{F_{13}}$ and $C_{S_{23}}$-$C_{F_{23}}$, sample the input signal to stage 3 in $\Phi_1$ and $\Phi_2$ respectively. The capacitors are connected to the amplifier in only half of the next clock phase ($\Phi_2$ or $\Phi_1$), which is $\Phi_{23}$ and $\Phi_{13}$. The amplifier of stage 3 functions in $\Phi_3$ and it can be used for stage 4 in $\Phi_4$. The op-amp is shared between stage 3 and stage 4 in $\Phi_3$ and $\Phi_4$, while the input signal to stage 3 is sampled in $\Phi_1$ and $\Phi_2$ (Sahel Abdinia et al. 2009).
4.2.4 Sample and hold circuit

In order to improve the accuracy and speed of ADC, sample and hold circuit was used. Figure 4.6 shows the circuit diagram of sample and hold circuit. The sample and hold circuit operating in $\Phi_1$ and $\Phi_2$ uses the timing skew insensitive double sampled architecture (Haider S. et al. 2005). The sample and hold circuit is required to capture a wideband input signal and drive the large load capacitance of the next stage of the pipelined ADC with low distortion. The double sampling technique increases the sampling rate and also reduces the power consumption by increasing the settling time of the op-amp. Op-amp is shared with two parallel paths which is possible because the op-amp is needed only during one half of the clock cycle.
Due to the inherent parallelism in the circuit, the Double sampling MDAC becomes more susceptible to timing skew. Figure 4.7 shows the timing diagram of sample and hold circuit. As shown in timing diagram, two additional clock phase $\Phi_1$ and $\Phi_2$ are essential to act as multiplexer, which shares the sampling switch to the circuits. The sample is taken by applying a short zero pulse to the sampling switch. Each sample pulse is generated with same edge of a full speed clock signal and thus any systematic error between the channels is avoided (Mikko Waltari 1999). Due to the large signal swings the MOS-switch on-resistance is a limitation on the tracking speed and the settling time.
The on resistance has a nonlinear voltage dependence which produces distortion when tracking continuous time signals. These effects are well-defined in the input switches of the SHA.

4.2.5 Dynamic comparator

Pipelined architecture gives large correction range of offset errors of comparators and allows the use of dynamic comparators. Figure 4.8 shows the circuit diagram of dynamic comparator. This comparator has no static power consumption. By using the clock signal clk$_{2p}$, which falls earlier than the signal clk$_2$, the sampling of reference voltage is done. Figure 4.9 shows the timing diagram of dynamic comparator. As shown in timing diagram, when clk$_1$=1 the reference voltage and the comparator offset are sampled in the capacitor. When clk$_{1p}$ goes high, the comparator's outputs are reset. When signal clk$_{1p}$ goes low, the transistor M$_c$ is turned on and the outputs are generated by the positive feedback of M3- M6. During the amplifying phase (clk$_2$=1) the feedback switch is turned off and the output signal is amplified. Therefore, at the end of the amplifying phase the signal is regenerated to logic high or low by the latch (Wei-Hsuan Tu et al. 2008). By using clk$_{1p}$ as a latch clock, the comparators outputs are generated without the settling behavior of the pipelined stage being degraded.

![Figure 4.8 Circuit diagram of dynamic comparator](image-url)
4.2.6 Sub-ADC and Sub-DAC

The sub-ADC quantizes the input signal and generates the intermediate bits for each stage. For 1.5 bits per stage architecture the sub-ADC generates any one of the three binary states as its output: 00, 01 and 10. The sub-ADC consists of two differential comparators with reference voltages set at $+V_{ref}/4$ and $-V_{ref}/4$, where $+V_{ref}$ and $-V_{ref}$ represent the range of the differential input signal to the comparator. The outputs of the sub-ADC are sent to a logic block which generates the control signals for the sub-DAC. This logic block along with the sub-DAC will generate the three allowable binary states for the 1.5 bit per stage architecture. The architecture of the sub-ADC and sub-DAC is depicted in Figure 4.10. The role of the sub-DAC is to supply the residue amplifier and the gain stage with an analog voltage level that represents the quantized portion of the input signal that was fed to the 1.5 bit stage architecture. The quantized portion of the input signal is subtracted from the original input signal to create a residue voltage that will be sent to the next stage. The sub-DAC calculates the residue voltage for that stage according to the outputs from the sub-ADC. For architecture with 1.5 bits per stage, the sub-ADC can have one of the three binary outputs: 00, 01, and 10. These correspond to the sub-DAC outputs of $-V_{ref}/2$, 0, $+V_{ref}/2$ respectively.
4.2.7 Operational Transconductance Amplifier (OTA)

A novel cascode compensation scheme called hybrid cascode compensation has been introduced (Kim C. et al. 2006, Li Su et al. 2005). In this method, two distinct capacitors are used between two low-impedance nodes of the first stage and the output node. In turn, this compensation technique merges (Waltari M. et al. 2001) compensation methods. This scheme of compensation yields a higher amplifier bandwidth compared to the standard Miller and conventional cascode compensation techniques at the cost of more complex design procedure for the settling behavior of the amplifier (Yavari M. et al. 2004). This technique also offers all advantages of the cascode compensation technique such as high PSRR, etc. A low-voltage and low-power two-stage class AB amplifier based on an OTA is being designed (Reza Latfi et al. 2005). Figure 4.11 shows a two-stage class A/AB OTA composed of a folded-cascode as the first stage and the class AB amplifier with active current mirrors as the second stage that employs the hybrid cascode compensation technique. The class AB structure of the second stage reduces the OTA power consumption and the hybrid cascode compensation enhances its speed. The first stage is a folded cascode amplifier with PMOS input transistors. The second stage is a class AB amplifier with active...
current mirrors. Two separate capacitors, \( C_1 \) and \( C_2 \), have been used for compensation of the op-amp where \( C_1 \) is used in a signal path and \( C_2 \) in a non-signal path.

![Figure 4.11 OTA used for MDAC and sample and hold circuit](image)

For a supply voltage of 1.8V an initial power budget of 2.5mW was allotted, which gives total biasing current of 1666\( \mu \)A. This is the total current from rail to rail which should be divided into five branches. Then 600\( \mu \)A was distributed for differential input amplifier pair, 300\( \mu \)A for single side common source output stage amplifiers and 233\( \mu \)A for each branch of current mirror circuit. Here the targeted output differential swing was 1.8V, whereas total output swing is equal to twice of \( (V_{dd} - V_{od4} - V_{od5}) \). Therefore, \( V_{od4} + V_{od5} \leq 0.5 \) V. The initial assumption is to start with \( V_{od4} = 1.35 \) V, \( V_{od5} = 0.45 \) V after a careful analysis. Initial W/L values (in \( \mu \)m) can be chosen by using the current expression in saturation region operation (Toihria I. et al. 2010). The initial assumption is such that \( \mu_n * C_{ox} = 150 \) \( \mu \)A/V\(^2\) and \( \mu_p * C_{ox} = 60 \) \( \mu \)A/V\(^2\) for first iteration. The saturation region current expression helps us in calculating the aspect ratios (W/L) of transistors as the current through them is known and overdrive voltage is assigned (Douglas A.Pucknell et al. 1994)
Here $I_d$ is the biasing current, $\mu_n$ and $C_{ox}$ are process parameters, $W/L$ is the aspect ratio of a transistor, $V_{gs}$ is gate-source voltage and $V_t$ is threshold voltage of device. The circuits were simulated in a 180nm CMOS technology. The OTAs were designed with load capacitances 3.5pF for a 9MHz input signal. The body terminal of all NMOS and PMOS transistors were connected to the $V_{SS}$ and $V_{DD}$, respectively.

4.3 RESULTS AND DISCUSSION

The architecture of the 10 bit 165 MSPS pipelined analog-to-digital converter involves nine cascaded 1.5 bit stages, including the front end sample and hold circuit and the 2-bit Flash ADC which forms the last stage. Each stage performs coarse A/D conversion and computes its quantization error, or residue, which is fed as input to the next stage. The design of each 1.5 bit stage includes a two stage operational transconductance amplifier which is used in the sample and hold circuit as well as the residue amplifier in the MDAC of each 1.5 bit stage, the dynamic comparators that forms the sub-ADC and the sub-ADC circuit whose outputs are fed as inputs to the MDAC circuit. The residue voltage generated from each stage is then fed as inputs to the next stage. The various sub blocks including OTA, Sub-DAC, Sub-ADC, 2-bit Flash ADC, Dynamic comparator and digital error correction logic are simulated.

4.3.1 OTA

Figure 4.12 shows the simulated circuit diagram of the operational transconductance amplifier in cadence. It shows the input signal of $1V_{pp}$ and the simulated output waveform of $1.8V_{pp}$. It consists of a folded cascaded as the first stage with a class AB along with current mirrors as the second stage. The load capacitors were chosen to have values of 3.5 pF each.
Figure 4.12 Operational transconductance amplifier

Figure 4.13 shows the common mode feedback circuit. Its inputs are the two inputs of the OTA and its output is the $V_{cmfb}$ voltage. This circuit amplifies the difference between the average of the outputs and the common mode input signals.

Figure 4.13 CMFB circuit
Figure 4.14 Transient analysis of OTA

Figure 4.14 shows the transient analysis of OTA. It shows the input signal of $1V_{pp}$ and the simulated output waveform of $1.8V_{pp}$. Figure 4.15 shows the AC analysis of OTA. The AC analysis shows the gain of 42.69dB. The power consumption of this OTA is 2.46mW.

Figure 4.15 AC analysis of OTA

The Common-Mode Rejection Ratio (CMRR) of a differential amplifier is the tendency of the device to reject the input signals common to both input leads. The obtained CMRR of the OTA is 98dB. The Power Supply Rejection Ratio (PSRR) is defined as the ratio of the change in supply voltage to the
equivalent (differential) input voltage it produces in the op-amp, often expressed in decibels. An ideal op-amp would have infinite PSRR. PSRR for any analog circuit is the measure of its immunity to power supply changes. The PSRR for the OTA is shown in Figure 4.16. The PSRR for the two stage OTA is 58dB.

![Figure 4.16 PSRR of OTA](image)

The settling time of an amplifier is the time elapsed from the application of an ideal instantaneous step input to the time at which the amplifier output has entered and remained within a specified final value. The settling time of the OTA is 1µs. Table 4.1 shows the performance summary of OTA.

**Table 4.1 Performance summary of the OTA**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input range</td>
<td>$1 \text{ V}_{pp}$ differential</td>
</tr>
<tr>
<td>Power supply</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Load capacitor</td>
<td>3.5pF</td>
</tr>
<tr>
<td>Technology</td>
<td>180 nm</td>
</tr>
<tr>
<td>DC gain</td>
<td>42.68 dB</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>2.46mW</td>
</tr>
<tr>
<td>Settling time</td>
<td>1µs</td>
</tr>
<tr>
<td>PSRR</td>
<td>58 dB</td>
</tr>
<tr>
<td>CMRR</td>
<td>98 dB</td>
</tr>
</tbody>
</table>
4.3.2 Sample and hold circuit

The accuracy and speed of ADC critically depends on the performance of front-end sample and hold. The sample and hold needs to acquire a wideband input signal, and drive the large load capacitance of the next stage with low distortion. This has to be achieved without adding too much of noise or consuming high power. The output voltage of the SHA is 1.6V. The total power consumption of this circuit is 4.87mW. It has a sampling rate of 165 MSPS. The double sampling increases the sampling rate and reduces the power consumption by increasing the settling time of amplifier.

![Output waveform of the sample and hold circuit](image)

**Fig 4.17 Output waveform of the sample and hold circuit**

Figure 4.17 shows the simulated waveforms of the skew insensitive sample and hold circuit. The input voltage applied to the SHA is 1V.
Figure 4.18 Schematic of dynamic comparator

Figure 4.18 shows the schematic of the dynamic comparator. Figure 4.19 shows the output of the dynamic comparator. From the waveform it is clear that when the input signal is above the reference voltage the output pulse goes high, otherwise it remains at low.

4.3.3 Sub-ADC

Function of the sub-ADC is to quantize the input signal and provide the intermediate bits for each stage. For 1.5 bits per stage architecture sub-ADC
can have one of the three binary states as an output: 00, 01, 10. The output waveform goes high when the input voltage is above the reference voltage levels. These outputs are sent to logic block. This logic block with the sub-DAC will generate the three allowable binary states for a 1.5 bit per stage architecture. Figure 4.20 shows the schematic of sub-ADC.

![Figure 4.20 Schematic of sub-ADC](image)

Figure 4.21 shows the transient response of sub-ADC. The input to the subADC is 1.0 V_{pp} analog signal and the output obtained is the digital output. Table 4.2 lists the outputs of the two dynamic comparators which forms the sub-ADC.

![Figure 4.21 Transient response of sub-ADC](image)
Table 4.2 Output of sub-ADC

<table>
<thead>
<tr>
<th>Condition</th>
<th>$V_{outp1}$</th>
<th>$V_{outn1}$</th>
<th>$V_{outp2}$</th>
<th>$V_{outn2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in} &gt; V_{ref}$</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$-\frac{V_{ref}}{4} &gt; V_{in} &gt; \frac{V_{ref}}{4}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V_{in} &lt; \frac{V_{ref}}{4}$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

4.3.4 Sub-DAC

The role of the sub-DAC is to supply the gain stage with the analog voltage level that represents the quantized portion of the input sample. The quantized portion is subtracted from the input signal to create a residue that will be sent to the next stage. The sub-DAC calculates the digital word for that stage according to the outputs from the sub-ADC. For architecture with 1.5 bits per stage, the sub-ADC can have one of the three binary outputs: 00, 01, and 10. These correspond to the sub-DAC outputs of $-\frac{V}{2}$, 0, $+\frac{V}{2}$ respectively. Figure 4.22 shows the schematic of the sub-ADC along with the sub-DAC and Figure 4.23 shows the output waveform of the sub-DAC.
Figure 4.23 Transient analysis of sub-DAC

Figure 4.23 depicts the transient analysis of sub-DAC in which the input digital signal is converted into analog signal of 1V.

4.3.4 MDAC

The performance of pipeline ADC critically depends on the multiplying-digital-to-analog converter (MDAC). In the double sampling MDAC two parallel sets of capacitors are used to increase the speed. These two parallel paths are controlled by opposite phase clocks. The switches are implemented by transmission gates. During the first phase capacitor $C_{S1^+}, C_{F1^+}$ and $C_{S1^-}, C_{F1^-}$ are charged to the input voltage and $C_{F2^+}$ and $C_{F2^-}$ are connected in feedback. $C_{S2^+}$ and $C_{S2^-}$ are connected to a proper reference voltage generated by sub-DAC which is determined by the digital output of sub-ADC. Figure 4.24 shows the schematic of the double sampling MDAC circuit. Figure 4.25 shows the schematic of op-amp sharing MDAC.
The switched capacitor architecture of the third stage of pipelined ADC matches the double sampling stages (stage 1 and stage 2) with the next stages. In other words, the holding time for outputting the signals from stage 2 to stage 3 is the same as a conventional stage using the double sampling technique, while the amplifiers of stages 3 to 8 are shared between two adjacent stages and are twice as fast as the double sampling stages.
The sub-ADC block along with the MDAC and front end sample and hold circuit forms the first 1.5 bit stage of the 10 bit pipelined ADC.

Figure 4.26 First 1.5 bit stage of 10 bit pipelined ADC

Figure 4.27 Transient response of first stage of 10- bit pipelined ADC

Figure 4.26 shows the 1.5 bit stage of 10-bit pipelined ADC. The front-end sample and-hold (SH) and the first three stages use the double sampling (DS) technique. Figure 4.27 shows the transient response for the first
1.5 bit stage of the 10 bit pipelined ADC. As shown in transient response the MSB and LSB are generated by comparing the input voltage of 1V for each stage i.e. the residue from the previous stage with reference voltages of the comparators in the sub-ADC.

### 4.3.5 2-bit Flash ADC

The final stage of the pipeline ADC is a 2-bit Flash ADC. This 2-bit flash ADC resolves the last two bits of the ADC since the 1.5-bit stage calibration cannot be used on the final stage because there is no following stage. Figure 4.28 shows the schematic of the 2-bit Flash ADC used as the last stage of a pipelined ADC. The Flash ADC uses a resistive ladder that divides the reference voltages, which are then compared with the input voltage by the comparators. The comparator outputs are followed by a 4 to 2 decoder which generates the MSB and the LSB. The output pulses rise to the high values only when the input voltage is greater than the reference voltage. The power consumption of this circuit is only about 6.022nW. Figure 4.29 shows the output waveform of 2-bit Flash ADC in which analog input of 1V_{pp} is converted into digital output.

![Figure 4.28 Schematic of 2-bit Flash ADC](image)
4.3.6 Digital error correction logic

To correct the output of analog chain, delay elements and full adders are included as the digital correction. Although each stage generates 2-bit of output codes, they are not time synchronous. Every output of single stage is delayed by half of clock cycle compared to its previous stage. This delay should be compensated before adding them together. Flip-flop is used as delay element. Figure 4.30 shows the digital error correction logic used in the design.
4.3.7 10-bit pipelined ADC using DS and op-amp sharing technique

Figure 4.31 shows all the stages of the 10 bit pipelined ADC integrated together to generate 18 sets of LSBs and MSBs. This code has to be then corrected using the digital error correction logic to obtain the final 10 bit output of the pipelined ADC. As shown in Figure 4.32 the input analog signal of $1V_{pp}$ input differential signal is converted into 10-bit digital outputs.
Lesser power dissipation is a very important factor in any design. This design has a power dissipation of only 22mW. A 10 bit ADC is supposed to produce 10 bit output codes with exactly $2^n$ i.e. $2^{10}$ (1024) combinations, each combination corresponding to a small value of the total full scale input range. Here, the full scale input range is 2V. So the voltage magnitude corresponding to 1 LSB is calculated using the formula

$$ V_{\text{LSB}} = \frac{\text{FSR}}{2^{10}} $$

$$ = \frac{2V}{1024} = 1.9\text{mV}. $$

FSR is the full scale range. It means that for every 1.9mV change in the input voltage magnitude, the 10-bit digital code should change. The 10 bit pipelined ADC was designed and implemented in 180nm CMOS process with a differential input signal of 1V$_{\text{pp}}$, 9MHz input frequency, and the supply voltage of 1.8V. Simulation results show that the obtained power consumption of the 10-bit 165MSPS ADC is 22mW at 1.8V supply voltage. Differential non linearity (DNL) is the deviation in the width of a certain code from the value of 1LSB. The obtained differential non-linearity (DNL) is illustrated in Figure 4.33. The DNL is within +0.41/-1 LSB and the INL is within +0.6/-1 LSB at 165 MSPS.

![Figure 4.33 DNL plot](image)
The obtained integral- nonlinearity (INL) is illustrated in Figure 4.34.

![INL plot](image)

**Figure 4.34 INL plot**

The obtained output fast Fourier transform (FFT) spectrum with a 9 MHz sinusoidal input at 1.8 V and 165 MSPS is plotted in Figure 4.35. The obtained SFDR is about 64 dB, the SNDR is about 56.10 dB, Figure of merit is 0.25 pJ/step and the ENOB is about 9.0256. The obtained dynamic performance versus input frequency is shown in Figure 4.36 and Figure 4.37.
The ADC is designed in a 180nm CMOS process and achieves 22 mW power consumption for a 1 V differential input signal and 9 MHz input frequency from a 1.8 V supply. From the results it was observed that this 10 bit pipelined ADC was suitable for video applications. Figure 4.38 shows the layout of 10-bit pipelined ADC using DS and op-amp sharing technique.

Table 4.3 shows the performance summary of 10-bit pipelined ADC and Table 4.4 shows the comparison of designed pipelined ADC with reported ADCs.
Figure 4.38  Layout of 10- bit pipelined ADC using DS and op-amp sharing technique

Table 4.3 Performance summary of 10 bit pipelined ADC using DS and op-amp sharing technique

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
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<tr>
<td>Power supply</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Input frequency</td>
<td>9 MHz</td>
</tr>
<tr>
<td>Input range</td>
<td>1V\text{pp}</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>22mW</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>165 MSPS</td>
</tr>
<tr>
<td>DNL/INL</td>
<td>+0.41/-1 /0.6/-1 LSB</td>
</tr>
<tr>
<td>SFDR</td>
<td>64 dB</td>
</tr>
<tr>
<td>SNDR</td>
<td>56.1dB</td>
</tr>
<tr>
<td>FOM</td>
<td>0.25\text{pJ/step}</td>
</tr>
<tr>
<td>Conversion time</td>
<td>10\text{ns}</td>
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### Table 4.4 Comparison of designed pipelined ADC with reported ADCs

<table>
<thead>
<tr>
<th>Reference</th>
<th>Technology (nm)</th>
<th>Supply Voltage (V)</th>
<th>Resolution (bits)</th>
<th>Sample Frequency (MSPS)</th>
<th>Power (mw)</th>
<th>SNDR (dB)</th>
<th>SFDR (dB)</th>
<th>ENOB (bits)</th>
<th>DNL/INL (LSB)</th>
<th>FOM (PJ/Conv./step)</th>
<th>Area (mm²)</th>
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</thead>
<tbody>
<tr>
<td>Yong-Inpark et al. (2001)</td>
<td>180</td>
<td>1.8</td>
<td>10</td>
<td>80</td>
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<td>-</td>
<td>64.8</td>
<td>9.20</td>
<td>0.66/+0.33/-0.76/+0.76</td>
<td>-</td>
<td>2.55</td>
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<tr>
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<td>10</td>
<td>150</td>
<td>123</td>
<td>52.0</td>
<td>65.6</td>
<td>-</td>
<td>0.69/1.5</td>
<td>-</td>
<td>2.20</td>
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<td>Jian Li et al. (2008)</td>
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<td>57.4</td>
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<td>9.10</td>
<td>0.57/0.8</td>
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<td>0.70</td>
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<td>1.2</td>
<td>10</td>
<td>165</td>
<td>56</td>
<td>-</td>
<td>-</td>
<td>9.00</td>
<td>0.56/-0.49/1.03/-0.72</td>
<td>0.78</td>
<td>0.15</td>
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<td>100</td>
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<td>58.7</td>
<td>65</td>
<td>9.50</td>
<td>0.61671/0.315</td>
<td>-</td>
<td>0.24</td>
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<tr>
<td>Andrew et al. (2013)</td>
<td>180</td>
<td>1.8</td>
<td>10</td>
<td>100</td>
<td>28.3</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1105 fJ/conv. step</td>
<td>0.30</td>
</tr>
<tr>
<td>Present Work</td>
<td>180</td>
<td>1.8</td>
<td>10</td>
<td>165</td>
<td>22.0</td>
<td>56.1</td>
<td>64</td>
<td>9.02</td>
<td>-1/+0.41/-1/+0.6</td>
<td>0.25</td>
<td>0.36</td>
</tr>
</tbody>
</table>

### 4.4 SUMMARY

This work describes a 10 bit 165MSPS pipelined analog to digital converter for HDTV and high frame rate video instruments application. The proposed architecture employs both double sampling and operational amplifier sharing techniques in the MDAC circuits for power reduction. The subcircuits of various stages were integrated to form the single bit stage which was then cascaded to form the 10 bit pipelined ADC. A 2-bit Flash ADC which is used as the last stage of the 10 bit pipelined ADC was designed using a resistor divider branch and three clocked dynamic comparators. To correct the output of analog chain which generates 18 bits, delay elements and full adders are included as the digital correction which generates the final 10 bit output. Results for power are compared with the reported value in (Martin et al. 2008) and 60% of power reduction was achieved. Since this ADC achieves a very good FOM and conversion time this ADC is very suitable for high performance video applications.