CHAPTER 3

MODIFIED FULL BRIDGE ZERO VOLTAGE SWITCHING DC-DC CONVERTER

3.1 INTRODUCTION

This chapter introduces the Full Bridge Zero Voltage Switching (FBZVSC) converter. Operation of the circuit is explained. Design procedure is presented. Simulation and experimental results are presented to support the design procedure.

Section 3.2 introduces the modified Full Bridge Zero Voltage Switching converter. Design procedure is explained in section 3.4. Simulation and experimental results are presented in section 3.5 and 3.6 respectively.

3.2 FULL BRIDGE ZERO VOLTAGE SWITCHING DC-DC CONVERTER

The Full Bridge Zero Voltage Switching converter (FBZVSC) is shown in Figure 3.1. By adding a simple external commutating aid circuit to the full bridge DC-DC converter with phase shift control and by reducing the magnetizing inductance, optimum performance can be obtained. ZVS operation and high conversion efficiency can be achieved from full load down to almost zero load. Constant-frequency, phase-shifted operation of the primary side switches provides a convenient method for achieving zero-voltage turn on of the switches, which significantly reduces switching losses.
The Full Bridge Zero Voltage Switching converter consists of a DC source, an inverter, an isolation transformer, an uncontrolled bridge rectifier, an inductor, a capacitor and the load. The DC input is inverted; high frequency AC voltage is fed to uncontrolled bridge rectifier through isolation transformer. The output of rectifier is fed to LC resonating circuit and henceforth to the load.

The ZVS energy stored in the primary inductor is dependent on its inductance value and the volt-second product of the secondary of the auxiliary transformer T. The size of the primary inductor can be minimized by properly selecting the turns ratio of the auxiliary transformer T. The size of the primary inductor is very much reduced, compared to that of the conventional PS FB converter. Because of the energy used to create the ZVS condition at light loads is not stored in the leakage inductances of the transformer T, The transformer’s leakage inductances can also be minimized. As a result of the reduced total primary inductance (the inductance of the primary inductor used for ZVS energy storage and the leakage inductance of the power transformer, FBZVS converter exhibits a relatively small duty cycle loss. It minimizes the conduction loss of the primary switches, the voltage stress on the components in the secondary side of the transformer, and improves the conversion efficiency. Due to reduced total primary inductance, the secondary side

Figure 3.1 FBZVS DC-DC Converter
parasitic ringing is also reduced and is effectively controlled by the primary side diodes D₁ and D₂.

### 3.3 OPERATING PRINCIPLE

Modified Full Bridge Zero Voltage Switching converter is shown in Figure 3.2.

![Figure 3.2 Modified FBZVS DC-DC Converter](image)

Modified FBZVS DC-DC converter employs a series inductor and two capacitors to achieve zero voltage switching. The differences between the modified and conventional FBZVS converter are as follows.

- The DC blocking capacitor of conventional converter is split into two capacitors, $C_{dc1}$ and $C_{dc2}$, in the modified circuit.
- The conventional converter uses a single high-frequency transformer, whereas it is divided into two transformers $T_{x1}$ and $T_{x2}$ (with primary-to-secondary turns ratio of $N:1$) in the modified circuit.
The modified circuit has additional inductor $L_a$ which adaptively stores additional energy for ZVS operation when the stored energy transformer leakage is inadequate.

The secondary windings of the transformers are connected in series. The leakage inductances of both the transformers are shown in Figure 3.2 as a lumped inductor $L_0$ in series with secondary windings. Figure 3.3 shows the operation principle waveforms of modified FBZVS. The diodes, inductors and capacitor $C_0$ together act as current doubler and the same inductor and capacitors act as filters. $R$ is the load resistance. By using the series connected primary winding, DC blocking capacitor and a saturable inductor the primary current can be reduced to zero. The conventional FBZVS has limited range. When load current is low the ZVS is lost as the energy stored in the leakage inductance of the transformer is insufficient to discharge the switch and transformer capacitances. While extending the range of ZVS operation, the full load conduction loss increases. The main power transformer is divided into two half rated transformers and an uncoupled inductor to achieve ZVS over entire conversion range. The converter is suitable over wide range and load resistance is varied.

The converter is analyzed for low power, varying load resistance and high frequency. When duty cycle is high, the load current is high. Energy stored in transformer leakage inductance is sufficient for ZVS operation. Auxiliary current is low thereby causing low additional conduction losses. When duty cycle is low, load current is low and energy in transformer leakage inductance is insufficient for ZVS operation. Hence Auxiliary current increases and assists to achieve ZVS operation from full load to approximately 35% of load. At low power the auxiliary current is circulates in all the four switches causing more conduction loss.
By properly selecting the duty cycle for the switches, optimal values for resonant components the efficiency of modified FBZVS at light loads can be improved. The operation of the circuit is divided into four modes.

Figure 3.3 Operation principle waveforms of modified FBZVS

Mode-1 \([t_0,t_1]\)

The MOSFETs \(M_1\) and \(M_2\) are turned on. In steady state the output capacitor \(C_o\) is charged. The current in the input side flows through \(M_1\), primary, \(M_4\) and back to the source. In the secondary side the diodes \(D_1\) and \(D_4\) conduct and the energy is transferred to the output capacitor.

Mode-2 \([t_1,t_2]\)

The pulse to \(M_4\) is withdrawn and the driving pulse is given to \(M_3\) along with \(M_1\). The charging started in the primary circulates current through the MOSFETs \(M_1\) and \(M_3\). \(D_1\) and \(D_4\) continue to conduct in the secondary side.
Mode-3 \([t_2,t_3]\)

The pulse to \(M_1\) is withdrawn and pulse is applied to \(M_2\) along with \(M_3\). The diodes \(D_1\) and \(D_4\) continue to conduct due to the energy in the filter inductance. The diodes \(D_2\) and \(D_3\) conduct due to the forward bias given by the secondary of the transformer. This is called period of overlap. \(D_1\) and \(D_4\) get turned off by the end of this mode.

Mode-4 \([t_3,t_4]\)

The pulse to \(M_3\) is withdrawn and pulse is applied to \(M_4\). The energy in the primary circulates current. Through the devices \(M_2\) and \(M_4\) diodes \(D_2\) and \(D_3\) continue to conduct.

3.4 DESIGN PROCEDURE

The proposed converter is designed for the following specifications:

**Table 3.1 Design parameters of modified FBZVS**

<table>
<thead>
<tr>
<th>Input Voltage (V_i)</th>
<th>48V</th>
<th>Input Power</th>
<th>48w</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage (V_o)</td>
<td>12 V</td>
<td>Time period</td>
<td>26(\mu)s</td>
</tr>
</tbody>
</table>

Resonant Frequency = 38 kHz

The design values are as follows for the above specification.

\[ s = \frac{V_o}{V_i} \quad (3.1) \]

\[ s = 12/48 = 0.25 \]
Power is given by

\[ P_o = \frac{V_o^2}{R} \]  

Therefore Resistance value is given by

\[ R = \frac{V_o^2}{P_o} = 4\Omega \]  

\[ T_s = \frac{1}{f_s} \]  

\[ T_s = \frac{1}{f_s} = 2.6 \times 10^{-4} \text{ sec} \]  

\[ L_1 = \frac{T_s(1-s)R}{2} \]  

The value of \( L_1 \) is 39 \( \mu \text{H} \)

Transformer design

\[ E_1 = 4.44 \times N_1 \times \phi_m \times f \]  

\[ E_1 = 48 \text{ V}, N_1 = 60, \phi_m = 10 \mu\text{wb} \]

Number of turns in the primary winding \( N_1 = 28 \)

\[ E_2 = 4.44 \times N_2 \times \phi \times f \]  

\[ N_2 = \frac{E_2}{E_1} \times N_1 \]

Number of turns in the secondary winding \( N_2 = 7 \)

Ripple factor \( r = 4\% \)

Ripple factor(\( r \)) is given by
\[ r = \frac{1}{4\sqrt{3}fCR} \]  \hspace{1cm} (3.8)

\[ 0.04 = 1 / 4 \sqrt{3}.f .C.R \]

\[ C = 23 \mu F \]

\[ f_s = \frac{1}{2\pi\sqrt{LC}} \]  \hspace{1cm} (3.9)

\[ L = 0.75 \mu H \]

\[ r = \frac{\sqrt{3}}{\omega^2 L_0 C_0} \]  \hspace{1cm} (3.10)

Therefore \( L_o = 3.6 \mu H \)

\( I_o = 3 \text{ A} \)

Conduction losses \( w_c = 2 \). \( V_o s.I_D = 1.5 \text{ w} \)  \hspace{1cm} (3.11)

Conduction Loss in diode = 0.7 \( I_o \)

Iron loss \( w_i = 2\% \) of the rated power = 0.72w

\[ \eta = \frac{V_o I_o}{V_o I_o + w_c + w_i} \]  \hspace{1cm} (3.12)

Therefore Converter efficiency \( \eta = 94\% \)

### 3.5 SIMULATION RESULTS

The simulation is carried out using MATLAB/Simulink. The simulation circuit is shown in Figure 3.4. Input voltage is 48V DC which is shown in Figure 3.5. The Driving pulses, transformer’s primary winding voltage, DC output voltage and current are also shown in Figure 3.5.
The driving pulse, current and voltage of switch $S_1$ is shown in Figure 3.6. The driving pulse, current and voltage of switch $S_4$ is shown in Figure 3.7. Figure 3.6 shows the $S_1$’s driving signal gate-source voltage, drain-source voltage and the current flowing through drain-source. It can be observed $I_{ds3}$ is negative before the arrival of the driving signal, which assures that $V_{ds1}$ decreases to zero before the switch turning on and achieves ZVS. From Figure 3.7 it is observed that the voltage from drain to source of $S_4$ decreases to zero before the switch turns on and achieves ZVS. Hence turn-off loss is negligible. Figure 3.8 shows the output voltage and output current. The switching frequency is 38.3 kHz.

Table 3.2 Simulation parameters of modified FBZVS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC input voltage</td>
<td>48V</td>
</tr>
<tr>
<td>$L_a$</td>
<td>32 $\mu$H</td>
</tr>
<tr>
<td>Resonant frequency</td>
<td>38 kHz</td>
</tr>
<tr>
<td>$C_{dc1}$</td>
<td>1 $\mu$F</td>
</tr>
<tr>
<td>$C_0$</td>
<td>470 $\mu$F</td>
</tr>
<tr>
<td>$C_{dc2}$</td>
<td>1 $\mu$F</td>
</tr>
<tr>
<td>$R_0$</td>
<td>4 $\Omega$</td>
</tr>
<tr>
<td>$L_0$</td>
<td>10 $\mu$H</td>
</tr>
</tbody>
</table>
Figure 3.5 Simulation waveforms of modified Full bridge ZVS

Figure 3.6 (a) Driving pulse, (b) current and (c) voltage across switch1
DC output voltage is found to be 12V and the current is 3.05A. There is no overlapping between voltage and current wave forms. Hence the conduction losses are minimized. DC output voltage and current are free from ripple.

The load is varied from 35.5% to 100% and the performance of the converter is observed and tabulated. Table 3.3 shows the performance of the modified FBZVS for changes in % of load. Table 3.4 shows the performance of the modified FBZVS for changes in input voltage.
### Table 3.3  Performance of the modified FBZVS DC-DC converter for changes in load

<table>
<thead>
<tr>
<th>% of load</th>
<th>Output voltage(V)</th>
<th>Output current(A)</th>
<th>Output power(w)</th>
<th>Input power(w)</th>
<th>Efficiency(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>35.5</td>
<td>12.55</td>
<td>0.64</td>
<td>8.03</td>
<td>9.77</td>
<td>82.21</td>
</tr>
<tr>
<td>50</td>
<td>12.48</td>
<td>0.83</td>
<td>10.36</td>
<td>12.40</td>
<td>83.54</td>
</tr>
<tr>
<td>62.5</td>
<td>12.3</td>
<td>1.4</td>
<td>17.22</td>
<td>20.38</td>
<td>84.5</td>
</tr>
<tr>
<td>75</td>
<td>12.23</td>
<td>2</td>
<td>24.46</td>
<td>28.74</td>
<td>85.1</td>
</tr>
<tr>
<td>87.5</td>
<td>12.1</td>
<td>2.52</td>
<td>30.49</td>
<td>35.66</td>
<td>85.49</td>
</tr>
<tr>
<td>100</td>
<td>12</td>
<td>3.05</td>
<td>36.6</td>
<td>42.7</td>
<td>85.71</td>
</tr>
</tbody>
</table>

### Table 3.4  Performance of the modified FBZVS DC-DC converter for changes in input voltages

<table>
<thead>
<tr>
<th>Input voltage (V)</th>
<th>Input current (A)</th>
<th>Input power (w)</th>
<th>Output voltage (V)</th>
<th>Output current (A)</th>
<th>Output power (w)</th>
<th>Efficiency(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>0.66</td>
<td>26.4</td>
<td>11.5</td>
<td>1.93</td>
<td>22.2</td>
<td>84.09</td>
</tr>
<tr>
<td>44</td>
<td>0.82</td>
<td>36.08</td>
<td>11.95</td>
<td>2.56</td>
<td>30.62</td>
<td>84.87</td>
</tr>
<tr>
<td>48</td>
<td>0.89</td>
<td>42.72</td>
<td>12</td>
<td>3.05</td>
<td>36.6</td>
<td>85.67</td>
</tr>
<tr>
<td>52</td>
<td>0.94</td>
<td>48.88</td>
<td>12.3</td>
<td>3.42</td>
<td>42.06</td>
<td>86.04</td>
</tr>
</tbody>
</table>
From Figure 3.9 and 3.10 it is observed that the output voltage varies slightly with respect to input voltage and output power increases with increase in input voltage. From Figure 3.11 it is observed that efficiency is flat over the entire range of input voltage.
From Figure 3.14 it is evident that the efficiency at light load is improvised than conventional converter.
### 3.5.1 Comparison of Open Loop System with Closed Loop System with Step Change in Input Voltage

The simulink model of open loop system is shown in Figure 3.15. A step change in voltage is applied at the input. The DC input voltage, output current, and output voltage with input step change is shown in Figure 3.16. When input voltage is increased to a value of 60V at 0.4s, the output voltage also increases and settles at new value of 15V.

![Figure 3.15 Open loop system with step change in input](image1)

![Figure 3.16 Results of open loop system with step change in input](image2)

(a) Input voltage (b) Output current (c) Output voltage
The simulink model of closed loop system is shown in Figure 3.17. In order to maintain the required output voltage level, closed loop control is used. The instantaneous voltage signal is taken from the output and given to a comparator. Other input to the comparator is the set voltage of 12V. Output of the comparator is the error signal which is given to the PI controller. The output of PI controller is compared with a reference triangular wave form of peak value 17 and time period 0.1ms to generate PWM waves as shown in Figure 3.19. They are used as control signals for the gates of MOSFETs S1 to S4. The DC input voltage, output current, and output voltage with input step change are shown in Figure 3.18. The parameters of PI controller are shown in Table 3.5.

Figure 3.18 Results of closed loop system with step change in input
(a) Input voltage (b) Output current (c) Output voltage
The step change is applied at 0.4 seconds for open loop system as shown in Figure 3.15. From Figure 3.16 it is observed that the open loop system has steady state error and its peak value is 15V. For the closed loop system shown in Figure 3.17, the input voltage is increased to 60V at 0.4 seconds. From Figure 3.18 it is observed that the control circuit takes proper action and the output voltage is maintained at 12V. Set voltage is taken as 12V. The closed loop system reduces the steady state error. It settles at 0.72s. The settling time is 0.32s.

Figure 3.19 a. PI controller output b. Reference voltage c. PWM waves

<table>
<thead>
<tr>
<th>Parameters of PI controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proportional gain($K_p$)</td>
</tr>
<tr>
<td>Integral gain($K_i$)</td>
</tr>
<tr>
<td>Output limits</td>
</tr>
<tr>
<td>Sample time</td>
</tr>
</tbody>
</table>
3.5.2 Comparison of Open Loop System with Closed Loop System for Output Load Regulation

The simulink model of open loop system without output load regulation is shown in Figure 3.20. Input voltage is 48V DC. A breaker is connected in parallel with the load. Load resistance is 4Ω. The breaker is opened at initial state and it is closed at 0.4s. DC output voltage is shown in Figure 3.21 where the output voltage is increased at 0.4s due to change in the load.

![Figure 3.20 Open loop system without output load regulation](image)

**Figure 3.20** Open loop system without output load regulation

![Figure 3.21 DC output voltage with step change in load](image)

**Figure 3.21** DC output voltage with step change in load
The simulink model of closed loop system for output load regulation is shown in Figure 3.22. Input voltage is 48V DC. Set voltage is 12V DC. In order to maintain the required output voltage level, closed loop control is used. The instantaneous output voltage signal is given to a comparator. Other input to the comparator is the set voltage. Output of the comparator is the error signal which is given to the PI controller. The output of PI controller is compared with a triangular reference signal to generate gate pulses. They are used as control signals for the gates of MOSFETs $S_5$ and $S_6$.

Figure 3.22 Closed loop system with output load regulation

Figure 3.23 DC output voltage of closed loop system
The breaker is opened at initial state and it is closed at 0.4s. When the breaker is closed, due to load side disturbance the output voltage increases to a value of 13.9V. But the closed loop system settles the output voltage to a value of 12V at 0.8s as shown in Figure 3.23. The settling time is 0.4s.

3.6 EXPERIMENTAL RESULTS

The DC-DC converter was built and tested for open loop modified FBZVS at 48 V DC. The hardware layout is shown in Figure 3.24. The circuit parameters are as follows.

**Table 3.6 Experimental parameters of modified FBZVS**

<table>
<thead>
<tr>
<th>L_a</th>
<th>32 µH</th>
<th>R_0</th>
<th>4 Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_0</td>
<td>470 µF</td>
<td>L_0</td>
<td>10 µH</td>
</tr>
</tbody>
</table>

The switching frequency is 38.3 kHz. The pulses are generated using 89C2051. Crystal and two capacitors are connected externally. The pulses are amplified using the driver IR 2110. Each driver is capable of driving two MOSFETs. Two drivers are required to control four MOSFETs. Experimental waveform of driving pulses of switch3 and switch1 is shown in Figure 3.25. Driving pulses of switch4 and switch2 is shown in Figure 3.26. The primary side voltage of the transformer is shown in Figure 3.27. The secondary side voltage of the transformer is shown in Figure 3.28. Load voltage waveform is shown in Figure 3.29 and the output voltage is shown in Figure 3.30. The output voltage is 12V.
Figure 3.24. Hardware layout of modified FBZVS DC-DC converter

Figure 3.25 (a) Driving pulses of MOSFET3 (b) Driving pulses of MOSFET1
Figure 3.26 (a) Driving pulses of MOSFET4 (b) Driving pulses of MOSFET2

X axis 1 div = 10 µs; Y axis 1 div = 20V

Figure 3.27 Primary side voltage of the transformer
X axis 1 div = 10µs. Y axis 1 div = 10V

**Figure 3.28 Secondary side voltage of the transformer**

X axis 1 div = 10µs, Y axis 1 div = 10V

**Figure 3.29 Load voltage waveform**
Figure 3.30 Output voltage across the load

The output voltage across the load from open loop experimental result is 12V and the output voltage from simulation result is 12V. Hence the experimental results closely agree with the simulation results.

3.7 SUMMARY

Modified FBZVS DC to DC converter is modeled using the blocks of simulink. Soft switched FB ZVS DC to DC converter is analysed, simulated, tested and the results are presented. The converter is designed for low power, varying load resistance and high frequency conditions. When duty cycle is low, load current is low and energy in transformer leakage inductance is insufficient for ZVS operation. Hence the auxiliary current increases and assists to achieve ZVS operation from full load to approximately 35% of load. At light loads the auxiliary current is circulating in all the four switches causing more conduction loss. By properly selecting the duty cycle for the switches, optimal values for resonant components the efficiency of modified FBZVS at low load is improved and it is found to be 85.71% at full load and
82.21% at 35.5% of load. Switching losses and stresses are reduced using zero voltage switching over entire conversion range. The experimental results closely agree with the simulation results. In order to maintain the required output voltage level, a closed loop circuit model was developed, and it was used for simulation studies. It is observed that the control circuit takes proper action to reduce the peak amplitude from 15V to 12V. The closed loop system reduces the steady state error and settles at 0.72s. The Settling time is 0.32s.