CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

Multilevel power conversion technology is evolved initially from the need for reducing the THD in the output voltage of the inverter. Later it is implemented practically to serve the need for realizing inverters driven from high-voltage dc buses. The switching devices have been either very highly stressed or lacking sufficient voltage rating to realize high voltage and high power converters. By using multilevel structures, the stress on each switching device can be proportionally decreased. Thus a high voltage dc bus can be handled without using hefty and lossy step up / down transformers. Hence, MLI can be used in the grid connected RE applications without the user of bulky transformers. This chapter presents an overview of various MLI topologies proposed in the literature to synthesize staircase (multilevel) waveforms.

At given environmental conditions (mainly dependent on temperature and insolation level for PV cells), PV cells supply maximum power at a particular operating points—the MPP. Unlike conventional (fueled) power sources, it is desirable to operate PV energy conversion systems at their MPP. However, the MPP locus varies over a wide range, depending on the environmental conditions. This chapter presents various methods available in the literature to track the MPP.
2.2 REVIEW ON MULTILEVEL INVERTERS

The topologies of MLI can be classified into six categories, based on their basic structural differences. Delegated examples from each group are illustrated and described in the following sections.

2.2.1 Configurations with Diode Clamps

Usually, the oldest reference in multilevel power conversion literature is found in the works of Nabae et al who invented the Neutral-Point-Clamped MultiLevel Inverter (NPCMLI) in 1981(Figure 1.9). It has been demonstrated that the resultant three-level PWM waveform has appreciably lesser THD when compared with the traditional Voltage Source Inverter (VSI). Later, the same principle of clamping the intermittent levels with diodes is extended to higher number of levels (Choi et al 1993; Carpita & Tenconi 1991). Such multilevel structures are generically known as 'Diode Clamped Multilevel Inverters'(DCMLI). These MLI not only improves the waveform quality, but also reduces voltage stress on the devices. This stress reduction is directly proportional to the number of levels.

Although theoretically very attractive, there are three main problems one needs to overcome before one can accomplish a successful practical realization of this topology. First and foremost, these inverters suffer from an inherent problem of capacitor voltage imbalances due to their series connected nature when active power is supplied to the load (Satoshi Ogasawara & Hirofumi Akagi 1993, Menzies et al 1994, Fang Zheng Peng et al 1995, Borondau et al 1997, Newton & Sumner 1997, Dong Ho Lee et al 1998). Hence special concentration and treatment is required to use this approach in practical applications.
Another disadvantage of DCMLI is that the required voltage blocking capability of the clamp diodes is proportional to the level for which they are used to employ clamping action. Hence, several series-connected clamping diodes are required at higher level, which is a typical scenario in utility applications. An interesting pyramid structure as shown in Figure 2.1 which offers a more systematic connection of series connected diodes has been studied in (Yuan et al 1999).

However, it should be noted that the problems encountered by the three level inverter circuit proposed in (Nabae et al 1981) are relatively simple because it can give comparatively easier solution for capacitor voltage imbalance problems. For this reason, the application of DCMLI topology has been growing increasingly. Three-level inverters for high-voltage and high-power ac drive systems have been successfully implemented for industrial applications and is reported in (Yehia TacLros et al 1991, Nakata et al 1994, Katta et al 1995, Jie Zhang 1995).

Figure 2.1 One leg of a five-level DCMLI with series connected clamping diodes arranged in a pyramid.
The problem of unbalanced capacitor voltages appears when the inverter is transferring real power to the load. This is because the charging and discharging times for each capacitor are unequal and vary with the load power factor. Nevertheless, one can use this inverter for utility applications such as reactive power compensation and harmonic filtering which require no real power flow interaction (Nam Choi et al 1993, Yiqiang Chen & Boon-Teck Ooi 1996, Bakari Mwinyiwiwa et al 1997, Yiqiang Chen et al 1997, Victor A burto et al 1997).

An active solution to mitigate the problem of unbalanced capacitor voltages is to employ diode-clamped rectifiers at the utility front end. This enables one to access the intermediate points on the dc bus which aids in controlling their potential, thereby actively controlling the capacitor voltages (Gautam Sinha & Thomas Lipo 1997, Chiharu Osawa et al 1997, Shoji Fukuda & Yasumasa Matsumoto 1997, Kouki Matsuse et al 1999). A combination of PWM rectifier and inverter (also referred to as 'Back-lo-Back Intertie') based on these diode clamped structures is also possible and has proven to be a promising solution for high power ac drive applications (Hideo Okayama et al 1996, Gautam Sinha & Thomas Lipo 1996, Bacigalupo et al 1997, Noriyuki Kimura et al 1997).

One more interesting configuration with cascaded diode-clamped inverters has been investigated (Shoji lida et al 1996). The authors have added a three-level auxiliary diode-clamped structure at the neutral point clamping node of the main three-level inverter (Figure 2.2). This modification results in a five-level leg output and thus enhances the spectral performance of the original topology. However, it should be noted that the component count for a single-phase application is the same as that of a conventional five-level diode-clamped inverter topology.
2.2.2 Configurations With Bidirectional Switch Interconnections

An improvement in the spectral structure of output waveforms using multiple levels reported in (Nabae et al 1980) was presented in the same conference by Pradeep Bhagwat & Stefanovic (1980). This may be the first document which adopted the name 'MLIs' for this class of inverters. However, the structure presented in the paper is topologically different as shown in Figure 2.3. Access to the neutral point is obtained through a bidirectional switch. This bidirectional switch was synthesized in the original paper using a back-to-back connection of thyristors. Note that the required voltage blocking capability of the 'outer' devices is higher than that of the 'inner' devices. Therefore, this topology does not offer an advantage of reduced voltage stress.
The application spectrum of this approach is restricted to low-power applications where harmonic spectrum is the only concern. In the early days of semiconductor development, thyristors were the only reliable available devices to realize high power switches, and considerable effort was spent towards the development of a commutation scheme for these devices. With the advent of high-power Gate Turn-Off (GTO) devices, it is now possible to realize the same structure with modern high-power devices such as Insulated Gate Bipolar Transistors (IGBT). A three-level structure based on this configuration has been reported (William Brumsickle et al 1998). However, the authors use the neutral point clamping only during the switching interval in order to reduce switching stress on the devices. Therefore, it has been named ‘Quasi Three-Level Inverter'.
2.2.3 Configurations with Dedicated Capacitor Banks

One of the disadvantages in using a diode-clamped inverter is that the required voltage blocking capability of the clamping diodes varies with the levels. This may result in the requirement of multiple series diodes at the higher voltage levels. An alternative multilevel structure where the voltage across an open switch is constrained by clamping capacitors instead of clamping diodes has been proposed in 1992 (Meynard & Foch 1992). A representative five-level structure is shown in Figure 1.13. These inverters are commonly known as ‘Flying Capacitor MLIs’. Another advantage of this topology is that there is no unbalanced capacitor voltage problem because of its independent voltage source structure. However, a problem associated with this approach is the requirement of a complicated control strategy to regulate the floating capacitor voltages (Duarte et al 1997). Also one needs increasing numbers of capacitor banks as the number of levels is increased.

2.2.4 Configurations with Multiple Three-Phase Inverters

Multiple low-power three-phase inverters have been used in utility applications through multi pulse converter configurations (IEEE Press 1995). These converters achieve multilevel voltage output through phase shifting of multiple two-level waveforms which are added together vectorically using series-connected transformer secondary windings (Figure 2.4).

![Simplified block schematic of a five-level transformer coupled inverter](image-url)
However, when the number of levels increases beyond three or five this approach becomes difficult to realize due to the requirement of increased numbers of multiple transformer windings. An alternative approach to combining three three-phase inverters to obtain a multilevel output has been discussed (Enjeti et al 1997). The phase shifting is realized by using interconnecting reactances as shown in Figure 2.5. In addition to the requirement of interconnecting reactances, this approach suffers from a complicated control strategy. Moreover, this topology requires eighteen primary power devices but the reported line-line voltage output exhibits only five distinct levels. This is similar to the line-line output of a conventional three-level inverter which also has five distinct levels but employs only twelve primary power devices.

It should be noted that it is not possible to practically combine multiple conventional three-phase VSIs without adding extra interconnecting reactances or transformers which are usually bulky and lossy. In contrast, it is possible to achieve direct interconnection using Current Source Inverters (CSI). Hombu et al 1987 have demonstrated that it is feasible to realize multilevel current waveforms by connecting together multiple three-phase CSIs (Figure 2.6). However, it should be noted that each CSI typically requires a reactor to provide high-impedance source characteristics.

![Figure 2.5 Simplified block schematic of a multilevel inverter realized with three three-phase inverters and interconnecting reactances](image-url)
2.2.5 Configurations with Series Connected Single Phase H-Bridge Inverters

Series connection of single phase H-bridge inverters with multiple dedicated dc buses to realize multilevel waveforms were probably first introduced in 1973 by Bates (Bates 1997). However, the potential of this technology was realized when it was employed for plasma stabilization a decade and a half later. This modular approach has been subsequently extended for three-phase applications. (Fang Zheng Peng et al 1995, Hammond 1997) have presented topologies based on this approach for reactive power compensation and drive applications. In this approach, several full bridge single-phase inverters with dedicated isolated dc bus capacitors / voltage sources are connected together in series to form a high-voltage inverter for each phase of the system.

Figure 1.14 (a) shows two such single-phase H-bridge inverters connected in series to form one leg of the multilevel inverter. The remaining two phases have the same switch configuration and respective independent dc voltage sources. It may be observed that this inverter is capable of synthesizing five distinct voltage levels ($\pm 2V, \pm V, 0$) if all the dc bus voltages
are equal to V. Therefore, the output voltage waveform resembles that of a five-level diode clamped inverter.

A primary advantage of this topology is that it provides flexibility for expansion of the number of levels easily without introducing undue complexity into the power circuit. Also, extra clamping elements are not needed as in the previous cases while requiring the same number of primary switches as in a diode-clamped topology to achieve a given number of (odd) voltage levels. Note that this configuration requires multiple dedicated dc buses which make it an expensive solution. On the other hand, since the dc voltage sources are independent, the problem of capacitor voltage balancing is eliminated. It is difficult to synthesize a rectifier-inverter combination based on this approach owing to modulation problems. Therefore, the application spectrum of this topology is somewhat limited (Jih-Sheng Lai & Fang Zheng Peng 1997). It has been repeatedly claimed that these circuits are more useful for utility applications like Static VAR Compensators (SVC) and active filters rather than high-power ac drives. However, one finds successful industrial implementation of such inverters in medium-voltage drive applications (Peter Hammond 1997, Richard Osman 1995).

2.2.6 Configurations with Voltage Doublers

Voltage doubling using diodes and capacitors has been a common practice to achieve voltage amplification. A four-level inverter (however called three-tier waveform synthesizer) has been introduced by Baker (Richard Baker 1979). A simplified schematic of one leg of such an inverter is shown in Figure 2.7. As may be seen, this topology uses a voltage-doubler to provide multilevel effects, which limits the power output capability of the inverter. Moreover, the switch-sets S₁—S₂ and S₃—S₄ need to be operated simultaneously which is rather difficult in practical situations.
Figure 2.7  Simplified schematic of one leg of a four-level voltage doubler inverter

2.2.7  Comparison of MLI Topologies

Various topologies discussed above are compared in terms of number of power electronic devices required to generate the same number of levels. Table 2.1 gives the comparisons between various symmetrical multilevel inverter topologies available in the literature with the well known conventional MLI topologies. It is observed from the Table 2.1 that the H bridge inverter with bidirectional switches (Rahim et al 2011) is the best topology among the symmetrical MLI topologies. Similarly Table 2.2 gives the comparison of asymmetrical MLI topologies, among the compared topologies asymmetrical MLI 1:3:9 topology dominate because it requires minimum number of switches to generate higher number of levels. Figure 2.8 shows the number of levels vs. number of power electronic devices of various topologies of MLI.
Table 2.1 Comparison of basic symmetrical topologies of MLI

<table>
<thead>
<tr>
<th>Topology</th>
<th>Number of Power Semiconductor devices</th>
<th>Number of Clamping diodes</th>
<th>Number of Clamping capacitor</th>
<th>Number of DC link Capacitors</th>
<th>Number of Isolated DC sources</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode Clamped</td>
<td>2(N-5)+8</td>
<td>2+(N-5)</td>
<td>0</td>
<td>$\frac{N - 1}{2}$</td>
<td>1</td>
</tr>
<tr>
<td>Capacitor Clamped</td>
<td>2(N-5)+8</td>
<td>0</td>
<td>$2^{\frac{(N-5)}{2}}$</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Cascaded H bridge (1:1:1)</td>
<td>2(N-5)+8</td>
<td>0</td>
<td>0</td>
<td>$\frac{N - 1}{2}$</td>
<td>$2^{\frac{(N-5)}{2}}$</td>
</tr>
<tr>
<td>New MLI Topology (Najafi &amp; Yatim 2012)</td>
<td>(N-7)+10</td>
<td>0</td>
<td>0</td>
<td>$\frac{N - 1}{2}$</td>
<td>$3^{\frac{(N-7)}{2}}$</td>
</tr>
<tr>
<td>Rahim et al 2011</td>
<td>(\frac{(N-5)}{2}+5)</td>
<td>0</td>
<td>0</td>
<td>$\frac{N - 1}{2}$</td>
<td>1</td>
</tr>
</tbody>
</table>

N = required number of levels.

Figure 2.8  Number of levels Vs power electronic devices of various MLI topologies
Table 2.2 Comparison of basic asymmetrical cascaded MLI topologies

<table>
<thead>
<tr>
<th>Topology</th>
<th>Number of Isolated DC sources ($N_{DC}$)</th>
<th>Number of Levels ($N$)</th>
<th>Number of Power Semiconductor devices (PD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cascaded H bridge (Asymmetrical 1:2:4 Configuration)</td>
<td>$N_{DC} = 2, 3…$</td>
<td>$2^{(N_{DC}+1)} - 1$</td>
<td>$4N_{DC}$</td>
</tr>
<tr>
<td>Cascaded H bridge (Asymmetrical 1:3:9 Configuration)</td>
<td>$N_{DC} = 2, 3…$</td>
<td>$3^{(N_{DC}+1)}$</td>
<td>$4N_{DC}$</td>
</tr>
</tbody>
</table>
| Switched Series/Parallel DC sources (Hinago & Koizumi 2010) | $N_{DC} = 3, 4, 5…$                      | $4(N_{DC}-1)+3$        | $PD = 11$ for $N_{DC} = 3$
$= 14$ for $N_{DC} = 4$
$= 17$ for $N_{DC} = 5$
and so on. |

2.3 REVIEW ON MAXIMUM POWER POINT TRACKING FOR PV ARRAYS

MPPT algorithms are designed for the PV energy conversion system to adapt to environmental changes so that optimal power is delivered. Typically, MPPT algorithms are integrated into power electronic converter systems, where the duty cycle of the converter is controlled to deliver maximum available power to the load. This section presents various MPPT algorithms proposed in the literature. Figures 2.9 and 2.10 show typical Voltage Vs Current (VI) and Power Vs Voltage (PV) characteristics of a photovoltaic array.

2.3.1 Fractional Open Circuit Voltage

The near linear relationship between $V_{MPP}$ (Voltage at MPP) and $V_{OC}$ (Open circuit Voltage) of the PV array, under varying irradiance and temperature levels, has given rise to the fractional $V_{OC}$ method (Schoeman & Van Wyk 1982, Buresch 1983, Hart et al 1984, Patterson 1990).
\[ V_{MPP} \approx k_1 V_{OC} \]  \hfill (2.1)

Figure 2.9 VI characteristics of PV array

where \( k_1 \) is a constant of proportionality. Since \( k_1 \) is dependent on the characteristics of the PV array being used, it usually has to be computed beforehand by empirically determining \( V_{MPP} \) and \( V_{OC} \) for the specific PV array at different irradiance and temperature levels. The factor \( k_1 \) has been reported to be between 0.71 and 0.78.

Figure 2.10 Power Vs Voltage characteristics of PV array
Once $k_1$ is known, $V_{MPP}$ can be computed using (2.1) with $V_{OC}$ measured periodically by momentarily shutting down the power converter. However, this incurs some disadvantages, including temporary loss of power. To prevent this, (Hart et al 1984) used pilot cells from which $V_{OC}$ can be obtained. These pilot cells must be carefully chosen to closely represent the characteristics of the PV array. In (Kobayashi et al 2004), it is claimed that the voltage generated by pn-junction diodes is approximately 75% of $V_{OC}$. This eliminates the need for measuring $V_{OC}$ and computing $V_{MPP}$. Once $V_{MPP}$ has been approximated, a closed-loop control on the array power converter can be used to asymptotically reach this desired voltage.

Since (2.1) is only an approximation, the PV array technically never operates at the MPP. Depending on the application of the PV system, this can sometimes be adequate. Even if fractional $V_{OC}$ is not a true MPPT technique, it is very easy and cheap to implement as it does not necessarily require DSP or microcontroller control. However, (Bekker & Beukes 2004) points out that $k_1$ is no more valid in the presence of partial shading (which causes multiple local maxima) of the PV array and propose sweeping the PV array voltage to update $k_1$. This obviously adds to the implementation complexity and incurs more power loss.

2.3.2 **Fractional Short-Circuit Current**

Fractional $I_{SC}$ (Short circuit Current) results from the fact that, under varying atmospheric conditions, $I_{MPP}$ (Current at MPP) is approximately linearly related to the $I_{SC}$ of the PV array as shown (Hart et al 1984, Masoum et al 2002, Noguchi et al 2000)

$$I_{MPP} \approx k_2 I_{SC}$$ (2.2)
where \( k_2 \) is proportionality constant. Just like in the fractional \( V_{OC} \) technique, \( k_2 \) has to be determined according to the PV array in use. The constant \( k_2 \) is generally found to be between 0.78 and 0.92.

Measuring \( I_{SC} \) during operation is problematic. An additional switch usually has to be added to the power converter to periodically short the PV array so that \( I_{SC} \) can be measured using a current sensor. This increases the number of components and cost. In (Yuvarajan & Xu 2003), a boost converter is used, where the switch in the converter itself can be used to short the PV array.

Power output is not only reduced when finding \( I_{SC} \) but also because the MPP is never perfectly matched as suggested by (2.2). In (Noguchi et al 2000), a way of compensating \( k_2 \) is proposed such that the MPP is better tracked while atmospheric conditions change. To guarantee proper MPPT in the presence of multiple local maxima, (Bekker & Beukes 2004) periodically sweeps the PV array voltage from open-circuit to short-circuit to update \( k_2 \). Most of the PV systems using fractional \( I_{SC} \) in the literature use a DSP. In (Yuvarajan & Xu 2003), a simple current feedback control loop is used instead.

### 2.3.3 Perturb & Observe and Perturb & Observe Based on PI

The P&O (Perturb & Observe) method operates by periodically incrementing or decrementing the output terminal voltage of the PV cell and comparing the power obtained in the current cycle with the power of the previous one (performs \( dP/dV \)). If the voltage varies and the power increases, the control system changes the operating point in that direction; otherwise, it changes the operating point in the opposite direction. Once the direction for the change of voltage is known, the voltage is varied at a constant rate. This rate is a parameter that should be adjusted to allow the balance between faster
response and less fluctuation in steady state (Li et al 2010, Yu et al 2010, Abdelsalam et al 2011, Yu 2002). A modified version is obtained when the steps are changed according to the distance of the MPP, resulting in higher efficiency. This is an excellent method to reach the MPP, and it is independent from the PV panel/manufacturer; however, this method may suffer from fast changes in environmental conditions. Interesting P&O algorithm comparisons can be found (Abdelsalam et al 2011). The following equation represents this method:

$$\text{Signal} \left( \frac{dP}{dV} \right) X(-kr) = D$$  \hspace{1cm} (2.3)

where \(dP/dV\) represents the derivative of Power (P) in relation to Voltage (V), \(kr\) is a constant, and D is the duty cycle.

Improvements can be obtained through a digital controller, transforming the conventional P&O into an adaptive solution once different step sizes according to the distance of the MPP are performed. In steady state, the operation point is not altered unless changes in environmental conditions happen. The key idea is to reduce to zero the \(dP/dV\) using a closed-loop control performing the P&O based on PI.

### 2.3.4 Incremental Conductance and Incremental Conductance Based on PI

The IC (Incremental Conductance) method is based on the fact that the power slope of the PV is null at MPP \((dP/dV = 0)\), positive in the left, and negative in the right, as shown in Figure 2.9 (Abdelsalam et al 2011, Hsieh et al 2008). Thus, due to this condition, the MPP can be found in terms of the increment in the array conductance. Using (2.4), it is possible to find the IC conditions presented by (2.5)
\[
\frac{dP}{dV} = \frac{d(v \times i)}{dv} = i + v \frac{di}{dv} = 0 \quad (2.4)
\]

\[
\frac{\Delta i}{\Delta v} = -\frac{i}{v} \quad (a)
\]

\[
\frac{\Delta i}{\Delta v} > \frac{i}{v} \quad (b)
\]

\[
\frac{\Delta i}{\Delta v} < \frac{i}{v} \quad (c)
\]

where (a) represents the condition at MPP, (b) represents the condition in the left of MPP, and (c) represents the condition in the right of MPP.

In theory, the steady-state oscillations would be eliminated once the derivative of power with respect to voltage is null at MPP. However, a null value of this slope hardly ever occurs due to digital implementation resolution. Strong points are that this method also features a modified version and does not suffer from fast transients in environmental conditions (Mastromauro et al 2009, Liu et al 2008)

The IC method needs to monitor both the voltage and current of the PV as P&O method. However, it is not necessary to calculate the PV power. A contribution in the implementation of this method can be done by adding a simple PI controller to improve the IC method, minimizing the error between the actual conductance and the incremental conductance, because the compensator can be adjusted and updated according to the system necessity. Moreover, this PI controller can reduce the ripple oscillations in steady state, minimizing the issues involving digital resolution implementation. This method can be seen as an adaptative solution once it presents large step sizes when the PV is far from the MPP; then, the step sizes are reduced according to the distance of MPP, and finally, when the MPP is achieved, the system
operation point is not changed, unless the climate conditions are modified. The digital PI can control directly the duty cycle ($D$) or the converter current ($I_L$). With both constraints, it is possible to find the MPP. Using $I_L$ rather than $D$, it makes the control more attractive once it permits that great changes in environmental conditions can be described as small changes in the converter current; however, if $D$ is the control action, great changes mean big changes in the operation point of the converter. Thus, the controller bandwidth must be reduced in the second case.

2.3.5 Beta Method

The beta method is the approximation of the point of maximum power through the equation of an intermediate variable $\beta$, as given in the following (Jain & Agarwal 2004):

$$\beta = \ln \left( \frac{I_{pv}}{V_{pv}} \right) - c x V_{pv}$$

(2.6)

where $c = (q / (\eta \cdot K_B \cdot T \cdot N_s))$ is a constant that depends on the electron charge ($q$), the quality factor of the junction panel ($\eta$), the Boltzmann constant ($K_B$), temperature ($T$), and amount of series PV cells ($N_s$). Moreover, as the operating conditions change, the value of $\beta$ at the optimum point remains almost constant. Thus, $\beta$ can be continuously calculated using the voltage and current of the panel and inserted on a conventional closed loop with a constant reference (Jain & Agarwal 2004). However, for optimal performance, it is mandatory to know the PV electrical parameters, which can reduce the attractiveness of this method.
2.3.6 System Oscillation and Ripple Correlation

The system oscillation method is based on the principle of maximum power transfer, and it uses the oscillations to determine the optimum point of operation. At the MPP, the ratio of the amplitude of the oscillation to the average voltage is constant. This method needs only to sense PV voltage, and it can be easily implemented with only analogical circuitries (Ho et al. 2004, Ho & Chung 2005). Its implementation is basically characterized by the usage of filters. For implementing system oscillation, the double grid frequency (in the case of grid-tied converters) or the additional low-frequency ripple can be used. However, switching frequencies must be filtered before being acquired in order to avoid wrong switching states and an increase of electromagnetic interference issues, and because of that, implementation of this method in the converter switching frequency is not a common option. Ripple correlation is also based on the principles of maximum power transfer, and it uses the oscillations in power through all pass filters to obtain the optimal point. In other words, the high-frequency ripples in power and voltage are captured using high-frequency filters, which are used to compute $dP/dV$. Then, the sign of this derivative is used in a signal function to indicate the right region of operation, and an integrator also ensures the MPP. Additionally, this method presents very fast dynamics converging asymptotically to the MPP, and it is also possible to achieve convergent speeds at a rate similar to the switching converter frequency; however, it is limited by the converter controller gain (Casadei et al. 2006, Esram et al. 2006).

2.3.7 Temperature Method

Another very good option is to use a temperature method where the shortcomings of variations in temperature, which strictly changes the MPP, can be avoided. For this purpose, a low-cost temperature sensor is adopted
and in turn if modifies the MPP algorithm function by maintaining the right track of MPP. However, temperature sensing in practical implementations can be a problematic issue due to irregular distribution of PV array temperature, which can be avoided in small PV converters.

Moreover, the sensor may be poorly calibrated or not correctly attached, providing wrong measurements of PV temperature. This method is similar to the fractional open circuit voltage method, and because of that, it is simple for implementation (Park & Yu 2004, Mutoh et al 2002). The equation that guides the temperature method is presented in

\[ V_{MPP}(t) = V_{MPP}(T_{ref}) + T_{Kvoc}(T - T_{ref}) \]  

where \( V_{MPP} \) is the MPP voltage, \( T \) is the panel temperature surface, \( T_{Kvoc} \) is the temperature coefficient of \( V_{MPP} \), and \( T_{ref} \) is the standard test conditions temperature.

### 2.3.8 Fuzzy Logic Control

The inputs to a MPPT fuzzy logic controller are usually an error \( E \) and a change in error \( \Delta E \). The user has the flexibility of choosing how to compute \( E \) and \( \Delta E \). Since \( dP/dV \) vanishes at the MPP, uses the approximation

\[ E(n) = \frac{p(n) - p(n-1)}{v(n) - v(n-1)} \]  

and

\[ \Delta E(n) = E(n) - E(n - 1) \]

Equivalently, (2.5) is very often used. Once \( E \) and \( \Delta E \) are calculated and converted to the linguistic variables, the fuzzy logic controller output, which is typically a change in duty ratio \( \Delta D \) of the power converter, can be looked up in a rule base table such as Table 2.1
Fig 2.11 Membership functions for MPPT Controller

Table 2.3 Fuzzy Rule Base for MPP Tracking

<table>
<thead>
<tr>
<th>$\Delta E$</th>
<th>Nb</th>
<th>NS</th>
<th>ZE</th>
<th>PS</th>
<th>PB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nb</td>
<td>ZE</td>
<td>ZE</td>
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</table>

The linguistic variables assigned to $\Delta D$ for the different combinations of $E$ and $\Delta E$ is based on the power converter being used and also on the knowledge of the user. Table 2.3 is based on a boost converter. If, for example, the operating point is far to the left of the MPP (Figure 2.10), that is $E$ is PB, and $\Delta E$ is ZE, then if it required to largely increase the duty ratio that is $\Delta D$ should be PB to reach the MPP.

In the defuzzification stage, the fuzzy logic controller output is converted from a linguistic variable to a numerical variable still using a membership function as in Figure 2.11. This provides an analog signal that will control the power converter to the MPP. MPPT fuzzy logic controllers
have been shown to perform well under varying atmospheric conditions. However, their effectiveness depends a lot on the knowledge of the user or control engineer in choosing the right error computation and coming up with the rule base table. In (Patcharaprakiti & Premrudeeprachaecharn 2002) an adaptive fuzzy logic control is proposed that constantly tunes the membership functions and the rule base table so that optimum performance is achieved. Experimental results from (Senju & Uezato 1994) show fast convergence to the MPP and minimal fluctuation about it. In (Veerachary et al 2003), two different membership functions are empirically used to show that the tracking performance depends on the type membership functions considered.

2.3.9 Neural Network

Neural networks commonly have three layers: input, hidden, and output layers as shown in Figure 2.12. The number of nodes in each layer varies and is user-dependent. The input variables can be PV array parameters like $V_{OC}$ and $I_{SC}$, atmospheric data like irradiance and temperature, or any combination of these. The output is usually one or several reference signal(s) like a duty cycle signal used to drive the power converter to operate at or close to the MPP. How close the operating point gets to the MPP depends on the algorithms used by the hidden layer and how well the neural network has been trained. The links between the nodes are all weighted. The link between nodes $i$ and $j$ is labeled as having a weight of $w_{ij}$ in Figure 2.12. To accurately identify the MPP, the $w_{ij}$'s have to be carefully determined through a training process, whereby the PV array is tested over months or years and the patterns between the input(s) and output(s) of the neural network are recorded.
Since most PV arrays have different characteristics, a neural network has to be specifically trained for the PV array with which it will be used. The characteristics of a PV array also change with time, implying that the neural network has to be periodically trained to guarantee accurate MPPT.

2.3.10 Summary of MPPT Algorithms for PV Arrays

MPPT techniques discussed in the previous section will suit different applications. For example, in space satellites and orbital stations that involve large amount of money, the costs and complexity of the MPP tracker are not as important as its performance and reliability. The tracker should be able to continuously track the true MPP in minimum amount of time and should not require periodic tuning. In this case, hill climbing/P&O, IC, and RC (Ripple Correlation) are appropriate. Solar vehicles would mostly require fast convergence to the MPP. Fuzzy logic control, neural network, and RC are good options in this case.
<table>
<thead>
<tr>
<th>MPPT Technique</th>
<th>PV array Dependent?</th>
<th>True MPPT</th>
<th>Analog or Digital</th>
<th>Periodic Tuning?</th>
<th>Convergence Speed</th>
<th>Implementation Complexity</th>
<th>Sensed Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fractional $V_{OC}$</td>
<td>Yes</td>
<td>No</td>
<td>Both</td>
<td>Yes</td>
<td>Medium</td>
<td>Low</td>
<td>Voltage</td>
</tr>
<tr>
<td>Fractional $I_{SC}$</td>
<td>Yes</td>
<td>No</td>
<td>Both</td>
<td>Yes</td>
<td>Medium</td>
<td>Low</td>
<td>Current</td>
</tr>
<tr>
<td>P &amp; O</td>
<td>No</td>
<td>Yes</td>
<td>Both</td>
<td>No</td>
<td>Varies</td>
<td>Low</td>
<td>Voltage, Current</td>
</tr>
<tr>
<td>Inc. Conductance</td>
<td>No</td>
<td>Yes</td>
<td>Digital</td>
<td>No</td>
<td>Varies</td>
<td>Medium</td>
<td>Voltage, Current</td>
</tr>
<tr>
<td>Beta</td>
<td>Yes</td>
<td>Yes</td>
<td>Digital</td>
<td>No</td>
<td>Fast</td>
<td>Medium</td>
<td>Voltage, Current</td>
</tr>
<tr>
<td>System Oscillation</td>
<td>Yes</td>
<td>Yes</td>
<td>Analog</td>
<td>No</td>
<td>Medium</td>
<td>Complex</td>
<td>Voltage, Current</td>
</tr>
<tr>
<td>Ripple Correlation</td>
<td>No</td>
<td>Yes</td>
<td>Analog</td>
<td>No</td>
<td>Fast</td>
<td>Low</td>
<td>Voltage, Current</td>
</tr>
<tr>
<td>Temperature</td>
<td>Yes</td>
<td>Yes</td>
<td>Analog</td>
<td>No</td>
<td>Fast</td>
<td>Simple</td>
<td>Voltage, Temperature</td>
</tr>
<tr>
<td>Fuzzy Logic</td>
<td>Yes</td>
<td>Yes</td>
<td>Digital</td>
<td>Yes</td>
<td>Fast</td>
<td>High</td>
<td>Varies</td>
</tr>
<tr>
<td>Neural Network</td>
<td>Yes</td>
<td>Yes</td>
<td>Digital</td>
<td>Yes</td>
<td>Fast</td>
<td>High</td>
<td>Varies</td>
</tr>
</tbody>
</table>
Since the load in solar vehicles consists mainly of batteries, load current or voltage maximization should also be considered. The goal when using PV arrays in residential areas is to minimize the payback time and to do so, it is essential to constantly and quickly track the MPP. Therefore incremental conductance method is most suitable. For all other applications not mentioned here, containing in Table 2.4 are put together the major characteristics of all the MPPT techniques Table 2.4 should help in choosing an appropriate MPPT method. Further in this dissertation a simple sliding mode control based MPPT and evolutionary programming based MPPT techniques are introduced.

2.5 CONCLUSIONS

A brief literature review of various MLI topologies, MPPT algorithms for PV array reported for RE conversion has been discussed in this chapter. The MLI topologies are grouped into six groups based on their structural difference. Various topologies proposed in the literature are compared. Figure 2.8 shows the comparison of various topologies with respect to the number of power electronics devices required to generate a specific level. Among various configurations discussed, configurations with series connected H bridges are more popular for RE applications. In this dissertation a novel cascaded H bridge MLI is introduced with minimum number of power devices and minimum number of isolated DC sources.

Various algorithms of tracking the MPP have been presented briefly. Among the algorithms discussed, the performance of beta method is good in steady state and transient conditions. Further, it has medium complexity in implementation; however, it is dependent on the PV characteristics. In this dissertation a novel MPPT techniques based on evolutionary programming and sliding mode control is proposed.