CHAPTER 2
LOW-VOLTAGE FGMOS BASED VOLTAGE-CONTROLLED RESISTORS

2.1. Introduction

The resistors are widely used as the basic circuit elements for the development of analog circuits such as filters, oscillators, and amplifiers etc. However, there are certain limitations in direct implementation of resistors such as accuracy, low sheet resistance, and poor utilization of chip area. One of the possible solutions to overcome these problems is the use of JFETs or MOSFETs operating in ohmic region. In this technique, the value of the resistor is controlled by applying gate-to-source voltage to the JFETs or MOSFETs. The main drawback of these resistors is their very limited voltage range, which is due to the non-linear characteristics of the JFETs or MOSFETs. There are several techniques for increasing the linear range of the characteristics of JFETs or MOSFETs [69-72]. The most commonly used technique for improving linearity is to apply an appropriate voltage proportional to the input voltage obtained either by a scaled source follower [69-70] or by terminal voltage feedback [71] to the gate of the JFETs or MOSFETs. Most of the techniques available in literature to realize voltage-controlled resistors use additional circuitry for the cancellation of non-linear term present in the drain current equation.

Banu and Tsividis [69] have suggested a floating voltage-controlled resistor, in which four n-type MOSFETs and two p-type MOSFETs are used. The non-linear term present in the drain current equation of the p-type MOSFET is cancelled by applying an appropriate gate voltage, which is achieved by using two identical devices with their substrate terminals connected in parallel. Nay and Budak [73-74] have suggested a positive/negative voltage-controlled resistor, in which two op-amps and six resistors, along with a JFET operated in linear region are used. The non-linear term present in the drain current equation is cancelled by applying the appropriate gate-to-source voltage using additional circuitry. The value of the resistance is controlled by applied gate-to-source voltage. Senani and Bhaskar [75] have proposed an extremely simple configuration of voltage-controlled resistor, that achieves the same objective as [73-74], by using two op-amps and four resistors along with a JFET operated in linear region. The non-linear term present in the drain current equation is
cancelled by the additional circuitry applied at the gate terminal. The value of the resistance of this circuit is controlled by the voltage applied at the gate terminal of the JFET. The same circuit also provides both voltage-controlled inductance and capacitance elements.

Babanezhad and Temes [72] have proposed two grounded and one floating resistors by using two depletion-type MOSFETs operating in ohmic region. Instead of using depletion-type MOSFETs, Moon et al. [76] have suggested a voltage-controlled resistor with wide dynamic range similar to that of [72] using enhancement-type MOSFETs. The value of the resistance is controlled by the gate voltage of one of the MOSFETs. Wilson and Chan [71] have suggested voltage-controlled grounded resistor, in which a single MOSFET operating in the ohmic region is linearized by the terminal voltage feedback. The circuit uses seven n-type MOSFETs and two p-type MOSFETs. Wang [77] has proposed voltage-controlled grounded resistor, in which one of the MOSFETs operating in the ohmic region is linearized by connecting another MOSFET in parallel, biased in the saturation region. The circuit uses three n-type MOSFETs and two p-type MOSFETs. Dejhan et al. [78] have suggested a CMOS voltage-controlled grounded resistor, in which the non-linear term of the drain current equation is cancelled by a voltage adder circuit connected to the gate terminal. The circuit uses six MOSFETs operating in saturation region and one in the ohmic region. This resistor uses a single power supply for its operation. Sakurai and Ismail [79] have proposed a threshold independent CMOS square-law programmable floating resistor. This circuit uses fourteen n-type MOSFETs and six p-type MOSFETs operating in the saturation regions. Mahmoud [80] has suggested a floating resistor based on a configuration with only two MOSFETs between the supply rails. The linearization is achieved by addition and subtraction of the drain current equations. This circuit uses eight n-type MOSFETs and six p-type MOSFETs operating in the saturation regions. Liu et al. [81] have proposed a voltage-controlled resistor, in which non-linear term of one of the MOSFETs operating in ohmic region is cancelled by the other MOSFET operating in ohmic region. This circuit uses four n-type MOSFETs and two p-type MOSFETs. Ozalevli and Hasler [63] have suggested a floating-gate CMOS resistor based on a common-mode linearization technique. The circuit uses four transistors, four capacitors and two programming circuits. Popa’s [64-67] contribution in the design of voltage-controlled resistors is very significant. Recently, Manolescu and Popa [68] have suggested a FGMOS active resistor. The linearity of this circuit is improved by MOSFETs operating in the saturation region, which form a perfect
symmetrical structure. This circuit uses ten n-type MOSFETs, six p-type MOSFETs and four FGMOS transistors operating in the saturation regions.

In this chapter, FGMOS based voltage-controlled grounded and floating resistors have been proposed. The grounded and floating resistors developed here are namely FGMOS based voltage-controlled grounded resistor (FGVCGR), FGMOS based voltage-controlled resistor (FGVCR), modified FGVCR, threshold-dependent FGMOS based tunable grounded resistor (TD FGTGR), threshold-independent FGMOS based tunable grounded resistor (TI FGTGR) and FGMOS based tunable floating resistor (FGTFR). Grounded resistors FGVCGR, FGVCR and modified FGVCR have been developed by using additional circuitry for the cancellation of non-linear term present in the drain current equation whereas TD FGTGR and TI FGTGR have been developed without the use of any additional circuitry. The floating resistor FGTFR has been developed by addition and subtraction of drain currents of FGMOS operating in saturation region.

All the proposed circuits in this chapter have been simulated using OrCAD PSPICE and the simulation results are presented to validate the effectiveness of these circuits. The performance parameters of the proposed circuits have also been compared with the existing circuits available in literature and the comparison shows that the proposed circuits have improved performance in terms of supply voltage requirement, power dissipation, total harmonic distortion (THD) and input range as compared to the existing circuits.

This chapter is organized as follows. Section 2.2 discusses the FGMOS based voltage-controlled grounded resistors such as FGVCGR, FGVCR, modified FGVCR, TD FGTGR and TI FGTGR. In Section 2.3, FGMOS based tunable floating resistor (FGTFR) is suggested. The simulation results of all the proposed resistors are presented in Section 2.4. The chapter is concluded in Section 2.5.

2.2. FGMOS based voltage-controlled grounded resistors

Voltage-controlled grounded resistors are extensively used in the area of signal processing such as filters, oscillators, and automatic gain controller etc. In this Section, several voltage-controlled grounded resistors and their applications are proposed.
2.2.1. **FGMOS based voltage-controlled grounded resistor (FGVCGR)**

The basic circuit of FGMOS based voltage-controlled grounded resistor (FGVCGR) is shown in Fig. 2.1.

![Diagram of FGVCGR circuit](image)

**Fig. 2.1 Basic circuit of FGVCGR**

In this circuit, the non-linear term of the drain current equation of M₁, operating in the ohmic region is cancelled by the drain current equation of transistor M₂, operating in the saturation region. Using eqn. (1.8), the drain current $I₁$ is given as

$$I₁ = K_{n₁} \left( (k_{₁₁} V_b + k_{₁₂} V_C - V_{T₁}) V_{IN} - \frac{V_{IN}^2}{2} \right)$$  \hspace{1cm} (2.1)

where $K_{n₁}$ is the transconductance parameter,

$k_{₁₁} (= C₁/C_T)$, $k_{₁₂} (= C₂/C_T)$ are the capacitive coupling ratios,

$C_T (= C₁ + C₂)$ is the total capacitance,

$V_b$ is the bias voltage,

$V_C$ is the control voltage,

$V_{T₁}$ is the threshold voltage and

$V_{IN}$ is the input voltage.

The drain current $I₂$ of conventional MOSFET is given as

$$I₂ = \frac{K_{n₂}}{2} (V_{IN} - V_{SS} - V_{T₂})^2$$  \hspace{1cm} (2.2)

where $K_{n₂}$ is the transconductance parameter,

$V_{IN}$ in the input voltage,
$V_{SS}$ is the source voltage and $V_{Tn2}$ is the threshold voltage of the transistor $M_2$.

From Fig. 2.1, it can be seen that the input current of the circuit is the sum of both the drain currents $I_1$ and $I_2$, i.e.

$$I_{IN} = I_1 + I_2$$  \hfill (2.3)

By substituting $K_{n1} = K_{n2}$ in eqn. (2.3), the squared term of input voltage $V_{IN}$ is cancelled out, (since $k_{11} + k_{12} = 1$) and the input current is then given as

$$I_{IN} = K_{n1}V_{IN} \left((k_{11}V_b + k_{12}V_c - V_{Tn1}) - (V_{SS} + V_{Tn2})\right) + I_{offset}$$  \hfill (2.4)

where $I_{offset} = \frac{K_{n2}}{2}(V_{SS} + V_{Tn2})^2$.

From eqn. (2.4), it is observed that if $I_{offset}$ is eliminated, a linear relationship between $I_{IN}$ and $V_{IN}$ can be established. Fig. 2.2 shows the complete circuit of FGVCGR in which the offset component $I_{offset}$ is eliminated by transistor $M_3$ which is biased in the saturation region.

![Fig. 2.2 Complete circuit of FGVCGR](image-url)
The transistor M3 is perfectly matched with M2 i.e. \( K_{n2} = K_{n3}, V_{tn2} = V_{tn3} \). The perfectly matched transistors M4 and M5 are used to form a current mirror that copies the offset current. Hence, eqn. (2.4) reduces to

\[
I_{IN} = K_{n1} V_{IN} \left( (k_{11} V_b + k_{12} V_c - V_{tn1}) - (V_{SS} + V_{tn2}) \right)
\]  

(2.5)

From eqn. (2.5), the equivalent resistance \( R_{eq} \) is defined as

\[
R_{eq} = \frac{V_{IN}}{I_{IN}} = \frac{1}{K_{n1} \left( (k_{11} V_b + k_{12} V_c - V_{tn1}) - (V_{SS} + V_{tn2}) \right)}
\]  

(2.6)

Equation (2.6) verifies the resistive behaviour of the circuit of Fig. 2.2. Hence, Fig. 2.2 behaves as a voltage-controlled grounded resistor and the value of the resistance is controlled by the voltage \( V_c \). The simulation results of FGVCGR are presented in Section 2.4.1.1.

2.2.1.1. High-pass filter based on FGVCGR

The high-pass filter based on FGVCGR is shown in Fig. 2.3. This high-pass filter is developed by using a capacitor (\( C=10\text{pF} \)) and a FGVCGR. The frequency response of this filter is controlled by FGVCGR and the simulation results of this circuit are presented in Section 2.4.1.1.1.

![Fig. 2.3 Tunable high-pass filter based on FGVCGR](image)
2.2.2. **FGMOS based voltage-controlled resistor (FGVCR)**

The FGMOS based voltage-controlled resistor (FGVCR) is shown in Fig. 2.4. In this figure, the transistors M₁, M₂, M₃, and M₄ are floating-gate MOSFETs and M₅ and M₆ are conventional MOSFETs. The transistors M₁ and M₂ are used to develop the resistive behaviour of the circuit and the circuit is biased with the help of remaining transistors M₃, M₄, M₅ and M₆. The transistors M₁ and M₂ are perfectly matched i.e. $K_{n1} = K_{n2} = K_n$, $V_{Tn1} = V_{Tn2} = V_{Tn}$, $k_{11} = k_{21} = k_1$ and $k_{12} = k_{22} = k_2$ and both are biased in the ohmic region.

![Fig. 2.4 FGMOS based voltage-controlled resistor](image)
Using eqn. (1.8), the drain currents $I_1$ and $I_2$ are given as

$$I_1 = K_n \left\{ (k_1 (0 - V_{ss}) + k_2 (0 - V_{ss}) - V_{Tn}) V_{DS1} - \left( \frac{1}{2} \right) V_{DS1}^2 \right\} \quad (2.7)$$

$$I_2 = I_N + I_4 = K_n \left\{ (k_1 (V_b - V_{ss}) + k_2 (V_c - V_{ss}) - V_{Tn}) V_{DS2} - \left( \frac{1}{2} \right) V_{DS2}^2 \right\} \quad (2.8)$$

where $K_n$ is the transconductance parameter,

$k_1 = C_1/C_T$, $k_2 = C_2/C_T$ are the capacitive coupling ratios,

$C_T = C_1 + C_2$ is the total capacitance,

$V_{ss}$ is the source voltage,

$V_b$ is the bias voltage,

$V_c$ is the control voltage,

$V_{Tn}$ is the threshold voltage and

$V_{DS1}$ & $V_{DS2}$ are the drain-to-source voltages of transistors $M_1$ and $M_2$.

The transistors $M_5$ and $M_6$ are biased in the saturation region and both are perfectly matched i.e. $K_{p5} = K_{p6}$, $V_{Tp5} = V_{Tp6}$, $k_{51} = k_{61}$, $k_{52} = k_{62}$. These transistors form a current mirror that generate current $I_3$, therefore

$$I_3 = I_4 = I_1 \quad (2.9)$$

The transistors $M_3$ and $M_4$ are biased in the saturation region and both are perfectly matched i.e. $K_{n3} = K_{n4}$, $V_{Tn3} = V_{Tn4}$, $k_{31} = k_{41}$. Using eqn. (1.9), the currents $I_3$ and $I_4$ are obtained as
\[ I_3 = \frac{K_{n3}}{2} (V_{FGS3} - V_{TN3})^2 \quad (2.10) \]

\[ I_4 = \frac{K_{n3}}{2} (V_{FGS4} - V_{TN3})^2 \quad (2.11) \]

From eqns. (2.9), (2.10) and (2.11), the voltages \( V_{FGS3} \) and \( V_{FGS4} \) are obtained as

\[ V_{FGS3} = V_{FGS4} = \sqrt{\frac{2I_4}{K_{n3}}} + V_{TN3} \quad (2.12) \]

Since \( V_{FGS3} + V_{DS1} = V_{FGS4} + V_{DS2} \), therefore

\[ V_{DS1} = V_{DS2} \quad (2.13) \]

Substituting eqns. (2.7), (2.9) and (2.13) in eqn. (2.8), the current \( I_N \) is given as

\[ I_N = K_n (k_1 V_b + k_2 V_c) V_{DS2} \quad (2.14) \]

From eqn. (2.14), the equivalent resistance \( R_{eq} \) is defined as

\[ R_{eq} = \frac{V_{DS2}}{I_N} = \frac{1}{K_n (k_1 V_b + k_2 V_c)} \quad (2.15) \]

Equation (2.15) verifies the resistive behaviour of the circuit of Fig. 2.4. Hence, Fig. 2.4 behaves as a voltage-controlled resistor and the value of the resistance is controlled by the voltage \( V_c \). The simulation results of FGVCRR are presented in Section 2.4.1.2.
2.2.2.1. Modified FGVCR

Figure 2.5 shows the modified FGVCR which uses six, two-input FGMOS transistors. The FGMOS transistors $M_5$ and $M_6$ form a low-voltage current mirror that generates the current $I_3$, so that

$$I_3 = I_4 = I_1 \quad (2.16)$$

![Fig. 2.5 Modified FGVCR](image)

The FGMOS transistors $M_3$ and $M_4$ are biased in saturation region and both are perfectly matched i.e. $n_3 = n_4$, $V_{Tn3} = V_{Tn4}$, $k_{31} = k_{41} = k_3 = C_3/C_T$, $k_{32} = k_{42} = k_4 = C_4/C_T$. Using the eqn. (1.9), the currents $I_3$ and $I_4$ are obtained as

$$I_3 = \frac{K_{n_3}}{2} (V_{FGS3} - V_{Tn3})^2 \quad (2.17)$$

$$I_4 = \frac{K_{n_4}}{2} (V_{FGS4} - V_{Tn4})^2 \quad (2.18)$$
From eqns. (2.16), (2.17) and (2.18), the voltages \( V_{FGS3} \) and \( V_{FGS4} \) are obtained as

\[
V_{FGS3} = V_{FGS4} = \sqrt{\frac{2I_n}{K_{n3}}} + V_{Tn3}
\]  
(2.19)

Since \( V_{FGS3} + V_{DS1} = V_{FGS4} + V_{DS2} \), therefore

\[
V_{DS1} = V_{DS2}
\]  
(2.20)

Substituting eqns. (2.7), (2.16) & (2.20) in eqn. (2.8), the current \( I_N \) is given as

\[
I_N = K_n \left( k_1 V_b + k_2 V_c \right) V_{DS2}
\]  
(2.21)

From eqn. (2.21), the equivalent resistance \( R_{eq} \) is defined as

\[
R_{eq} = \frac{V_{DS2}}{I_N} = \frac{1}{K_n \left( k_1 V_b + k_2 V_c \right)}
\]  
(2.22)

Equation (2.22) verifies the resistive behaviour of the circuit of Fig. 2.5. Hence, Fig. 2.5 behaves as a voltage-controlled resistor and the value of the resistance is controlled by the voltage \( V_c \). The FGVCR presented in this section can be modified to obtain output voltage (\( V_{DS2} \)) with respect to ground by adding a differential-to-single ended converter given in [82]. The simulation results of modified FGVCR are presented in Section 2.4.1.2.1.

2.2.2.2. FGMOS based voltage-controlled negative resistor (FGVCNR)

The modified FGVCR can be used as a negative resistor, if the direction of the input current \( I_N \) is changed as shown in Fig. 2.5 (as shown by the dotted line). For this case, eqn. (2.21) is modified as

\[
I_N = -K_n \left( k_1 V_b + k_2 V_c \right) V_{DS2}
\]  
(2.23)
From eqn. (2.23), the equivalent negative resistance $R_{eq(negative)}$ is defined as

$$R_{eq(negative)} = -\frac{1}{K_n (k_1 V_b + k_2 V_c)} \quad (2.24)$$

Equation (2.24) verifies the negative resistive behaviour of the circuit of Fig. 2.5. Hence, the same circuit of Fig. 2.5 behaves as a tunable negative resistor and the voltage $V_c$ controls the value of the resistance. The simulation results of FGVCNR are presented in Section 2.4.1.2.2.

### 2.2.3. FGMOS based tunable grounded resistor (FGTGR)

The FGMOS based tunable grounded resistor (FGTGR) is shown in Fig. 2.6. The circuit has been realized using only one, three-input FGMOS. From this circuit, it can be seen that the gate voltage is equal to the weighted-sum of the three input voltages, $V_{in}$ (input voltage), $V_c$ (control voltage) and $V_b$ (bias voltage). The non-linear term of the drain current equation of FGMOS operating in the ohmic region is cancelled with the help of input gate voltage ($V_{in}$) under certain conditions. The voltage $V_c$ controls the value of the resistance and the bias voltage $V_b$ is used to realize either a threshold-dependent FGTGR (TD FGTGR) or a threshold-independent FGTGR (TI FGTGR). The simulation results of FGTGR are presented in Section 2.4.1.3.

#### 2.2.3.1. Threshold-dependent FGTGR (TD FGTGR)

From Fig. 2.6, it is evident that $I_{DS}^o = I_{in}$, $V_{DS} = V_{in}$, $V_{SS} = 0$, $V_{BS} = 0$. Substituting these values in eqn. (1.8), the drain current equation reduces to

$$I_{in} = K_n \left((V_{FG} - V_T) - (V_{in}/2)\right)V_{in} \quad (2.25)$$

where $K_n$ is the transconductance parameter,
$V_{FG}$ is the equivalent floating gate voltage,
$V_T$ is the threshold voltage and
$V_{in}$ is the input voltage.
The floating gate voltage ($V_{FG}$) of three-input FGMOS is given as

$$V_{FG} = k_1V_C + k_2V_b + k_3V_{in} \quad (2.26)$$

where $k_1 = C_1/C_T$, $k_2 = C_2/C_T$, and $k_3 = C_3/C_T$ are the capacitive coupling ratios,

$C_1, C_2, C_3$ are the capacitances between floating-gate and control gates,

$V_C$ is the control voltage,

$V_b$ is the bias voltage,

$V_{in}$ is the input voltage and

$C_T = C_1 + C_2 + C_3$ is the total capacitance.

Substituting the value of $V_{FG}$ from eqn. (2.26) in eqn. (2.25), it is observed that the non-linear term $V_{in}^2/2$ is cancelled out if $k_3$ is chosen as 1/2. Hence, eqn. (2.25) reduces to

$$I_{in} = K_n \left( k_1V_C + k_2V_b - V_T \right) V_{in} \quad (2.27)$$

From eqn. (2.27), the equivalent resistance $R_{eq}$ is defined as

$$R_{eq} = \frac{V_{in}}{I_{in}} = \frac{1}{K_n \left( k_1V_C + k_2V_b - V_T \right)} \quad (2.28)$$
Equation (2.28) verifies the resistive behaviour of the circuit of Fig. 2.6. Hence, Fig. 2.6 behaves as a threshold-dependent tunable grounded resistor and the value of the resistance is tuned by voltage $V_c$. The simulation results of TD FGTGR are presented in Section 2.4.1.3.1.

2.2.3.2. Threshold-independent FGTGR (TI FGTGR)

From eqn. (2.28), it can also be seen that if

$$k_2 V_b = V_T$$

(2.29)

Then eqn. (2.28) reduces to

$$R_{eq} = \frac{1}{K_c k_1 V_c}$$

(2.30)

Equation (2.30) verifies the resistive behaviour of the circuit of Fig. 2.6. Hence, the same circuit of Fig. 2.6 behaves as a threshold-independent tunable grounded resistor and the value of the resistance is controlled by voltage $V_c$. The simulation results of TI FGTGR are presented in Section 2.4.1.3.2.

2.2.3.3. High-pass filter based on TD/TI FGTGR

In this Section, the TD/TI FGTGRs have been used to develop third order tunable high pass filters [77]. Figure 2.7 shows the third order tunable high pass filter, which uses three TD/TI FGTGRs and capacitors.

![Third order high-pass filter based on TD/TI FGTGR](image)

*Fig. 2.7 Third order high-pass filter based on TD/TI FGTGR*
The transfer function of the high-pass filter obtained by the use of Pascal’s triangle [83] is given as

\[ H(s) = \frac{s^3 R_{eq}^3 C^3}{s^3 R_{eq}^3 C^3 + 6s^2 R_{eq}^2 C^2 + 5s R_{eq} C + 1} \] (2.31)

From eqn. (2.31), it can be seen that the frequency response of this filter is controlled by the proposed FGTGRs \( R_{eq} \) and the simulation results of high-pass filter based on TD/TI FGTGRs are presented in Section 2.4.1.3.3.

2.3. FGMOS based tunable floating resistor (FGTFR)

The FGMOS based tunable floating resistor (FGTFR) is shown in Fig. 2.8. In the figure, nodes 1 and 2 are the two terminals of the resistor.

Fig. 2.8 FGMOS based tunable floating resistor (FGTFR)

The two-input FGMOS transistors \( M_1, M_2, M_3 \) and \( M_4 \) are used to form a floating resistor and are perfectly matched i.e. \( k_{n1} = k_{n2} = k_{n3} = k_{n4} = K_n \), \( V_{tn1} = V_{tn2} = V_{tn3} = V_{tn4} = V_{tn} \), \( k_{11} = k_{21} = k_{31} = k_{41} = k_1 \) and \( k_{12} = k_{22} = k_{32} = k_{42} = k_2 \). The transistors \( M_5, M_6, \)
M7 and M8, M9, M10 generate currents I6 and I9 respectively. The remaining transistors are used to copy the required current and transfer it to the nodes 1 and 2. All the transistors are biased in saturation region. Using eqn. (1.9), the drain currents of transistors M1, M2, M3 and M4 are

\[ I_1 = \frac{K_n}{2} (k_{12} V_1 + k_{22} V_{bias} - V_a - V_{TN})^2 \] (2.32)

\[ I_2 = \frac{K_n}{2} (k_{12} V_2 + k_{22} V_{bias} - V_a - V_{TN})^2 \] (2.33)

\[ I_3 = \frac{K_n}{2} (k_{13} V_3 + k_{23} V_{bias} - V_b - V_{TN})^2 \] (2.34)

\[ I_4 = \frac{K_n}{2} (k_{14} V_4 + k_{24} V_{bias} - V_b - V_{TN})^2 \] (2.35)

where \( K_n \) is the transconductance parameter,
\( k_{12} (= C_1/C_T) \) and \( k_{22} (= C_2/C_T) \) are the capacitive coupling ratios,
\( C_T (= C_1 + C_2) \) is the total capacitance,
\( V_1 \) and \( V_2 \) are input voltages,
\( V_{bias} \) is the bias voltage,
\( V_a \) and \( V_b \) are the source voltages and
\( V_{TN} \) is the threshold voltage.

By applying KCL at node 1 or node 2, the current I is obtained as

\[ I = I_6 - I_9 = (I_1 + I_3) - (I_2 + I_4) \] (2.36)

Using eqns. (2.32) to (2.35) in eqn. (2.36), the current I is obtained as

\[ I = K_n k_1 (V_i - V_2) (V_b - V_a) \] (2.37)

From eqn. (2.37), the equivalent resistance \( R_{eq} \) between nodes 1 and 2 is defined as

\[ R_{eq} = \frac{V_i - V_2}{I} = \frac{1}{K_n k_1 (V_b - V_a)} \] (2.38)
From eqn. (2.38), it is observed that the value of resistance is independent of the threshold voltage and the resistance is tuned by the differential voltage \((V_b - V_a)\). Further, it is observed that if \((V_b - V_a) > 0\), then the circuit behaves as a positive resistor and for \((V_b - V_a) < 0\), the circuit behaves as a negative resistor.

2.3.1. Second order effects

The influence of second order effects such as channel length modulation and mobility degradation on the tunable floating resistor are discussed in this section.

2.3.1.1. Channel length modulation

The drain current equation of two-input FGMOS including channel length modulation effect is

\[
I_D = \frac{K_n}{2} \left( k_1 V_1 + k_2 V_{bias} - V_{DS} - V_{TN} \right)^2 \left( 1 + \lambda V_{DS} \right) \quad (2.39)
\]

where \(\lambda\) is the channel length modulation parameter.

Hence, the drain currents equations of transistors M1, M2, M3 and M4 including channel length modulation effects are given as

\[
I_1 = \frac{K_n}{2} \left( k_1 V_1 + k_2 V_{bias} - V_a - V_{TN} \right)^2 \left( 1 + \lambda V_{DS1} \right) \quad (2.40)
\]

\[
I_2 = \frac{K_n}{2} \left( k_1 V_2 + k_2 V_{bias} - V_a - V_{TN} \right)^2 \left( 1 + \lambda V_{DS2} \right) \quad (2.41)
\]

\[
I_3 = \frac{K_n}{2} \left( k_1 V_2 + k_2 V_{bias} - V_b - V_{TN} \right)^2 \left( 1 + \lambda V_{DS3} \right) \quad (2.42)
\]

\[
I_4 = \frac{K_n}{2} \left( k_1 V_1 + k_2 V_{bias} - V_b - V_{TN} \right)^2 \left( 1 + \lambda V_{DS4} \right) \quad (2.43)
\]

where \(V_{DS1} = V_{D1} - V_a\), \(V_{DS2} = V_{D2} - V_a\), \(V_{DS3} = V_{D1} - V_b\) and \(V_{DS4} = V_{D2} - V_b\) are the drain-to-source voltages.
Substituting eqns. (2.40) to (2.43) in eqn. (2.36), current I is obtained as

\[ I = K_n k_i (V_1 - V_2)(V_b - V_a) + \frac{K_\lambda}{2} \left( A_0 + A_1 V_a + A_2 V_a^2 + A_3 V_b + A_4 V_b^2 \right) \]  \hfill (2.44)

where

\[ A_0 = (V_{D1} - V_{D2}) \left[ k_i^2 (V_i^2 + V_2^2) + 2k_i k_2 V_{bias}^2 + 2V_T + 2k_i k_2 V_{bias} (V_i + V_2) - 4k_i k_2 V_{bias} V_T - 2k_i V_T (V_i + V_2) \right] \],

\[ A_1 = \left[ k_i^2 (V_2^2 - V_1^2) + 2k_i (k_2 V_{bias} - V_T)(V_2 - V_1) + 2k_i (V_{D2} V_2 - V_{D1} V_1) + 2(k_2 V_{bias} - V_T)(V_{D2} - V_{D1}) \right] \],

\[ A_2 = \left[ (V_{D1} - V_{D2}) - 2k_i (V_2 - V_1) \right] \],

\[ A_3 = \left[ k_i^2 (V_i^2 - V_2^2) + 2k_i (k_2 V_{bias} - V_T)(V_1 - V_2) + 2k_i (V_{D2} V_1 - V_{D1} V_2) + 2(k_2 V_{bias} - V_T)(V_{D2} - V_{D1}) \right] \],

\[ A_4 = \left[ (V_{D1} - V_{D2}) - 2k_i (V_1 - V_2) \right] \],

\[ V_1 \text{ and } V_2 \text{ are input voltages,} \]

\[ V_{D1} \text{ and } V_{D2} \text{ are drain voltages and} \]

\[ V_a \text{ and } V_b \text{ are source voltages.} \]

From eqns. (2.44), it is observed that for small values of input voltages, drain voltages and source voltages, the channel length modulation effect can be neglected.

### 2.3.1.2. Mobility degradation effect

The effect of mobility degradation on the drain current of a two-input FGMOS is given as

\[ I_D = \frac{K_n}{2} \left[ \frac{(k_1 V_1 + k_2 V_{bias} - V_{SS} - V_{tn})^2}{1 + \theta (k_1 V_1 + k_2 V_{bias} - V_{SS} - V_{tn})} \right] \]  \hfill (2.45)

where \( \theta \) is the mobility degradation parameter.
In eqn. (2.45), by appropriate choices of \( k_1, V_1, k_2, V_{bias}, \) and \( V_{SS} \) the value of 
\[ 0(k_1 V_1 + k_2 V_{bias} - V_{SS} - V_{Tn}) \]

can be made much smaller than unity, then by using Binomial theorem and neglecting the higher order terms, equation (2.45) can be written as

\[
I_D = \frac{K_n}{2} \left( k_1 V_1 + k_2 V_{bias} - V_{SS} - V_{Tn} \right)^2 \left( 1 - 0 \left( k_1 V_1 + k_2 V_{bias} - V_{SS} - V_{Tn} \right) \right) \tag{2.46}
\]

The eqns. (2.32) to (2.35) are then modified as

\[
I_1 = \frac{K_n}{2} \left( k_1 V_1 + k_2 V_{bias} - V_a - V_{Tn} \right)^2 \left( 1 - 0 \left( k_1 V_1 + k_2 V_{bias} - V_a - V_{Tn} \right) \right) \tag{2.47}
\]

\[
I_2 = \frac{K_n}{2} \left( k_1 V_2 + k_2 V_{bias} - V_b - V_{Tn} \right)^2 \left( 1 - 0 \left( k_1 V_2 + k_2 V_{bias} - V_b - V_{Tn} \right) \right) \tag{2.48}
\]

\[
I_3 = \frac{K_n}{2} \left( k_1 V_1 + k_2 V_{bias} - V_b - V_{Tn} \right)^2 \left( 1 - 0 \left( k_1 V_1 + k_2 V_{bias} - V_b - V_{Tn} \right) \right) \tag{2.49}
\]

\[
I_4 = \frac{K_n}{2} \left( k_1 V_1 + k_2 V_{bias} - V_b - V_{Tn} \right)^2 \left( 1 - 0 \left( k_1 V_1 + k_2 V_{bias} - V_b - V_{Tn} \right) \right) \tag{2.50}
\]

Using eqns. (2.47) to (2.50) in eqn. (2.36), current \( I \) is obtained as

\[
I = K_n k_1 (V_1 - V_2)(V_b - V_a) \gamma \tag{2.51}
\]

where

\[
\gamma = \frac{\left[ 1 + (1/2)0(k_1 (V_1 + V_2) + 2k_2 V_{bias} - V_a - V_b - 2V_{T}) \right]}{1 + 20(k_1 (V_1 + V_2) + 2k_2 V_{bias} - V_a - V_b - 2V_{T})}.
\]

From eqn. (2.51), it is observed that if the values of \( k_1 V_1 + k_2 V_{bias} \) and \( k_1 V_2 + k_2 V_{bias} \) are made close to \( (V_a + V_b)/2 + V_T \), then the effect of mobility degradation can be reduced.

The simulation results of FGTFR are presented in Section 2.4.2.
2.4. Simulation results

This Section presents the simulation results of all the circuits proposed in this chapter. The workability of all the circuits proposed in this chapter have been verified by OrCAD PSPICE using model parameters of 0.5 µm or 0.25 µm CMOS technologies, which are listed in Appendix B.

2.4.1. Simulation results of grounded resistors

In this Section, the simulation results of FGMOS based voltage-controlled grounded resistor (FGVCGR), FGMOS based voltage-controlled resistor (FGVCR), modified FGVCR, FGMOS based voltage-controlled negative resistor (FGVCNR), threshold-dependent FGMOS based tunable grounded resistor (TD FGTGR), threshold-independent FGMOS based tunable grounded resistor (TI FGTGR) and high-pass filters based on FGVCGR, TD FGTGR and TI FGTGR using OrCAD PSPICE are presented.

2.4.1.1. Simulation results of FGVCGR

This Section presents the simulation results of FGVCGR shown in Fig. 2.2. Figure 2.9 shows the I-V characteristics of the FGVCGR operating at supply voltages of ± 0.75V. The input current $I_{IN}$ is plotted for $V_C = 0.10V$, $0.30V$, $0.50V$ and $0.70V$, while $V_{IN}$ is varied from -0.32V to 0.32V. Table 2.1 compares the simulated and theoretical values of equivalent resistances ($R_{eq}$) of FGVCGR for different values of control voltage $V_C$. The value of the simulated resistance is varied from 2.045 KΩ to 4.020 KΩ. From this table, it is observed that the simulation results are consistent with the theoretical results calculated using eqn. (2.6). The error between theoretical and simulated values of the resistance is found to be less than ±2%.
Fig. 2.9 I-V characteristics of FGVCGR

Table 2.1 Equivalent resistance values of FGVCGR for various values of $V_C$

<table>
<thead>
<tr>
<th>$V_C$ (Volts)</th>
<th>Equivalent Resistance ($R_{eq}$) (KΩ)</th>
<th>% Error ($\pm$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simulated</td>
<td>Theoretical</td>
</tr>
<tr>
<td>0.10</td>
<td>4.020</td>
<td>4.077</td>
</tr>
<tr>
<td>0.30</td>
<td>3.173</td>
<td>3.122</td>
</tr>
<tr>
<td>0.50</td>
<td>2.548</td>
<td>2.530</td>
</tr>
<tr>
<td>0.70</td>
<td>2.127</td>
<td>2.126</td>
</tr>
</tbody>
</table>

For the distortion analysis of this circuit, a sinusoidal input voltage $V_{IN}$ of 45 KHz with peak-to-peak amplitude ranging from 0.04V to 0.32V is employed.
Fig. 2.10 shows the total harmonic distortion (THD) obtained in the output waveform as a function of the peak-to-peak input voltage. (Appendix C - THD) From this figure, it is observed that for input voltage ranging from 0.04V to 0.32V, distortion is still low (≤0.28%). The total power dissipation of FGVCGR is 254 µW. Figure 2.11 shows the frequency response of FGVCGR and it is observed that the response remains constant till 5.2 GHz.

![Fig. 2.10 THD vs. input voltage amplitude of FGVCGR](image1)

![Fig. 2.11 Frequency response of FGVCGR](image2)

A comparison of the FGVCGR with voltage-controlled grounded resistors suggested in [71], [77] and [78] is listed in Table 2.2. From the table, it is evident that the FGVCGR has
lower supply voltage requirement, wider input range (42.66% of power supply) and lower THD as compared to the existing circuits. The -3dB frequency of this circuit is 5.2 GHz, which makes it suitable for high frequency signal processing applications.

### Table 2.2 Comparison of FGVCGR and voltage-controlled grounded resistors reported in [71], [77] and [78]

<table>
<thead>
<tr>
<th>Circuit parameters</th>
<th>Grounded resistor [71]</th>
<th>Grounded resistor [77]</th>
<th>Grounded resistor [78]</th>
<th>FGVCGR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages</td>
<td>( V_{DD}=</td>
<td>V_{SS}</td>
<td>=5V )</td>
<td>( V_{DD}=</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>Not available</td>
<td>Not available</td>
<td>Not available</td>
<td>0.25 µm</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>5V</td>
<td>4V</td>
<td>-0.4V to 0.4V</td>
<td>-0.32V to 0.32V</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Not available</td>
<td>Not available</td>
<td>21 µW</td>
<td>254 µW</td>
</tr>
<tr>
<td>THD</td>
<td>0.4% for input signals of 1V&lt;sub&gt;pp&lt;/sub&gt; and 1% for input signals of 4V&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>Not available</td>
<td>Less than 1%</td>
<td>0.28% for input signals of 0.32V&lt;sub&gt;pp&lt;/sub&gt;</td>
</tr>
<tr>
<td>-3dB frequency</td>
<td>4.3 MHz</td>
<td>Not available</td>
<td>7.2 GHz</td>
<td>5.2 GHz</td>
</tr>
</tbody>
</table>

#### 2.4.1.1.1. Simulation results of high-pass filter based on FGVCGR

This Section presents the simulation results of high-pass filter based on FGVCGR shown in Fig. 2.3. The frequency response of this high-pass filter is shown in Fig. 2.12 and it is observed that -3dB frequency of this filter is 9.385 MHz.

![Fig. 2.12 Frequency response of tunable high-pass filter based on FGVCGR](image)
2.4.1.2. Simulation results of FGVCR

In this Section, the simulation results of FGVCR shown in Fig. 2.4 are presented. Figure 2.13 shows the I-V characteristics of the FGVCR operating at supply voltages of ±0.90V. The output voltage ($V_{DSS}$) is plotted for $V_C = 0.10V$, 0.20V, 0.40V and 0.80V, while $I_N$ is varied from $-30\mu A$ to $30\mu A$.

![Fig. 2.13 I-V characteristics of FGVCR](image)

Table 2.3 compares the simulated and theoretical values of equivalent resistances ($R_{eq}$) of FGVCR for various values of control voltage $V_C$. The value of the simulated resistance is varied from $6 \, K\Omega$ to $8.33 \, K\Omega$. From this table, it is observed that the simulation results are consistent with the theoretical results calculated using eqn. (2.15). The error between theoretical and simulated values of the resistance is found to be less than 1%.

<table>
<thead>
<tr>
<th>$V_C$ (Volt)</th>
<th>Equivalent Resistance ($R_{eq}$) (K$\Omega$)</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simulated</td>
<td>Theoretical</td>
</tr>
<tr>
<td>0.10</td>
<td>8.33</td>
<td>8.25</td>
</tr>
<tr>
<td>0.20</td>
<td>7.69</td>
<td>7.62</td>
</tr>
<tr>
<td>0.40</td>
<td>6.67</td>
<td>6.62</td>
</tr>
<tr>
<td>0.60</td>
<td>6</td>
<td>5.95</td>
</tr>
</tbody>
</table>
For the distortion analysis of this circuit, a sinusoidal input current $I_n$ of 100 KHz with peak-to-peak amplitude ranging from 2 $\mu$A to 30 $\mu$A is employed. Fig. 2.14 shows the THD obtained in the output waveform as a function of the peak-to-peak input current. From this figure, it is observed that for input current ranging from 2 $\mu$A to 30 $\mu$A, distortion is still low ($\leq 1.66\%$). The total power dissipation of FGVCR is 27 $\mu$W. Figure 2.15 shows the frequency response of FGVCR and it is observed that the response remains constant till 123.5 MHz.

![Fig. 2.14 THD vs. input current amplitude of FGVCR](image1)

![Fig. 2.15 Frequency response of FGVCR](image2)
2.4.1.2.1. Simulation results of modified FGVCR

This Section presents the simulation results of modified FGVCR shown in Fig. 2.5. Figure 2.16 shows the I-V characteristics of the modified FGVCR operating at supply voltages of ±0.75V. The output voltage ($V_{DS2}$) is plotted for $V_c = 0.30$, 0.45, 0.60V and 0.75V, while $I_N$ is varied from -30μA to 30μA.

![Fig. 2.16 I-V characteristics of modified FGVCR](image)

Table 2.4 compares the simulated and theoretical values of equivalent resistances ($R_{eq}$) of modified FGVCR for the different values of control voltage $V_c$. The value of the simulated resistance is varied from 3.852 KΩ to 7.001 KΩ. From this table, it is observed that the simulation results are consistent with the theoretical results calculated using eqn. (2.22). The error between theoretical and simulated values of the resistance is found to be less than 1%.

**Table 2.4 Equivalent resistance values of modified FGVCR for various values of $V_c$**

<table>
<thead>
<tr>
<th>$V_c$ (Volts)</th>
<th>Equivalent Resistance ($R_{eq}$) (KΩ)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simulated</td>
<td>Theoretical</td>
</tr>
<tr>
<td>0.30</td>
<td>7.001</td>
<td>6.983</td>
</tr>
<tr>
<td>0.45</td>
<td>5.392</td>
<td>5.371</td>
</tr>
<tr>
<td>0.60</td>
<td>4.467</td>
<td>4.428</td>
</tr>
<tr>
<td>0.75</td>
<td>3.852</td>
<td>3.838</td>
</tr>
</tbody>
</table>
For the distortion analysis of this circuit, a sinusoidal input current $I_N$ of 100 KHz with peak-to-peak amplitude ranging from 2 µA to 30 µA is employed. Figure 2.17 shows the THD obtained in the output waveform as a function of the peak-to-peak input current. From this figure, it is observed that for input current ranging from 2 µA to 30 µA, distortion is still low ($\leq 0.94\%$). The total power dissipation of modified FGVCR is 18.6µW. Figure 2.18 shows the frequency response of the modified FGVCR and it is observed that the response remains constant till 66.7 MHz.

![Fig. 2.17 THD vs. input current amplitude of modified FGVCR](image)

![Fig. 2.18 Frequency response of modified FGVCR](image)
2.4.1.2.2. Simulation results of FGVCNR

In this Section, the simulation results of FGVCNR shown in Fig. 2.5 are presented. Figure 2.19 shows the I-V characteristics of FGVCNR operating at supply voltages of ±0.75V. The output voltage \( V_{DS2} \) is plotted for \( V_C = 0.30V, 0.45V, 0.60V \) and \( 0.75V \), while \( I_N \) is varied from -30µA to 30µA. The value of the simulated resistance is varied from -3.852 KΩ to -7.001 KΩ. The total power dissipation of FGVCNR is 14.7μW.

![Fig. 2.19 I-V characteristics of FGVCNR](image)

Table 2.5 compares the modified FGVCR with FGVCR and CMOS based voltage-controlled resistor reported in [81]. From the table, it is observed that the modified FGVCR has lower supply voltage requirement of ±0.75V, lower power dissipation of 18.6 µW, lower THD of 0.94% and wider input current range from -30 µA to 30 µA as compared to the existing circuits.
Table 2.5 Comparison of modified FGVCR with FGVCR and CMOS voltage-controlled resistor [81]

<table>
<thead>
<tr>
<th>Circuit parameters</th>
<th>voltage-controlled resistor [81]</th>
<th>FGVCR</th>
<th>Modified FGVCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages V_{DD}=</td>
<td>V_{SS}</td>
<td>= 1.5V</td>
<td>V_{DD}=</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
</tr>
<tr>
<td>Variation of input current</td>
<td>0 µA to 30 µA</td>
<td>-30 µA to 30 µA</td>
<td>-30 µA to 30 µA</td>
</tr>
<tr>
<td>Maximum equivalent resistance (R_{eq})</td>
<td>18.44 KΩ</td>
<td>8.33 KΩ</td>
<td>7.001 KΩ</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Not available</td>
<td>27 µW</td>
<td>18.6 µW</td>
</tr>
<tr>
<td>THD</td>
<td>Not available</td>
<td>≤ 1.66%</td>
<td>≤ 0.94%</td>
</tr>
<tr>
<td>-3dB frequency</td>
<td>Not available</td>
<td>123.5 MHz</td>
<td>67 MHz</td>
</tr>
</tbody>
</table>

2.4.1.3. Simulation results of FGTGR

This Section presents the simulation results of TD/TI FGTGR shown in Fig. 2.6. For the development of TD/TI FGTGR, the capacitances of three-input FGMOS are chosen as C_1 = 10pF, C_2 = 3.4514425pF, C_3 = 5.8760775pF, C_{fd} = 0.05924pF, C_{fs} = 0.554pF and C_{fb} = 0.05924pF. As discussed in Section 2.2.3.2, the TI FGTGR can be realized from the same circuit of TD FGTGR shown in Fig. 2.6, if the condition k_2 V_b = V_T given in eqn. (2.29) is satisfied. Further, since k_2 is the ratio of C_2 and C_T, and C_T is chosen as 20pF, then k_2 becomes 0.172572125. The PSPICE model parameters of 0.5 µm CMOS technology listed in Appendix B provide the threshold voltage V_T = 0.6902885V. By using eqn. (2.29), the value of the bias voltage is selected as V_b = 4V.
2.4.1.3.1. Simulation results of threshold-dependent FGTGR (TD FGTGR)

Figure 2.20 shows the I-V characteristics of the threshold-dependent FGTGR. The current $I_{in}$ is plotted for $V_C = -4V$, -1V and 2V, while $V_{in}$ is varied from -0.45V to 0.45V.

![I-V characteristics of TD FGTGR](image)

Table 2.6 compares the simulated and theoretical values of equivalent resistances ($R_{eq}$) of TD FGTGR for different values of control voltage $V_C$. The value of the simulated resistance is varied from 4.039 KΩ to 5.224 KΩ. From this table, it is observed that the simulation results are consistent with the theoretical results calculated using eqn. (2.28). The error between theoretical and simulated values of the resistance is found to be less than ±2.5%.

<table>
<thead>
<tr>
<th>Control voltage $V_C$ (Volt)</th>
<th>Equivalent Resistance ($R_{eq}$) (KΩ)</th>
<th>%Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simulated</td>
<td>Theoretical</td>
</tr>
<tr>
<td>-4V</td>
<td>5.224</td>
<td>5.258</td>
</tr>
<tr>
<td>-2V</td>
<td>4.732</td>
<td>4.738</td>
</tr>
<tr>
<td>0V</td>
<td>4.318</td>
<td>4.310</td>
</tr>
<tr>
<td>2V</td>
<td>4.039</td>
<td>3.954</td>
</tr>
</tbody>
</table>
For the distortion analysis of this circuit, a sinusoidal input voltage $V_{in}$ of 100 KHz with peak-to-peak amplitude ranging from 0.15V to 0.90V is employed. Figure 2.21 shows the THD obtained in the output waveform as a function of the peak-to-peak input voltage. From this figure, it is observed that for input voltage ranging from 0.15V to 0.90V, distortion is still low ($\leq 0.348\%$). The total power dissipation of the TD FGTGR is 2.61µW.

![Fig. 2.21 THD vs. input voltage amplitude of TD FGTGR](image)

Figure 2.22 shows the frequency response of this circuit and it is observed that the response remains constant till 14.9 GHz.

![Fig. 2.22 Frequency response of TD FGTGR](image)
2.4.1.3.2. Simulation results of threshold-independent FGTGR (TI FGTGR)

Figure 2.23 shows the I-V characteristics of the threshold-independent FGTGR. The current $I_{in}$ is plotted for $V_c=0.5V$, 1V and 1.5V, while $V_{in}$ is varied from -0.45V to 0.45V.

![Fig. 2.23 I-V characteristics of TI FGTGR](image)

Table 2.7 compares the simulated and theoretical values of equivalent resistances ($R_{eq}$) of TI FGTGR for different values of control voltage $V_c$. The range of the simulated resistance is varied from 6.331 KΩ to 24.385 KΩ. From this table, it is observed that the simulation results are consistent with the theoretical results calculated using eqn. (2.30). The error between theoretical and simulated values of the resistance is found to be less than ±3%.

<table>
<thead>
<tr>
<th>Control voltage $V_c$ (Volt)</th>
<th>Equivalent Resistance ($R_{eq}$) (KΩ)</th>
<th>%Error (±)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5V</td>
<td>24.385</td>
<td>1.09</td>
</tr>
<tr>
<td>1V</td>
<td>11.975</td>
<td>1.09</td>
</tr>
<tr>
<td>1.5V</td>
<td>8.419</td>
<td>2.85</td>
</tr>
<tr>
<td>2V</td>
<td>6.331</td>
<td>-2.7</td>
</tr>
</tbody>
</table>
For the distortion analysis of this circuit, a sinusoidal input voltage $V_{\text{in}}$ of 100 KHz with peak-to-peak amplitude ranging from 0.15V to 0.90V is employed. Figure 2.24 shows the THD obtained in the output waveform as a function of the peak-to-peak input voltage. From this figure, it is observed that for input voltage ranging from 0.15V to 0.90V, distortion is still low ($\leq 0.342\%$). The total power dissipation of the TD FGTGR is $1.63\mu W$.

![Fig. 2.24 THD vs. input voltage amplitude of TI FGTGR](image)

Figure 2.25 shows the frequency response of this circuit and it is observed that the response remains constant till 3.9 GHz.

![Fig. 2.25 Frequency response of TI FGTGR](image)
In the proposed TD/TI FGTGR, the value of capacitive coupling ratio $k_2 (= C_2 / C_T)$ is equal to 0.172572125. If $k_2$ is rounded off as 0.17, then it can be seen that the value of input capacitance $C_2$ changes from 3.4514425pF to 3.4pF. Figure 2.26 compares the I-V characteristics of the threshold-independent FGTGR for $V_C = 0.5V$, 1V and 1.5V with $k_2 = 0.172572125$ and $k_2 = 0.17$. In this figure, the I-V characteristics for $k_2 = 0.172572125$ and $k_2 = 0.17$ are shown by red and blue lines respectively. It is observed that these two plots almost overlap each other for all values of $V_C$. The percentage relative error has also been shown in Fig. 2.27, and it is further observed that the maximum relative error is less than 1%.

Fig. 2.26 I-V characteristics of TI FGTGR for $V_C = 0.5V$, 1.0V and 1.5V with $k_2 = 0.172572125$ and $k_2 = 0.17$
Fig. 2.27 Relative error in the simulated value of resistance for $V_C = 0.5V$
with $k_2 = 0.172572125$ and $k_2 = 0.17$

Table 2.8 compares the different parameters of TD FGTGR and TI FGTGR. From this table, it is observed that TI FGTGR shows better results as compared to TD FGTGR.

<table>
<thead>
<tr>
<th>Circuit parameters</th>
<th>TD FGTGR</th>
<th>TI FGTGR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum resistance value</td>
<td>5.224 KΩ</td>
<td>24.385 KΩ</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>2.61 µW</td>
<td>1.63 µW</td>
</tr>
<tr>
<td>THD</td>
<td>$\leq 0.348%$</td>
<td>$\leq 0.342%$</td>
</tr>
<tr>
<td>Input voltage range ($V_n$)</td>
<td>-0.45V to 0.45V</td>
<td>-0.45V to 0.45V</td>
</tr>
<tr>
<td>-3dB frequency</td>
<td>14.9 GHz</td>
<td>3.9 GHz</td>
</tr>
</tbody>
</table>
2.4.1.3.3. Simulation results of high-pass filter based on TD and TI FGTGRs

In this Section, the simulation results of high-pass filter based on TD/TI FGTGRs shown in Fig. 2.7 are presented. Figures 2.28 and 2.29 show the frequency responses of the tunable third order high-pass filter based on TD and TI FGTGRs respectively. Table 2.9 shows the various -3dB frequencies of both TD/TI FGTGRs based third order high pass filters for $V_C = 0.5$ to $2.0V$ with the increments of $0.5V$. From this table, it is concluded that the high pass filter has a wider frequency range for TI FGTGR as compared to TD FGTGR.

![Fig. 2.28 Frequency responses of third order high-pass filter based on TD FGTGR for $V_C = 0.5V$ to $2.0V$ with increments of $0.5V$]

![Fig. 2.29 Frequency responses of third order high-pass filter based on TI FGTGR for $V_C = 0.5V$ to $2.0V$ with increments of $0.5V$]
Table 2.9 -3dB frequencies of third order high-pass filter for various values of $V_C$

<table>
<thead>
<tr>
<th>Control voltage $V_C$</th>
<th>FGTGR based high-pass filter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Threshold dependent (TD)</td>
</tr>
<tr>
<td></td>
<td>(-3dB frequency)</td>
</tr>
<tr>
<td></td>
<td>Threshold independent (TI)</td>
</tr>
<tr>
<td></td>
<td>(-3dB frequency)</td>
</tr>
<tr>
<td>0.5V</td>
<td>2.765 MHz</td>
</tr>
<tr>
<td></td>
<td>584.617 KHz</td>
</tr>
<tr>
<td>1.0 V</td>
<td>2.805 MHz</td>
</tr>
<tr>
<td></td>
<td>958.506 KHz</td>
</tr>
<tr>
<td>1.5V</td>
<td>2.885 MHz</td>
</tr>
<tr>
<td></td>
<td>1.327 MHz</td>
</tr>
<tr>
<td>2.0V</td>
<td>2.926 MHz</td>
</tr>
<tr>
<td></td>
<td>1.663 MHz</td>
</tr>
</tbody>
</table>

2.4.1.4. **Comparison between proposed resistors FGVCGR, FGVCR, modified FGVCR, TD FGTGR and TI FGTGR**

Table 2.10 compares the various parameters of FGVCGR, FGVCR, modified FGVCR, TD FGTGR and TI FGTGR. From this table, it can be seen that the performance of TI FGTGR is better than the other circuits proposed in this chapter as it has low power dissipation of 1.63 µW, large range of resistance value and low THD of 0.342%. The -3dB frequency of this circuit is 3.9 GHz, which makes it suitable for high frequency signal processing applications.

Table 2.10 Comparison of TI FGTGR with FGVCGR, FGVCR, modified FGVCR and TD FGTGR

<table>
<thead>
<tr>
<th>Circuit parameters</th>
<th>FGVCGR</th>
<th>FGVCR</th>
<th>Modified FGVCR</th>
<th>TD FGTGR</th>
<th>TI FGTGR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltages</td>
<td>$V_{DD}=</td>
<td>V_{SS}</td>
<td>=0.75V$</td>
<td>$V_{DD}=</td>
<td>V_{SS}</td>
</tr>
<tr>
<td>Maximum resistance value</td>
<td>4.020 KΩ</td>
<td>8.33 KΩ</td>
<td>7.001 KΩ</td>
<td>5.224 KΩ</td>
<td>24.385 KΩ</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>0.25 µm</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
<td>0.5 µm</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>254 µW</td>
<td>27 µW</td>
<td>18.6 µW</td>
<td>2.61 µW</td>
<td>1.63 µW</td>
</tr>
<tr>
<td>THD</td>
<td>≤0.28%</td>
<td>≤1.66%</td>
<td>≤0.94%</td>
<td>≤0.348%</td>
<td>≤0.342%</td>
</tr>
<tr>
<td>-3dB frequency</td>
<td>5.2 GHz</td>
<td>123.5 MHz</td>
<td>67 MHz</td>
<td>14.9 GHz</td>
<td>3.9 GHz</td>
</tr>
</tbody>
</table>
2.4.2. Simulation results of FGTFR

This Section presents the simulation results of FGTFR shown in Fig. 2.8. Figure 2.30 shows the I-V characteristics of the FGTFR operating at supply voltages of \( \pm 0.75\)V. The current \( I \) is plotted for \( V_2 = -0.25\)V, -0.125V, 0.0V, 0.125V and 0.25V, while \( V_1 \) is varied from -0.25V to 0.25V with \( V_a = -0.55\)V and \( V_b = -0.25\)V. From this plot, it can be seen that this circuit behaves as linear resistor over the differential input voltage range from -0.50V to 0.50V and the value of the simulated resistance is equal to 33.33\( \Omega \). The value of the resistance is also calculated using eqn. (2.38) and the error between theoretical and simulated values of the resistance is found to be less than 2%.

![Fig. 2.30 I-V characteristics of FGTFR for different values of \( V_2 \) with \( V_a = -0.55\)V and \( V_b = -0.25\)V](image)

The I-V characteristics in Fig. 2.31 show the positive resistive behaviour of the FGTFR. The current \( I \) is plotted for \( V_a = -0.45\)V, -0.60V and -0.75V, while \( V_1 \) is varied from -0.25V to 0.25V with \( V_b = -0.15\)V and \( V_2 = 0\)V. From this plot, it can be seen that this circuit behaves as linear positive resistor over the single ended input voltage range from -0.25V to 0.25V and the value of the simulated resistance is varied from 16.67\( \Omega \) to 33.33\( \Omega \). The range of the resistance is also calculated using eqn. (2.38) and it is found that the error between theoretical and simulated values of the resistance is less than \( \pm 2\% \).
The I-V characteristics in Fig. 2.32 show the negative resistive behaviour of the FGTFR. The current I is plotted for $V_b = -0.45\,\text{V}$, $-0.60\,\text{V}$ and $-0.75\,\text{V}$, while $V_i$ is varied from -0.25V to 0.25V with $V_a = -0.15\,\text{V}$ and $V_1 = 0\,\text{V}$. From the plot, it can be seen that the FGTFR behaves as linear negative resistor over the single ended input voltage range from -0.25V to 0.25V and the values of the simulated resistance vary from $-16.67\,\text{K}\Omega$ to $-33.33\,\text{K}\Omega$. The range of the resistance is also calculated using eqn. (2.38) and the error between theoretical and simulated values of the resistance is found to be less than $\pm 2\%$. 

Fig. 2.31 I-V characteristics of FGTFR for different values of $V_a$ with $V_2 = 0\,\text{V}$ and $V_b = -0.15\,\text{V}$

Fig. 2.32 I-V characteristics of FGTFR for different values of $V_b$ with $V_2 = 0\,\text{V}$ and $V_a = -0.15\,\text{V}$
For the distortion analysis of this circuit, a sinusoidal input voltage $V_{in}$ of 100 KHz with peak-to-peak amplitude ranging from 0.10V to 0.50V is employed. Figure 2.33 shows the THD obtained in the output waveform as a function of the peak-to-peak input voltage. From this figure, it is observed that for input voltage ranging from 0.10V to 0.50V, distortion is still low ($\leq 0.64\%$). The total power dissipation of the FGTFR is 876 $\mu$W. Figure 2.34 shows the frequency response of FGTFR and it is observed that the response remains constant till 2.30 MHz.

![Fig. 2.33 THD vs. input voltage amplitude of FGTFR](image)

![Fig. 2.34 Frequency response of FGTFR](image)
Table 2.11 compares the different parameters of proposed FGTFR and floating resistors reported in [68], [79], and [80]. From this table, it is concluded that FGTFR operates with low supply voltages of ±0.75V. This circuit has lower THD (≤0.64%) and wider input voltage range (33.33% of the supply voltage) as compared to the existing similar circuits.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltages</td>
<td>V_{DD}=</td>
<td>V_{SS}</td>
<td>= 3V</td>
<td>V_{DD}=</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>0.35 µm</td>
<td>2 µm</td>
<td>0.35 µm</td>
<td>0.25 µm</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>±0.90V</td>
<td>± 1.5V</td>
<td>± 0.25V</td>
<td>± 0.25V</td>
</tr>
<tr>
<td>Maximum Power dissipation</td>
<td>Not available</td>
<td>4 mW</td>
<td>Not available</td>
<td>876 µW</td>
</tr>
<tr>
<td>Resistance range</td>
<td>± (100 KΩ to 3 MΩ)</td>
<td>44 KΩ to 85 KΩ</td>
<td>± (25 KΩ to 50 KΩ)</td>
<td>± (16.67 KΩ to 33.33 KΩ)</td>
</tr>
<tr>
<td>THD</td>
<td>0.45 %</td>
<td>1 %</td>
<td>0.4 % for input signals of 0.20V_{pp}</td>
<td>0.63% for input signals of 0.50V_{pp}</td>
</tr>
<tr>
<td>-3dB frequency</td>
<td>Not available</td>
<td>Not available</td>
<td>10 MHz</td>
<td>2.30 MHz</td>
</tr>
</tbody>
</table>

2.5. Conclusions

In this chapter, FGMOS based voltage-controlled resistors have been developed. The basic idea for the development of these circuits is the cancellation of nonlinear-term present in the drain current equation of FGMOS. The simulation results of FGMOS based voltage-controlled grounded resistor (FGVCGR), FGMOS based voltage controlled resistor (FGVCR), modified FGVCR, FGMOS based tunable grounded resistor (FGTGR) and FGMOS based tunable floating resistor (FGTFR) have been presented and compared with existing circuits. From comparison it is evident that the proposed circuits in this chapter exhibit low supply voltage requirement, low power dissipation, low THD and wide input range.