References


[7]. Ma Jing, “Signal and Image processing via reconfigurable computing”, Department of Electrical Engineering, University of New Orleans, New Orleans.


[17]. E. Ostúa, J. Juan Chico, J. Viejo, M. J. Bellido, D. Guerrero, A. Millán & P. Ruiz-de-Clavijo, “A SOC Design Methodology For LEON2 on FPGA”.


[19]. Salih Bayar and Arda Yurdakul, “Dynamic Partial Self-Reconfiguration on Spartan-III FPGAs via a Parallel Configuration Access Port (PCAP)”.

[20]. Ron Sass, Parag Beeraka, Jason Agron, Jeff Young, David Andrews, Brian Greskamp, Srinivas Beeravolu, Christian Trefftz, “Run time reconfigurable java virtual machine on platform FPGA”, Information Technology and Communications Center, University of Kansas.


[95]. J.A. Ambrose, “RIJD: Random Code Injection to Mask Power Analysis based Side Channel Attacks”, in Dac ’07, June 4-8, 2007, San Diego, California, USA.


163


[172]. LEON Source Code: http://Gaisler.com


[179]. Microblaze: www.Xilinx.com


168


[207]. David Pellerin, Scott Thibault, “Practical FPGA Programming in C”, Prentice Hall PTR,
2005.


