Appendix I

Empirical formulae for the characteristic impedance of single line interconnects

In this section, closed-form empirical expressions for the characteristic impedance of two types of single line interconnects are presented. These include a microstrip-like interconnect guarded by ground tracks and a microstrip-like interconnect over a ground plane aperture, as discussed in chapter 3 and chapter 5, respectively.

The formulae for characteristic impedance given here have been developed using finite-difference time-domain (FDTD) simulations as a source for generation of reliable data. Besides a large number of test measurements have been done on both the interconnect structures under study using a vector network analyzer and has led to agreement with our model, which generally was of the order of 1% over a wide range of meaningful interconnect parameters. As a special case, when the GPA width $W_S$ is reduced to zero or the spacing $d$ made very large, the results confirm to standard microstrip data. Therefore, we can practically use the proposed formulae for computation of impedance of microstrip lines as well.

Refer Fig. 3.1 and Fig. 5.1 of chapter 3 and chapter 5, respectively. The considered substrate thickness is $h_2 = 0.254 \text{ mm, 0.508 mm, 0.79 mm, and 1.59 mm}$, the strip width is $W \geq 0.05 \text{ mm}$, and the range of operating frequencies is $f = 0, \ldots, 7 \text{ GHz}$. The range of GPA width $W_S$ is $0, \ldots, 5 \text{ mm}$, and spacing $d$ is $0.001, \ldots, 5 \text{ mm}$ for the two respective interconnect structures. The line thickness $t$ is considered to be negligible. The expressions developed in this work has a mathematical form which is identical to that of Wheeler’s formula for characteristic impedance of microstrips, namely

$$Z_{\text{wheeler}} = \begin{cases} \frac{60}{\sqrt{\varepsilon_{\text{eff}}}} \ln \left( \frac{8}{W} + 0.25 \frac{W}{h} \right) & \text{for } \frac{W}{h} < 1 \\ \frac{120\pi}{\sqrt{\varepsilon_{\text{eff}}}} \times \left[ \frac{W}{h} + 1.393 + \frac{2}{3} \ln \left( \frac{W}{h} + 1.44 \right) \right] & \text{for } \frac{W}{h} > 1 \end{cases} \quad (A1.1)$$
where

\[
\varepsilon_{\text{eff}} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left(1 + \frac{10h}{W}\right)^{-\frac{1}{2}}, \quad h \equiv b_2, \varepsilon_r \equiv \varepsilon_2
\]  

(A1.2)

However, the above formula has been modeled here anew to incorporate the effect of GPA and adjacent ground tracks, as discussed in the introduction. Equations (A1.3) and (A1.4) give the modified impedance formulae for a microstrip line over a GPA and that guarded by ground tracks, respectively.

\[
Z = \frac{6.5 \varepsilon_r^{0.5} W_S}{b_2} + Z_{\text{Wheeler}}
\]  

(A1.3)

\[
Z = 0.3 \times Z_{\text{Wheeler}} \left(1 + 2.33 \left(1 - e^{-\frac{4.5d}{b_2}}\right)\right)
\]  

(A1.4)

Fig. A1.1 gives a comparison between the formulae presented here and the numerical data obtained from FDTD simulations and measurements. Equations (A1.3) and (A1.4) are found to be accurate within ± 2% for \(1 \leq \varepsilon_2 \leq 20\) and \(0 \leq b_2/\lambda_g \leq 0.03\), i.e. about 6 GHz for 1.59 mm substrates. This incidentally happens to be the frequency of interest in modern high-speed interconnects. The applicability of equations (A1.3) and (A1.4) thus exceeds that of Wheeler's formula significantly. Introduction of GPA leads to substantial reduction in the overlap capacitance, resulting in increased characteristic impedance \(Z\). Also, adjacent ground tracks in Fig. 1b act as terminating planes for the lines of field thus increasing lateral capacitance and reducing characteristic impedance \(Z\). Equations (A1.3) and (A1.4) converge to (A1.1) when the GPA width \(W_S\) reduces to zero in (A1.3) or when the spacing \(d\) increases significantly in (A1.4). Although limited cases are illustrated in Figs. A1.1, equations (A1.3) and (A1.4) are found to be accurate for all types of materials and substrate heights. To the best of the authors' knowledge previously reported literature is either devoid of any analytical model for such type of interconnect structures or is too laborious. Thus the present work gains significance in light of the above discussions.
Fig. A1.1a. Microstrip line with GPA (Line width $w = 1$ mm, height of dielectric $h_2 = 0.254$ mm, line thickness $t = 0.003$ mm, line length $l = 20$ mm, and frequency $f = 6$ GHz)
Fig. A1.1b Microstrip line guarded by ground tracks (Line width $w = 1$ mm, height of dielectric $h_2 = 1.59$ mm, line thickness $t = 0.003$ mm, line length $l = 20$ mm, and frequency $f = 6$ GHz)
Appendix II

Design data on single microstrip-like interconnects – Characteristic impedance, capacitance, and inductance

In this section, exhaustive design data is presented for the characteristic impedance, line capacitance, and line inductance of the single line interconnects discussed in chapters 3, 4, and 5. The results presented here were obtained using the analytical models developed in these chapters. The design data is presented for $w/b_2 \leq 1$ and for $w/b_2 > 1$ in separate tables. The data is presented for $\varepsilon_2 = 2.2, 4.6, 9.9, \text{ and } 11.9 \text{ and } b_2 = 0.254 \text{ mm, } 0.508 \text{ mm, } 0.79 \text{ mm, and } 1.59 \text{ mm.}$ The presented design data may be useful to practicing engineers and scientists. The design data is given in a CDROM at the end of this thesis.
Appendix III

*FastEx*: A fast parameter extractor for high-speed interconnects

*FastEx* is an extraction program for capacitance, inductance, and impedance of high-speed interconnects common in the MCM environment. The program is based on analytical models developed using the variational analysis combined with transverse transmission line technique (*the unified approach*) for a class of transmission line interconnects. *FastEx* provides fast and accurate solution to such a class of problems.

Please find CDROM titled *FastEx* containing the software at the end of the thesis.
Appendix IV

List of publications


3. Rohit Sharma, T. Chakravarty, and A. B. Bhattacharyya, “Characteristic impedance of microstrip-like interconnects guarded by ground tracks”, Proceedings of the *XXIX URSI General Assembly*, Chicago, August 2008. (This work was supported by the Department of Science and Technology, Ministry of Science and Technology, New Delhi-110091, vide letter # SR/ITS/01313/2008-2009)


11. *FastEx: A fast parameter extraction program for high-speed interconnects*, Patent filing under process

12. Rohit Sharma “Mitigation of Signal Overshoots in High-Speed Interconnects via Adjacent Ground Lines”, communicated to *Journal of Computational Electronics, Springer*.