CHAPTER 4  
PWM STRATEGIES FOR INVERTERS WITH  
FLUCTUATING DC LINK INPUT  

4.1 INTRODUCTION  

The modified SPWM control schemes (MSPWM-T and MSPWM-S) [59] have served to achieve the desired fundamental and eliminate lower order harmonic components caused by the dc voltage source fluctuation. However, these analog based solutions are effective only at high switching frequencies and resulted in higher switching losses, besides being indirect in nature. 

It is normally assumed that the dc-link is a perfect constant dc voltage. However, in a practical system, it contains ripple components due to the rectification process. An analysis of the power conversion process shows that the power at the dc-link consists of constant active power as well as a pulsating component that fluctuates at twice the mains frequency. When a VSI is powered by the fluctuating dc-link voltage, it generates additional sub-harmonics because of the modulation between the inverter switching function and the dc-link ripple [97]. Moreover, the ripple in the dc-link is the primary contributor for the appearance of harmonics in the inverter output not present in the PWM switching function [98] and is responsible for the deterioration in the quality of the output voltage. Further the harsh loads on the inverter power supply contribute to waveform distortion and introduce abnormal harmonics in the inverter input current. The switching action further creates ripples at the dc-link. 

The input voltage distortion in a voltage source PWM controlled inverter will limit the amplitude of the fundamental and introduce unexpected lower order harmonics [56]. The use of conventional harmonic reduction techniques ends up only with the reappearance of the lower order harmonics in the output waveform. It is only appropriate that the next generation PWM modulators for inverters be inherently capable of rejecting the dc-link voltage ripple to offer a higher quality of output voltage. Therefore, there is a need to innovate a PWM switching strategy, which offers an
enhanced performance compared to existing methods in terms of minimal lower order harmonics, reduced THD and enhanced fundamental, especially at low switching frequencies.

4.2 PROBLEM FORMULATION

The distorted input due to the improper value of dc-link capacitor in an ac-ac PWM conversion system introduces lower order harmonics and increases the THD [56], as seen in Fig.4.1. The objective is to develop a low frequency, PPWM strategy, which will render an improved performance in terms of minimal lower order harmonics and reduced THD for inverters with fluctuating dc input. A new PWM technique is proposed for a single-phase inverter to reduce the lower order harmonics caused by the fluctuating dc input. The width of the PWM pulses in this approach is determined by making the area of the PWM signal equal to that under the sampled reference waveform.

![Output voltage and frequency spectrum of SPFB with fluctuating dc input](image)

Fig.4.1 Output voltage and frequency spectrum of SPFB with fluctuating dc input 
($V_s=230V, C=23.5\mu F$)
4.3 PROPOSED CONTROL STRATEGIES

Three slightly different approaches are formulated under the general area equalization technique, viz. (i) equal sampling technique (EST), (ii) centroid based technique (CBT) and (iii) modified centroid based technique (MCBT).

(i) Equal sampling technique: The width of the PWM pulse is determined by making the area under the PWM signal equal to that under the reference waveform [99]. Unlike the SPWM method, the triangular carriers are not compared with the modulating waveform, and therefore this method shown in Fig.4.2 is more direct for producing the PWM pattern. The width of each pulse is made directly proportional to the corresponding magnitudes of the target output fundamental waveform, $v_1(t)$. The center of each pulse is located at the middle of each sampling period.

The pulse width is directly determined by finding the area of the target fundamental component for each sampling interval irrespective of the distortion level. The pulse width ($\tau_k$) at each sampling period is calculated by approximating the area under the distorted signal as a combination of rectangular and triangular sections as shown in Fig.4.2 and making it equal to the area under the sampled reference as given below.

$$V_{s1} \tau_k + 0.5 \tau_k (V_{s2} - V_{s1}) = \int_{t_1}^{t_2} V_m \sin \omega t \, dt$$

$$\tau_k = \frac{V_m (\cos \omega t_k - \cos \omega t_k)}{V_{s1} + 0.5 (V_{s2} - V_{s1})}$$

(4.1)

(4.2)

where, $V_m$ is the maximum value of the desired (fundamental) output voltage, $v_1(t)$; $V_{s1}$ and $V_{s2}$ are the $s^{th}$ and $(s+1)^{th}$ sampled values of the dc-link voltage. The AEPWM technique is suitable for inputs with any degree of distortion since it is only the areas that are equated.
Fig. 4.2 Equal sampling technique

(ii) Centroid based technique: The horizon of the EST is extended to include a centroid based approach [100] that finds the pulse width in a manner similar to EST, but additionally it relocates the pulse position. The centroid of the sampled reference area in time axis is given by

\[
X_4 = \frac{\int_{t_a}^{t_b} t |\sin \omega t| dt}{\int_{t_a}^{t_b} |\sin \omega t| dt} \left[ \frac{\omega \cos \omega t - \sin \omega t}{\omega \cos \omega t + \sin \omega t} \right]_{t_a}^{t_b} \tag{4.3}
\]

(iii) Modified centroid based technique: A third method of determining the pulse position is to use the center of integration (COI) of the sampled irregular reference area in time axis as shown in (4.4).

\[
X_{4, \text{COI}} = \frac{1}{\omega} \cos^{-1} \left( \frac{\cos \omega t_a + \cos \omega t_b}{2} \right) \tag{4.4}
\]
4.4 SIMULATION RESULTS

When the inverter is connected to the rectifier, the filtered output is superimposed with high frequency ripples in addition to the distortions due to insufficient filtering. The circuit conditions are ac input=230V, capacitor, C=23.5μF and pulse number per cycle, z=40. The simulation is performed using Matlab. The results presented are chosen to provide a comparative basis for evaluating the performance of AEPWM techniques. The switching patterns are generated so as to provide a fundamental ac output of 255V. Fig.4.3 shows the frequency spectra with AEPWM techniques, which substantiates that the lower order harmonic components are almost less than five percent and hence within acceptable limits. Further it follows that the PWM pattern obtained using AEPWM techniques will enable the inverter to generate a much better spectra of output compared to the analog based MSPWM.

The SPWM and MSPWM methods are compared with the AEPWM methods for the fundamental (V₁), lower order harmonics (V₃, V₅ and V₇) and THD in Table 4.1. There is a considerable increase in the fundamental; the lower order harmonics are significantly reduced, besides a marginal reduction in THD in the AEPWM methods.
Fig. 4.3 Frequency spectra with MSPWM and AEPWM methods
Table 4.1 Comparison of SPWM, MSPWM and AEPWM methods

<table>
<thead>
<tr>
<th>Index</th>
<th>SPWM</th>
<th>MSPWM</th>
<th>EST</th>
<th>CBT</th>
<th>MCBT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_1$ (V)</td>
<td>230.40</td>
<td>246.30</td>
<td>253.00</td>
<td>256.30</td>
<td>255.80</td>
</tr>
<tr>
<td>$V_3$ (% of $V_1$)</td>
<td>19.43</td>
<td>7.84</td>
<td>5.29</td>
<td>3.50</td>
<td>3.92</td>
</tr>
<tr>
<td>$V_5$ (% of $V_1$)</td>
<td>3.83</td>
<td>4.88</td>
<td>4.76</td>
<td>4.60</td>
<td>5.42</td>
</tr>
<tr>
<td>$V_7$ (% of $V_1$)</td>
<td>5.82</td>
<td>3.77</td>
<td>1.19</td>
<td>3.78</td>
<td>4.66</td>
</tr>
<tr>
<td>THD (%)</td>
<td>65.96</td>
<td>59.38</td>
<td>55.59</td>
<td>53.93</td>
<td>53.95</td>
</tr>
</tbody>
</table>

4.5 HARDWARE IMPLEMENTATION

With the availability of low cost DSP chips, characterized by improved performance, high speed and reduced instruction set computing (RISC), complicated control algorithms can be executed in real-time, offering a high sampling rate for digitally-controlled inverters [101, 102].

The Texas instruments TMS320LF2407 DSP [103] controller (referred to as LF2407) is a programmable digital controller with a C2XX DSP central processing unit (CPU) as the core processor. The LF2407 contains the DSP core processor and useful peripherals integrated onto a single piece of silicon. It combines the powerful CPU with an on-chip memory and peripherals. It has a 16 bit fixed point arithmetic unit, a 40MHz CPU clock and several peripherals such as event manager (EV), controller area network (CAN) interface, serial peripheral interface (SPI), serial communications interface (SCI) and ADC modules. The 240x series of TI DSP combines this real-time processing capability with controller peripherals to create an ideal environment for control applications. The peripherals in the LF2407 enable virtually any application possible in the range from analog to digital conversion to
PWM generation. The LF2407 peripheral set includes two EVs, general purpose timers, PWM generators, CAN, analog-to-digital converter, SPI port, SCI-asynchronous serial port, watchdog timer and general-purpose bidirectional digital I/O (GPIO) pins.

The two EVs (EV A/B) in the board are identical to one another in terms of functionality and register/bit definition, but have different register names and addresses. Each EV has its own local interrupt subsystem, which includes its own interrupt mask and flag registers. There are two general-purpose (GP) timers in each module. The full compare units (1, 2 & 3) and (4, 5 & 6) in EVA and EVB modules respectively; enable logging of transitions on capture input pins. The value of the GP timer 1 counter is continuously compared with that of the compare register. When a match is achieved, a transition appears on the two outputs of the compare unit according to the bits in the action control register (ACTRA). The outputs of the compare units in the compare mode are subject to modification by the output logic, dead band units, and the SVPWM logic.

The proposed dc-link fluctuation compensation method is tested on a SPFB inverter system, built using IRF840 MOSFET devices. The uncontrolled rectifier is realised by 6A4 MIC diodes. The rectified output through a filter capacitance serves as an input to the inverter. The LF2407 has the necessary features to allow easy implementation of AEPWM techniques in an inverter with distorted dc input. The input is sensed accurately and fed to the DSP controller through a hall-effect voltage sensor LV25-P14048 seen in Fig.4.4. The closed loop model of the arrangement is shown in Fig.4.5.
Fig. 4.4 LV25-P 14048 voltage sensor

Fig. 4.5 Block diagram of a closed loop digitally controlled ac-ac system
The SPWM is a pulse train generated directly by comparing a sinusoidal reference signal with a carrier signal of higher frequency. The effectiveness in digital implementation of SPWM lies in efficient reproducing of look-up-table (LUT) based natural sampled functions. The flow chart of the algorithm of SPWM generation is shown in Fig.4.6. The effectiveness of the algorithm in generating SPWM pulses for a typical $M_n$ and $M_f$ values are demonstrated in Fig.4.7 and verified in Table 4.2. The SPWM and EST techniques use the timer continuous up mode while CBT and MCBT use continuous up/down mode due to the requirement of loading two counts in between overflow and underflow. The LF2407 registers are initialised in a manner similar to as that for the SPWM method. The pulse widths and the pulse positions are computed such that they match the LF2407 timer values and stored in compare unit buffer register. The timer period (T1PR) for the EST method is loaded with 19200 for $z=20$ according to the equation (4.5).

$$T1PR \text{ value} = \left[ \frac{\text{Desired PWM period}}{2 (\text{GP timer prescaled clock period})} \right]$$  \hspace{1cm} (4.5)

The values of T1PR for CBT and MCBT are loaded with 38400 for $z=20$ according to the equation (4.6).

$$T1PR \text{ value} = \left[ \frac{\text{Desired PWM period}}{\text{GP timer prescaled clock period}} \right]$$  \hspace{1cm} (4.6)

The PWM pulses are generated when a compare match occurs as set by the ACTRA. The PWM channels of the event manager in the LF2407 are used to generate the pulses. The PWM pins PWM1, PWM2, PWM3 and PWM4 are used to trigger the inverter switches.
Fig. 4.6 Algorithmic steps of SPWM for LF2407 implementation
Fig. 4.7 Durations of SPWM pulses ($M_s=1$ and $M_r=10$)
Table 4.2 Accuracy of generated SPWM pulse durations

<table>
<thead>
<tr>
<th>Pulse number</th>
<th>Pulse width (μS)</th>
<th>Simulation</th>
<th>DSP output</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/9</td>
<td>315</td>
<td>312</td>
<td></td>
</tr>
<tr>
<td>2/8</td>
<td>594</td>
<td>592</td>
<td></td>
</tr>
<tr>
<td>3/7</td>
<td>809</td>
<td>816</td>
<td></td>
</tr>
<tr>
<td>4/6</td>
<td>942</td>
<td>944</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>988</td>
<td>984</td>
<td></td>
</tr>
</tbody>
</table>

The experimental results are obtained for an ac input voltage of 230V using the arrangement shown in Fig.4.8. The dc-link voltage ripple for a capacitor value of 23.5μF is found to be fifty percent as shown in Fig.4.9. The inverter output voltage waveforms with EST for the same capacitor value is shown in Fig.4.10 and the frequency spectra with SPWM and the AEPWM methods are given in Fig.4.11. It is found that the dc-link voltage is considerably disturbed in compliance with the frequency of the PWM signal. The voltage spectrum obtained with SPWM illustrates that lower order harmonics are introduced in the output voltage. The frequency spectra with AEPWM techniques substantiate the close comparison of experimental and simulated performances in terms of reduced lower order harmonics. Table 4.3 validates the effectiveness of the DSP based implementation of the proposed strategies.
Fig. 4.9 Fluctuation in dc-link voltage

Fig. 4.10 Inverter output voltage with EST
Fig. 4.11 Frequency spectra of experimentally obtained output voltages

The inverter output voltage obtained using the AEPWM (EST) method with out a dc-link capacitor is shown in Fig. 4.12. Fig. 4.13(a) and Fig. 4.13(b) further highlight the fact that the system can work even without the capacitor, besides allowing a saving in space without any compromise on reliability and life time of the system even at higher ambient temperatures. Table 4.4 depicts comparison of lower order harmonics and THD of SPWM and EST for without the dc-link capacitor.

Fig. 4.12 Inverter output voltage with EST, without dc-link capacitor
Table 4.3 Comparison of AEPWM methods

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Simulation/Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EST</td>
</tr>
<tr>
<td>$V_1$</td>
<td>253.0/252.78</td>
</tr>
<tr>
<td>$V_3$</td>
<td>5.29/5.14</td>
</tr>
<tr>
<td>$V_5$</td>
<td>4.76/5.28</td>
</tr>
<tr>
<td>$V_7$</td>
<td>1.19/2.21</td>
</tr>
<tr>
<td>THD</td>
<td>55.59/54.62</td>
</tr>
</tbody>
</table>

Fig. 4.13 Frequency spectra with SPWM and EST without dc-link capacitor

Table 4.4 Comparison of lower order harmonics and THD without dc-link capacitor

<table>
<thead>
<tr>
<th>Techniques</th>
<th>$V_3$ (%) of $V_1$</th>
<th>$V_5$ (%) of $V_1$</th>
<th>$V_7$ (%) of $V_1$</th>
<th>THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPWM</td>
<td>27.2</td>
<td>11.4</td>
<td>2.8</td>
<td>67.93</td>
</tr>
<tr>
<td>EST</td>
<td>1.3</td>
<td>1.2</td>
<td>1.7</td>
<td>59.11</td>
</tr>
</tbody>
</table>
4.6 SUMMARY

The AEPWM techniques have served to provide compensation for the PWM inverters working with fluctuating dc input. The lower order harmonic components, which increase the filter size and cost, are well reduced by using AEPWM techniques. The proposed AEPWM methods are a low switching frequency solution to the dc voltage fluctuation, thus reducing the switching losses. The simulation results have revealed the superiority of the proposed strategy over the existing MSPWM. The experimental solutions that compares closely with the simulated results indicate that this approach can be implemented in a digital platform even in a fluctuating dc environment. The implemented strategy has brought out the suitability of the schemes for applications such as aircraft power supplies; UPS in computer system, traction drives, and drives for communication satellites and launch vehicles.