CHAPTER 3

ANALYSIS OF TRANSFORMERLESS PV INVERTER TOPOLOGIES

3.1 INTRODUCTION

Leakage current and DC injection have been the major concern with transformerless PV inverters. The influence of parasitic capacitance values on leakage current has not been investigated before. The common mode voltage model proposed by Gubia et al (2007) has been widely accepted. The effect of filter inductor imbalances on common mode voltage for DC bypass topologies was not investigated in previous literature. The harmonic spectrum of leakage current for different parasitic capacitance values have not been dealt with before. The parasitic capacitance values are varied from 1µF to 10 µF, considering humid conditions.

Blewitt et al (2010), Berba et al (2012) etc have studied the issue of DC injection in transformerless PV inverters. The effect of varying parasitic capacitance values have not been considered in literature. The effects of output filter inductors and series capacitance on DC injection values for different topologies have not been studied previously.

This chapter gives a detailed analysis of common mode model of single phase inverter. Five H-Bridge derived topologies have been selected for analysis of leakage current through the parasitic capacitance and also DC injection in the output of the inverter (Ozkan et al 2012). Analysis has been
done for varying values of parasitic capacitance. The effects of output series capacitance and filter inductor imbalances have also been investigated. The five topologies under consideration are as follows:

i) H-Bridge with Bipolar PWM  
ii) H-Bridge with Unipolar PWM  
iii) H-Bridge with Hybrid PWM  
iv) H-Bridge with DC Bypass (one switch) or DC Bypass 1  
v) H-Bridge with DC Bypass (two switches) or DC Bypass 2

The filter configuration is as given in Figure 3.1, and the simulations were performed in MATLAB/SIMULINK

![Figure 3.1 Filter Configuration](image)

The filter inductor is split equally between the two branches. The influence of filter parameters on leakage current has been investigated. The LCL is used for grid side filter (Lopez et al 2007, Yang et al 2012).

The parameters used for simulation are summarized in the Table 3.1. DC bus voltage is restricted below 750v to avoid insulation failure (Chatopadhyay et al 2012).
Table 3.1 Parameters Used

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching frequency</td>
<td>10 kHz</td>
</tr>
<tr>
<td>DC link Capacitance</td>
<td>1 mF</td>
</tr>
<tr>
<td>Filter Inductance</td>
<td>1.8 mH</td>
</tr>
<tr>
<td>Filter Capacitance</td>
<td>2 μF</td>
</tr>
<tr>
<td>Grid Voltage</td>
<td>325 V (peak)</td>
</tr>
<tr>
<td>DC Voltage</td>
<td>450V</td>
</tr>
</tbody>
</table>

3.2 COMMON MODE VOLTAGE ANALYSIS

The galvanic connection between PV inverter and the grid pauses the problem of leakage current and DC injection. The path of leakage current flow, the parasitic capacitance, line inductances, transformer winding capacitance etc are shown in Figure 3.2 (Kerekes et al 2008a).

Figure 3.2 Model of Inverter with stray elements

The description of stray elements shown in figure are given below

- $C_{LG}$ - This is the parasitic capacitance that exist between the line and ground
• $C_{PV}$ - Parasitic capacitance between PV panel and frame

• $C_{W}$ - Parasitic capacitance between primary and secondary winding of the transformer

• $L_{R}, L_{Y}$ - The output inductors used to control the current

• $L_{g}$ - Grid side inductor

For PV inverters with galvanic isolation, the stray capacitance between transformer windings offer impedance to DC current and therefore the DC injection is not much influenced by topology or PWM technique used in inverters. The common mode currents below 50Hz are also much reduced in case of inverters with isolation. However, in case of transformerless inverters, since stray capacitance across winding is absent the topology as well as modulation techniques can be effectively modified to limit DC injection.

The common mode voltage existing between R and Y terminals of the line is obtained, where $V_{CM-RY}$ and $V_{DM-RY}$ are the common mode and differential mode voltage between lines R and Y respectively (Vasquez et al 2009, Kerekes et al 2008a). $V_{RN}$ and $V_{YN}$ are the output voltages of the inverter with respect to the negative terminal N of the DC bus reference. $V_{CM-RY}$ and $V_{DM-RY}$ are defined as

$$V_{CM-RY} = \frac{V_{RN} + V_{YN}}{2} \quad (3.1)$$

$$V_{DM-RY} = V_{RN} - V_{YN} \quad (3.2)$$
From equations (3.1) & (3.2)

\[ 2V_{CM_{RY}} = V_{RN} + V_{YN} \]  

(3.3)

\[ V_{DM_{RY}} = V_{RN} - V_{YN} \]  

(3.4)

Adding equations (3.3) & (3.4)

\[ 2V_{RN} = 2V_{CM_{RY}} + V_{DM_{RY}} \]  

(3.5)

\[ V_{RN} = V_{CM_{RY}} + \frac{V_{DM_{RY}}}{2} \]  

(3.6)

Similarly,

\[ V_{YN} = V_{CM_{RY}} - \frac{V_{DM_{RY}}}{2} \]  

(3.7)

Equations (3.5) & (3.6) can be modeled as

\[ \text{Figure 3.3 Model of common mode and differential mode voltages} \]
Re-modeling the diagram

![Diagram of Thevenin Model of the Inverter](image)

**Figure 3.4 Thevenin Model of the Inverter**

Writing the mesh equation

\[
\frac{1}{2} V_{DM_{-}RY} - I X_{L_g} - I X_{L_y} + \frac{1}{2} V_{DM_{-}RY} = 0
\]  \hspace{1cm} (3.8)

\[V_{DM_{-}RY} = I (X_{L_y} + X_{L_g})\]  \hspace{1cm} (3.9)

\[I = \frac{V_{DM_{-}RY}}{X_{L_g} + X_{L_y}}\]  \hspace{1cm} (3.10)

\[V_{ry} = \frac{1}{2} V_{DM_{-}RY} - X_{L_g} \left( \frac{V_{DM_{-}RY}}{X_{L_g} + X_{L_y}} \right)\] \hspace{1cm} (3.11)

\[V_{ry} = \frac{V_{DM_{-}RY}}{2} \left( \frac{X_{L_y} - X_{L_g}}{X_{L_y} + X_{L_g}} \right)\] \hspace{1cm} (3.12)

\[V_{ry} = \frac{V_{DM_{-}RY}}{2} \left( \frac{L_R - L_y}{L_R + L_y} \right)\] \hspace{1cm} (3.13)
The model of effective common mode voltage is shown in figure.

\[ V_{CM_{\text{EFF}}} = V_{CM_{\text{RY}}} + V_{ry} \] \hspace{1cm} (3.14)

This voltage depends on \( L_Y \) and \( L_R \) values and can be made zero if \( L_Y = L_R \)

### 3.3 H-BRIDGE DERIVED TOPOLOGIES

#### 3.3.1 H-Bridge with Bipolar PWM

H-Bridge, first developed by McMurray in 1965, has been a widely accepted topology. It was the first structure that utilized the force commutated semiconductor devices. It finds use in motor drives, UPS etc. It can be used in both DC-DC and DC-AC conversion.
There are four switches arranged in two legs in this configuration as seen in Figure 3.6. These four switches can be switched using PWM techniques. Bipolar is a direct PWM technique where in a sinusoidal modulating signal is compared with triangular wave of required switching frequency. These pulse obtained are used to turn ON switches S1 & S4. The modes of operations are shown in Figures 3.7 (a) & 3.7 (b). S2 & S3 are switched complementarily to S1 & S4 as given in Figures 3.8 (a) & 3.8 (b). A two level output is obtained which means output voltage switches from $+V_{DC}$ to $-V_{DC}$ (Gubia et al 2007, Teoderscu et al 2011).
In bipolar modulation the diagonal switches in two legs are switched simultaneously (San et al 2012).

Features of this scheme are

- Two legs are switched such that S1 & S4 are switched synchronously and complementary to S2 & S3
- Same sinusoidal reference for generating switching reference for both legs
- The output current ripple has the same frequency as that of switching and hence filtering requirements are higher
- The output voltage switches from $+V_{DC}$ to $-V_{DC}$ resulting in high core losses in filter inductor
- Efficiency is nearly 96.5%
- Low efficiency is the result of reactive power exchange between filter inductor and DC link capacitor
- There is no zero output voltage state.
3.3.2 H-Bridge with Unipolar PWM

In unipolar PWM switching, the diagonal switches in the legs of the H-Bridge are not always switched simultaneously as in the bipolar PWM technique. In this technique sinusoidal and mirrored sinusoidal reference are used as modulating signal for each of the legs. These two references are compared with the same triangular wave to generate pulses. Several new types of unipolar are being investigated to adapt it in transformerless topologies (Cui et al 2011, Gu et al 2011 and Yang et al 2012).

The switching scheme is given below

i) S1 & S4 ON, $V_{RN} = +V_{DC}$, $V_{YN} = 0$, $V_O = +V_{DC}$
ii) S2 & S3 ON, $V_{RN} = 0$, $V_{YN} = +V_{DC}$, $V_O = -V_{DC}$
iii) S1 & S3 ON, $V_{RN} = +V_{DC}$, $V_{YN} = +V_{DC}$, $V_O = 0$
iv) S2 & S4 ON, $V_{RN} = 0$, $V_{YN} = 0$, $V_O = 0$

The modes of operation are shown in Figures 3.9(a), 3.9(b), 3.9 (c), 3.9 (d), 3.9 (e) & 3.9 (f). When both S1 and S3 are ON, the output voltage is zero. The current circulates in a loop through S1 & D3 or D1 & S3, depending on the direction of current. Similar condition occurs when S2 & S4 are ON. The switching scheme and output of unipolar PWM is shown in Figures 3.10 (a)&3.10 (b).

![Figure 3.9 H-Bridge Inverter with Unipolar PWM Modes of operation](a)
Figure 3.9  (continued) H-Bridge Inverter with Unipolar PWM Modes of operation b) Mode 2 c) Mode 3 d) Mode 4
Figure 3.9 (continued) H-Bridge Inverter with Unipolar PWM Modes of operation e) Mode 5 f) Mode 6

Figure 3.10 a) Switching Scheme for Unipolar PWM b) Unipolar output
The output voltage swings between 0 and \( +V_{\text{DC}} \) and 0 and \( -V_{\text{DC}} \). The voltage jump is therefore reduced to \( V_{\text{DC}} \) compared to \( 2V_{\text{DC}} \) in bipolar. The output voltage has a frequency equal to twice the switching frequency. To obtain the same output frequency as that of bipolar switching, the carrier frequency has to be reduced to half (Mohan et al 2002, Barater et al 2012a, Yang et al 2012).

Features

- The output current ripple is twice the switching frequency and hence the filtering requirements are lowered.
- The voltage output across the filter has swings between 0 to \( +V_{\text{DC}} \) and 0 to \( -V_{\text{DC}} \) and therefore filter inductor core losses are reduced.
- Efficiency is 98%
- Higher efficiency due to relatively lower reactive power exchange between filter inductor and DC link capacitor. Due to zero output states.

3.3.3 H-Bridge with hybrid PWM

In hybrid modulation, one leg is switched at grid frequency and the other leg at switching frequency. In this way, the neutral line of the topology is connected either to the positive or the negative terminal, considering the half period of the reference signal (Lai & Ngo 1995, Teodercu et al 2011).

The switching scheme is similar to unipolar PWM given as

i) \( S1 \& S4 \) ON, \( V_{\text{RN}} = +V_{\text{DC}}, V_{\text{YN}} = 0, V_{\text{O}} = +V_{\text{DC}} \)

ii) \( S2 \& S3 \) ON, \( V_{\text{RN}} = 0, V_{\text{YN}} = +V_{\text{DC}}, V_{\text{O}} = -V_{\text{DC}} \)
iii) S1 & S3 ON, \( V_{RN} = +V_{DC}, V_{YN} = +V_{DC}, V_{O} = 0 \)

iv) S2 & S4 ON, \( V_{RN} = 0, V_{YN} = 0, V_{O} = 0 \)

The modes of operation is shown in Figures 3.11(a), 3.11(b), 3.11(c) & 3.11(d) and switching scheme and output waveform is given in Figures 3.12 (a)&3.12 (b).

Figure 3.11  H-Bridge Inverter with Hybrid PWM- Modes of operation
a) Mode1 b) Mode2
Figure 3.11  (continued) H-Bridge Inverter with Hybrid PWM- Modes of operation  c)Mode3 d) Mode4

Figure 3.12 a) Switching Scheme for Hybrid PWM b) Hybrid output.
Features

- The output current ripple is equal to switching frequency as in bipolar resulting in high filtering requirements.
- This modulation has limited application since it can work for a two quadrant operation only.
- Efficiency is 98%
- There is very low reactive power exchange between filter inductor and DC link capacitor

3.3.4 H-Bridge with DC Bypass (One Switch)

H-Bridge with DC Bypass (one Switch) inverter topology is patented by SMA in 2005. This topology is a typical H-Bridge topology with an additional fifth switch in the positive DC bus (Wang et al 2012, Zhang et al 2013). The uses of this switch are to prevent reactive power exchange between filter inductor and DC link capacitor during zero voltage states and as an isolation of PV module from grid during zero state. S5, S4 and S2 are switched at high frequency and S1 & S3 at grid frequency. S1 is ON throughout the positive cycle while S3 is ON throughout the negative cycle of the reference voltage.

![Figure 3.13 H-Bridge with DC Bypass (one Switch)](image)
For positive current flow, S5, S4 are ON simultaneously, and S1 is ON, the current flows through S5, S1 and returns through S4. Similarly for negative current flow, S5 and S2 are ON, S3 is ON, current flows through S5-S3 and returns through S2. During zero state, S5 and S4 are turned off, current freewheels through S1-S3. The modes operation is given in Figures 3.14 (a), 3.14(b), 3.14(c) & 3.14(d). The switching scheme and output of the inverter is shown in Figures 3.15 (a)&3.15 (b).

![Diagram](image)

Figure 3.14  H-Bridge Inverter with DC bypass (one Switch)- Modes of operation  a)Model1  b) Mode2
Figure 3.14  (continued) H-Bridge Inverter with Dc bypass (one Switch)-Modes of operation  c) Mode 3 d) Mode 4

Figure 3.15  a) Switching Scheme for DC bypass 1 b) DC bypass 1 output
Features

- Voltage output swings from 0 to $+V_{DC}$ to 0 to $-V_{DC}$. Therefore filter inductor core losses are reduced.
- Efficiency is 98%
- There is no reactive power exchange between filter inductor and DC link capacitor
- Higher conduction losses because three switches are conducting during active state.

3.3.5 H-Bridge with DC Bypass (Two Switches)

This is a typical H-Bridge with two additional switches in the positive and negative DC bus and also two extra diodes clamping the output to the grounded middle point of the DC bus. The extra switches ensure that zero voltage is grounded unlike in DC bypass 1 where the zero voltage is floating. For active state, S5 and S6 are switched at high frequency, S1 and S4 are switched with grid frequency and complementary to S2, S3, depending on whether the modulating signal is in the positive or negative half cycle (Xu et al 2012, Wang et al 2012, Zhang et al 2014).

![Figure 3.16 H-Bridge with DC Bypass (Two Switches)](image)
Features

- The output voltage swings from 0 to \(+V_{DC}\) to 0 to \(-V_{DC}\) and hence there is lower coreloss in the filter inductor.
- Efficiency is higher due to no reactive power exchange between filter inductor and DC link capacitor.
- Four switches are conducting during active state and hence conduction losses increase.

The modes of operation are shown in Figures 3.17 (a), 3.17(b), 3.17(c) & 3.17(d). The switching scheme of H-Bridge with DC bypass (two switches) and output waveform is given in Figures 3.18 (a) & 3.18 (b).

![Diagram](image1)

Figure 3.17 H-Bridge Inverter with DC bypass (two switches)- Modes of operation a) Mode 1 b) Mode 2
Figure 3.17 (Continued) H-Bridge Inverter with DC bypass (two Switches)- Modes of operation c) Mode 3 d) Mode 4

Figure 3.18 (a) Switching Scheme for DC bypass 2(b) DC bypass 2 output
3.4 ANALYSIS OF H-BRIDGE TOPOLOGIES

The switching devices used are IGBTs for the simulation. $C_{PV}$ indicate the parasitic capacitance. DC link capacitance is split only in the case of DC bypass 2 topology, all others use single capacitance at the DC link. The filter inductors are split between phase and neutral for balancing the common mode voltage which is shown in analysis.

3.4.1 Leakage Current Analysis

This section analyses the leakage current for five H-Bridge derived topologies. The leakage current is measured using setup shown in Figure 3.19. The filter configuration is as shown in Figure 3.1. The parasitic capacitance is varied from 1 to 10 $\mu$F and the leakage current values are noted.

![Figure 3.19 H-Bridge Topology](image)

3.4.1.1 H-Bridge with Bipolar PWM

The common mode voltage for bipolar PWM is calculated as per Equation (3.15). The effective common mode for bipolar PWM is found
constant with balanced filter inductors where as it varies with imbalances in filter inductors.

Consider the equation for effective common mode voltage

\[
V_{CM\_EFF} = V_{CM\_RY} + \frac{V_{DM\_RY}}{2} \left( \frac{L_\gamma - L_R}{L_\gamma + L_R} \right)
\]  

(3.15)

For \(L_\gamma = 0\), \(V_{CM\_EFF} = V_{YN}\)

For \(L_\gamma = L_R\), \(V_{CM\_EFF} = V_{CM\_RY}\)

**Table 3.2  Effective Common Mode voltage for Bipolar PWM for \(L_\gamma=0\) and \(L_\gamma=L_R\)**

<table>
<thead>
<tr>
<th>Bipolar</th>
<th>(V_{CM_EFF} \text{ for } L_\gamma=0)</th>
<th>(V_{CM_EFF} \text{ for } L_\gamma=L_R)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1,S4 ON</td>
<td>0</td>
<td>(V_{DC}/2)</td>
</tr>
<tr>
<td>S2,S3 ON</td>
<td>(V_{DC})</td>
<td>(V_{DC}/2)</td>
</tr>
</tbody>
</table>

From Table 3.2, it can be seen that the effective common mode for bipolar PWM is found constant with balanced filter inductors where as it varies with imbalances in filter inductors. The magnitudes of leakage current values are reduced in bipolar PWM with balanced filter inductors.

**Analysis**

The operation of bipolar PWM ensures constant common mode voltage and hence voltage across parasitic capacitance has lower switching frequency components and hence lower leakage current. The leakage current waveforms for two values of parasitic capacitance – 1 \(\mu\)F and 10 \(\mu\)F are shown for balanced filter inductors in Figures 3.20 (a) and 3.21(a) respectively and the FFT analysis of both waveforms are shown in Figures
3.20(b) and 3.21(b). For lower values of parasitic capacitance the harmonics are very pronounced while for increasing values of parasitic capacitance, the fundamental current increases in magnitude and fifth order harmonics are more pronounced while higher order harmonics are not so much increased. The common mode behavior of bipolar PWM technique is excellent, but the prospectus of use of bipolar PWM in transformerless inverters is limited by low efficiency and output power quality.

![Figure 3.20a](image1.png)

(a) Leakage Current for parasitic capacitance of 1uF in Bipolar PWM

![Figure 3.20b](image2.png)

(b) FFT Analysis of leakage current.

**Figure 3.20**  a) Leakage Current for parasitic capacitance of 1uF in Bipolar PWM  b) FFT Analysis of leakage current.
Figure 3.21  a) Leakage Current for parasitic capacitance of 10uF in Bipolar PWM  
b) FFT Analysis of leakage current.

For lower values of parasitic capacitance magnitude of harmonic currents are less and for higher values of parasitic capacitance, magnitudes of selected harmonics are higher, which means, as the parasitic capacitance value increases, specific harmonic contents increase. In conclusion, it can be said that lower order (in this case fifth order) harmonics are higher which increases filter requirements. As parasitic capacitance value increases, magnitude of leakage current increases.
3.4.1.2 H-Bridge with unipolar PWM

For unipolar PWM the effective common mode voltage has been investigated using Equation (3.15), which is consolidated in Table 3.3 for different modes of operation.

Table 3.3 Effective Common Mode voltage for Unipolar PWM for $L_Y=0$ and $L_Y=L_R$

<table>
<thead>
<tr>
<th>Unipolar</th>
<th>$V_{CM_EFF}$ for $L_Y=0$</th>
<th>$V_{CM_EFF}$ for $L_Y=L_R$</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1, S4 ON</td>
<td>0</td>
<td>$V_{DC}/2$</td>
</tr>
<tr>
<td>S1, S3 ON</td>
<td>$V_{DC}$</td>
<td>$V_{DC}$</td>
</tr>
<tr>
<td>S2, S3</td>
<td>$V_{DC}$</td>
<td>$V_{DC}/2$</td>
</tr>
<tr>
<td>S2, S4 ON</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The Table 3.3 shows that the effective common mode values vary widely in case of unipolar PWM. The effective common mode voltage has three levels in the case of balanced filter inductor as well.

Analysis

The operation of unipolar does not give constant common mode voltage and hence, voltage across parasitic capacitance consists of high frequency components and hence leakage current increases. The analysis of leakage current in Unipolar PWM is similar to bipolar. For lower values of parasitic capacitance the harmonics of leakage current as shown in Figures 3.22(a) & 3.22(b) and the side bands exists and are distributed evenly for all order of harmonics while for higher value of parasitic capacitance, it is concentrated around fifth order. It can also be observed that the DC component in the leakage current is less for 10uF parasitic capacitance.
The suitability of unipolar PWM is limited due to varying common mode voltage, but compared to bipolar, unipolar offers higher efficiency and better power quality.

Figure 3.22  a) Leakage Current for parasitic capacitance of 1uF in Unipolar PWM  b)FFT Analysis of leakage current.
Figure 3.23  a) Leakage Current for parasitic capacitance of 10uF in Unipolar PWM  b)FFT Analysis of leakage current.

In Unipolar PWM, ground voltage has a high frequency signal super-imposed on it. Power output of converter influences ground current when UPWM is used. It can be concluded that leakage current increases as parasitic capacitance increases and lower order harmonics magnitude increases.
3.4.1.3 H-Bridge with hybrid PWM

<table>
<thead>
<tr>
<th>Hybrid</th>
<th>$V_{CM_EFF}$ for $L_Y=0$</th>
<th>$V_{CM_EFF}$ for $L_Y=L_R$</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1, S4 ON</td>
<td>0</td>
<td>$V_{DC}/2$</td>
</tr>
<tr>
<td>S1, S3 ON</td>
<td>$V_{DC}$</td>
<td>$V_{DC}$</td>
</tr>
<tr>
<td>S2, S3 ON</td>
<td>$V_{DC}$</td>
<td>$V_{DC}/2$</td>
</tr>
<tr>
<td>S2, S4 ON</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The variation in effective common mode voltage is summarized in Table 3.4. In hybrid, the effective common mode voltage varies widely for both combinations of output inductors. The variation of effective common mode voltage is similar to unipolar PWM.

Analysis

In hybrid PWM, for lower value of parasitic capacitance, i.e., 1 $\mu$F, the harmonics are very much pronounced for odd orders as shown in Figures 3.24(a) & 3.24(b), while for higher value of parasitic capacitance the third and fifth are more than seven and nine as shown in Figure 3.25(a) & 3.25(b). Also side bands appear across fifth order. The DC components are negligible for both values of parasitic capacitance. In switching period for hybrid PWM, in which $V_{DM}$, alternates from one half cycle to the other, a voltage step with amplitude equal to $VPV$, takes place in $V_{CM\_EFF}$. As can be seen in the FFT analysis (3.25(b)), ground current peaks are higher than unipolar. This is because, in hybrid PWM, the two legs of the H-Bridge are alternately switched at grid frequency and switching frequency. This amounts to voltage
variations across parasitic capacitance between grid and switching frequency components leading to higher leakage current peaks.

Figure 3.24  a) Leakage Current for parasitic capacitance of 1µF in Hybrid PWM  b)FFT Analysis of leakage current
The efficiency and power quality of hybrid PWM is better off than unipolar. In all the 3 PWM techniques, Bipolar, Unipolar and Hybrid, the harmonic spectrum of leakage current reveals that for larger values of parasitic capacitance, lower order harmonics are higher. This means, the filter requirements are higher for larger values of parasitic capacitances. So as
humidity increases, particularly for thin film solar panels, the parasitic capacitance values may exceed 10µF, and lower order harmonics may enter the grid side if filtering requirements are not adequate.

3.4.1.4 H – Bridge with DC bypass 1

![Diagram of H-Bridge with DC bypass](image)

Figure 3.26 H-Bridge with DC bypass (one switch)

The effective common mode voltage is summarized in Table 3.5.

<table>
<thead>
<tr>
<th>DC Bypass 1</th>
<th>( V_{CM,\text{EFF}} ) for ( L_Y=0 )</th>
<th>( V_{CM,\text{EFF}} ) for ( L_Y=L_R )</th>
</tr>
</thead>
<tbody>
<tr>
<td>S5,S4,S1 ON</td>
<td>0</td>
<td>( V_{DC}/2 )</td>
</tr>
<tr>
<td>S5,S2,S3 ON</td>
<td>( V_{DC} )</td>
<td>( V_{DC}/2 )</td>
</tr>
<tr>
<td>S1 ON</td>
<td>( V_{DC}/2 )</td>
<td>( V_{DC}/2 )</td>
</tr>
<tr>
<td>S3 ON</td>
<td>( V_{DC}/2 )</td>
<td>( V_{DC}/2 )</td>
</tr>
</tbody>
</table>
The fundamental value of leakage currents have decreased for DC bypass 1 topology compared to other topologies. Since the common mode voltage is constant, voltage across parasitic capacitance has lower frequency components and, hence leakage current is reduced. It can be observed from the Table 3.5 that the effective common voltage for DC bypass 1 topology does not vary when line inductors are balanced while it varies when the line

Figure 3.27  a) Leakage Current for parasitic capacitance of 1µF in DC Bypass 1 b) FFT Analysis of leakage current.
inductor is imbalanced. DC bypass 1 topology can be a good option for transformerless inverters, as it maintains effective common mode voltage with balanced filter inductors.

![Figure 3.28](image)

(a) Leakage Current for parasitic capacitance of 10 µF in DC Bypass 1 b) FFT Analysis of leakage current.

Figure 3.28  a) Leakage Current for parasitic capacitance of 10 µF in DC Bypass 1 b) FFT Analysis of leakage current.
In DC bypass 1, for lower values of parasitic capacitance as shown in Figures 3.27(a) & 3.27(b), high frequency component is present in comparatively higher magnitudes. But for higher values of parasitic capacitance, high frequency components are present in lower magnitudes as shown in Figures 3.28(a)& 3.28(b).

3.4.1.5 H-Bridge with DC Bypass 2

![Diagram of H-Bridge with DC bypass](image)

Figure 3.29 H-Bridge with DC bypass (two switches)

The effective common mode voltage is summarized in Table 3.6.

<table>
<thead>
<tr>
<th>DC Bypass 2</th>
<th>$V_{\text{CM-EFF for } L_\gamma=0}$</th>
<th>$V_{\text{CM-EFF for } L_\gamma=L_R}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>S5,S6,S1,S4 ON</td>
<td>0</td>
<td>$V_{\text{DC}/2}$</td>
</tr>
<tr>
<td>S5,S6,S2,S3 ON</td>
<td>$V_{\text{DC}/2}$</td>
<td>$V_{\text{DC}/2}$</td>
</tr>
<tr>
<td>S1 ON</td>
<td>0</td>
<td>$V_{\text{DC}/2}$</td>
</tr>
<tr>
<td>S3 ON</td>
<td>$V_{\text{DC}/2}$</td>
<td>$V_{\text{DC}/2}$</td>
</tr>
</tbody>
</table>
Figure 3.30  a) Leakage Current for parasitic capacitance of 1uF in DC Bypass 2  b) FFT Analysis of leakage current.
Figure 3.31  a) Leakage Current for parasitic capacitance of 10 μF in DC Bypass 2 b)FFT Analysis of leakage current.

Analysis

The fundamental value of leakage current for both values of parasitic capacitance has considerably reduced. This is because, the two DC
bypass switches effectively separates the DC supply and grid during freewheeling modes and reduces the leakage current by clamping the neutral to mid-point of DC link. In DC bypass 2 topology, lower parasitic capacitance exhibit high frequency components as shown in Figures 3.30(a)&(b), while for 10μF capacitance, the second, third, fourth, fifth and sixth harmonics are very pronounced as shown in Figure 3.31(a)&(b). In DC bypass2 topology, high frequency components are present with lower values of parasitic capacitance. But lower order harmonics are present with larger values of parasitic capacitances.

The nature of harmonic spectrum is different for DC bypass1 and DC bypass 2 topologies. Filtering requirements are easier for DC bypass 1 topology irrespective of parasitic capacitance value. In DC bypass 2 topology, filtering requirements vary with values of parasitic capacitance. Higher filtering is needed in DC bypass 2 topologies for larger values of parasitic capacitances.

The overall analysis of leakage current is given below

![Leakage Current Vs Parasitic Capacitance](image)

*Figure 3.32 Leakage Current Vs Parasitic Capacitance*
The effect of varying parasitic capacitance on the leakage current for different topologies is given in Figure 3.32. This chapter evaluates 5 topologies on the basis of leakage current and shows that hybrid switched inverter has the highest leakage current and the topologies with DC bypass has lesser leakage current values. In all the topologies, the fundamental magnitudes of leakage current increases with increasing values of parasitic capacitance.

3.4.2 DC Injection Analysis

The issue of DC injection has been mentioned in the previous sections. An analysis of five inverter topologies based on DC injection in the output current has been done and suitability of inverter structure is proposed.

The analysis is done in MATLAB/SIMULINK environment and FFT analysis of the output current has been done to measure the injected DC in the output. This analysis has been done for varying values of parasitic capacitance, $C_{PV}$ from 1μF to 10μF. The circuit arrangement for the experiment is shown in Figure3.33.

![Figure 3.33 Experimental set up for DC injection analysis and leakage current](image)

**Figure 3.33** Experimental set up for DC injection analysis and leakage current
The filter inductor imbalances and its effect on DC has been measured for all the five topologies. Further the effect of series capacitance connected in the output of the inverter on the DC injection values has also been investigated.

The FFT analysis of the output current for varying values of Parasitic capacitance is tabulated in Table 3.7.

Table 3.7  DC Injection Values for five topologies with varying parasitic capacitance

<table>
<thead>
<tr>
<th>Parasitic Capacitance C_{PVin} μF</th>
<th>Bipolar</th>
<th>Unipolar</th>
<th>Hybrid</th>
<th>DC Bypass1</th>
<th>DC Bypass2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.4824</td>
<td>0.5576</td>
<td>2.664</td>
<td>0.5143</td>
<td>0.5133</td>
</tr>
<tr>
<td>2</td>
<td>0.4828</td>
<td>0.5578</td>
<td>2.664</td>
<td>0.516</td>
<td>0.5139</td>
</tr>
<tr>
<td>3</td>
<td>0.4823</td>
<td>0.5575</td>
<td>2.665</td>
<td>0.5175</td>
<td>0.5148</td>
</tr>
<tr>
<td>4</td>
<td>0.4832</td>
<td>0.558</td>
<td>2.677</td>
<td>0.5186</td>
<td>0.5159</td>
</tr>
<tr>
<td>5</td>
<td>0.4831</td>
<td>0.558</td>
<td>2.664</td>
<td>0.5205</td>
<td>0.5169</td>
</tr>
<tr>
<td>6</td>
<td>0.4832</td>
<td>0.5579</td>
<td>2.666</td>
<td>0.5223</td>
<td>0.518</td>
</tr>
<tr>
<td>7</td>
<td>0.4837</td>
<td>0.5584</td>
<td>2.669</td>
<td>0.5239</td>
<td>0.5192</td>
</tr>
<tr>
<td>8</td>
<td>0.4837</td>
<td>0.5584</td>
<td>2.703</td>
<td>0.5254</td>
<td>0.5206</td>
</tr>
<tr>
<td>9</td>
<td>0.4845</td>
<td>0.559</td>
<td>2.658</td>
<td>0.5268</td>
<td>0.5223</td>
</tr>
<tr>
<td>10</td>
<td>0.4828</td>
<td>0.5575</td>
<td>2.664</td>
<td>0.5283</td>
<td>0.5242</td>
</tr>
</tbody>
</table>

From Table 3.7, it can be seen that DC injection values are not much influenced by variation in parasitic capacitance but is greatly affected by the topology. Referring to Table 3.7, a sudden increase of DC injection values in case of Bipolar, Unipolar and Hybrid against parasitic capacitance values 9μF and 8μF can be seen. This can be attributed to the establishment of resonant circuit including parasitic capacitance, filter inductors and grid impedance, due to galvanic connection between inverter and grid. This phenomenon is less pronounced in both topologies with DC bypass because
of the isolation provided by DC decoupling during zero states. This in turn ensures no reactive power exchange between filter inductor and DC link capacitor.

![DC Injection Chart]

**Figure 3.34 DC injection values for five topologies Vs Parasitic capacitance**

DC injection is maximum for hybrid topology as shown in Figure 3.34, and least for bipolar PWM. Compared to Unipolar topology, the topologies with DC bypass have lower DC injection values. Moreover the resonant effects are less pronounced in DC bypass topologies. Comparing the two DC bypass topologies, DC bypass 2 has lower DC injected values. Since the resonant effects are much less seen in DC bypass topologies, controllers for DC elimination can be effectively implemented in those topologies.

The effect of line inductor imbalances on the common mode voltage is obvious from the equivalent circuit and Equation (3.13) for \( V_{ry} \). There are two cases in which the effect is studied, one when line inductor is placed entirely in phase branch and the other when the line inductors are equally distributed between line and neutral branches.
The differential mode current always flows through total line inductors \(L_R\) and \(L_Y\). Therefore the positioning of line inductors does not affect the differential mode current. But common mode current flows through phase and neutral lines equally. Hence the positioning of line inductors will affect the common mode current.

Until now, the effect of line inductor imbalances on DC injection has not been investigated. In this section the dependence of DC injection on line inductors and hence on the common mode voltage is established. Moreover, the DC injection of each of the five topologies is investigated on the basis of line inductor imbalances.

Table 3.8 DC Injection values for inductor imbalances

<table>
<thead>
<tr>
<th></th>
<th>Bipolar</th>
<th>Unipolar</th>
<th>Hybrid</th>
<th>DC Bypass 1</th>
<th>DC Bypass 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>(L_Y=L_R)</td>
<td>0.48317</td>
<td>0.55801</td>
<td>2.6694</td>
<td>0.51791</td>
<td>0.52136</td>
</tr>
<tr>
<td>(L_Y=0)</td>
<td>0.6475</td>
<td>0.8433</td>
<td>4.122</td>
<td>7.995</td>
<td>7.806</td>
</tr>
</tbody>
</table>

Figure 3.35 DC injection values of five topologies for inductor imbalances
Table 3.9, shows the values of DC injection produced by 5 topologies. When the neutral inductor is absent, the value of DC injection increases. In the DC bypass topologies, the injected DC value is less when line inductors are balanced, but under imbalance, these topologies produce the highest DC injection as shown in Figure 3.35. This can be understood if the effective common mode voltages of these topologies are studied closely.

Table 3.9  Comparison of DC injection values for Hybrid and DC bypass topologies when \( L_Y = 0 \)

<table>
<thead>
<tr>
<th>Hybrid</th>
<th>( V_{CM,\text{EFF}} ) for ( L_Y=0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1,S4 ON</td>
<td>0</td>
</tr>
<tr>
<td>S2,S3 ON</td>
<td>( V_{DC} )</td>
</tr>
<tr>
<td>S1,S3,D3 ON</td>
<td>( V_{DC} )</td>
</tr>
<tr>
<td>S2,S4, D4 ON</td>
<td>0</td>
</tr>
<tr>
<td><strong>DC Bypass 1</strong></td>
<td></td>
</tr>
<tr>
<td>S5,S4,S1 ON</td>
<td>0</td>
</tr>
<tr>
<td>S5,S2,S3 ON</td>
<td>( V_{DC} )</td>
</tr>
<tr>
<td>S1 ON</td>
<td>( V_{DC}/2 )</td>
</tr>
<tr>
<td>S3 ON</td>
<td>( V_{DC}/2 )</td>
</tr>
<tr>
<td><strong>DC Bypass 2</strong></td>
<td></td>
</tr>
<tr>
<td>S5,S6,S1,S4 ON</td>
<td>0</td>
</tr>
<tr>
<td>S5,S6,S2,S3 ON</td>
<td>( V_{DC}/2 )</td>
</tr>
<tr>
<td>S1 ON</td>
<td>0</td>
</tr>
<tr>
<td>S3 ON</td>
<td>( V_{DC}/2 )</td>
</tr>
</tbody>
</table>

The comparison of effective common voltage between hybrid and DC Bypass topologies is shown in Table 3.9. Once the decoupling switch S5 opens, voltage of the high side of H-Bridge is floating. This voltage would decrease due to parasitic capacitance, but it is clamped \( V_{DC}/2 \) by the clamping diodes. So the effective common mode voltage fluctuation is more in DC
bypass topologies compared to hybrid when $L_Y = 0$. This causes the DC injection value to increase in DC bypass topologies when $L_Y = 0$.

Series capacitance in the output of the inverter can reduce the DC injection as capacitance is the basic element that blocks DC. This is obvious in the operation of half bridge inverters as it can be considered as an effective topology that inherently blocks DC. Poor voltage utilization and increased input voltage requirement limit the popularity of half bridge structures.

Table 3.10  Comparison of DC injection values for $L_Y = 0$, $L_Y=L_R$ and Series Capacitance

<table>
<thead>
<tr>
<th></th>
<th>Bipolar</th>
<th>Unipolar</th>
<th>Hybrid</th>
<th>DC Bypass 1</th>
<th>DC Bypass 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_Y=L_R$</td>
<td>0.48317</td>
<td>0.55801</td>
<td>2.6694</td>
<td>0.51791</td>
<td>0.52136</td>
</tr>
<tr>
<td>$L_Y=0$</td>
<td>0.6475</td>
<td>0.8433</td>
<td>4.122</td>
<td>7.995</td>
<td>7.806</td>
</tr>
<tr>
<td>$L_Y=L_R$ and with series Capacitance</td>
<td>0.09162</td>
<td>0.1074</td>
<td>0.5588</td>
<td>0.1045</td>
<td>0.09293</td>
</tr>
</tbody>
</table>

Figure 3.36  DC Injection Values for $L_Y = 0$, $L_Y=L_R$ and Series Capacitance
When series capacitance is added to the different topologies, as seen in Figure 3.36, the DC injection values have considerably dropped. In conclusion it can be said that DC injection values does not much depend on the value of parasitic capacitance. The value of injected DC definitely depends on the effective common mode voltage which can be adjusted by the balance of output inductors. From Table 3.10 it is obvious that DC injection values have considerably reduced from previous two cases. Also, bipolar PWM has the lowest DC injection values with series capacitance as well. The highest values are for hybrid PWM. DC bypass topologies have lower values than Unipolar PWM.

3.5 SUMMARY

Table 3.11 Comparison of Topologies.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Parameters</th>
<th>Effective Common Mode Voltage $V_{CM_{EFF}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Leakage Current</td>
<td>DC Injection $V_{DC}/2$</td>
</tr>
<tr>
<td>H-Bridge with Bipolar PWM</td>
<td>Low</td>
<td>Lowest</td>
</tr>
<tr>
<td>H-Bridge with Unipolar PWM</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>H-Bridge with Hybrid PWM</td>
<td>Highest</td>
<td>Highest</td>
</tr>
<tr>
<td>H-Bridge with DC Bypass (one Switch)</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>H-Bridge with DC Bypass (two Switches)</td>
<td>Lowest</td>
<td>Low</td>
</tr>
</tbody>
</table>

The effect of filter inductor imbalances have been investigated in all five topologies including DC bypass topologies. It has been observed that DC bypass topologies maintain the common mode voltage constant in all the
modes of operation with balanced filter inductors. Therefore the DC bypass topologies are excellent options for transformerless inverter structures. Bipolar PWM also gives constant common mode voltage, but, the quality of power and efficiency is lower to DC bypass topologies.

The analysis of harmonic spectrum of leakage current reveals that values of parasitic capacitance affect its frequency distribution. The H-bridge structure with bipolar, unipolar and hybrid PWM give higher order harmonics with small values of parasitic capacitance. Lower order harmonics are more pronounced with larger values of parasitic capacitance. Hence the filtering requirements are more with higher values of parasitic capacitance. Hence the filtering requirements are more with higher values of parasitic capacitance. For DC bypass 1 topology, higher order harmonics are present in leakage current irrespective of parasitic capacitance values and so filtering requirements are lower. DC bypass 2 follows the H-bridge philosophy, having higher order harmonics with smaller values of parasitic capacitance and lower order harmonics with larger values of parasitic capacitance. So the filtering requirements are similar to H-bridge structures.

In conclusion it can be said that DC injection values does not much depend on the value of parasitic capacitance. The value of injected DC definitely depends on the effective common mode voltage which can be adjusted by the balance of output inductors.

It can be concluded from Table 3.11 that, Bipolar PWM and DC bypass 1 topologies have low values for DC injection and leakage current. The lowest value for both leakage current and DC injection is exhibited by DC bypass 2 topology. Unipolar and Hybrid topologies are not well suited for transformerless topologies without adequate control devices. The summary of the analysis regarding leakage current and DC injection is shown in Table 3.11.