ABSTRACT

The work presented in the thesis evolves around the following ideas:

1. Development of a small signal MOSFET model considering second order effects and valid for all levels of inversion (strong, moderate and weak).

2. Comparison of performance of single transistor amplifier configuration for different inversion levels and determination of optimum inversion level for maximum gain for a given $f_t$.

3. Development of design guidelines for a 2-stage CMOS operational amplifier to meet certain specifications without any design iterations and valid for all levels of inversion.

4. Study of mismatch errors for the standard current mirror configurations at all inversion levels.

5. Development of scaling rule for MOSFET with reduction in power consumption and its application to an operational amplifier design.

The thesis has been organized in 7 chapters, contents of which are briefly given below.

(i) Chapter-1 introduces the rationale of investigating low-power CMOS analog design at different inversion levels. Motivation and need of development study of the analog blocks viz MOS amplifier, operational amplifier and current mirror are justified.
(ii) Chapter-2 describes the development of the small signal MOSFET model considering second order effects. The second order effects such as CLM, DIBL, velocity saturation are represented as different components of the drain, gate and source transconductances and are compared at different inversion levels.

(iii) In Chapter-3, the single stage amplifier design is optimized for maximum gain Bandwidth. The common source amplifier is found to give maximum gain at a given $f_t$ when operation at an optimum inversion level of 90.

(iv) Chapter-4 gives the details of 2-stage CMOS operational amplifier design. Analytical expressions using the Advanced Compact Mosfet (ACM) Model valid for all inversion levels are derived for all the parameters of the operational amplifier and design guidelines were developed for meeting given specifications of operational amplifier.

(v) Chapter-5 deals with the analysis of the DC matching errors in current mirrors at different inversion levels and its impact on the design.

(vi) The optimum scaling for reduction in power consumption is described in Chapter-6. The scaling laws are applied to single stage amplifier and operational amplifier using the ACM model.

(vii) Finally, conclusions and future scope of work is summarized in Chapter-7.