CHAPTER-5

ANALYSIS OF MATCHING ERRORS IN CURRENT MIRRORS AT DIFFERENT INVERSION LEVELS

5.0 INTRODUCTION

A very useful block in both nMOS and CMOS analogue circuit design is the current mirror[30,31]. As well as performing identity operations and current amplification [32,33], the current mirror is also used both as a biasing element and as a load device for amplifier stages [30,31]. The current comparator[34], current Schmitt trigger [35] and current A/D and D/A converters are additional examples of circuits or devices that benefit from the use of current mirrors [36,37,38]. The initial circuits were realized using bipolar transistors and rigorous analysis of bipolar current mirrors had been carried out, from their output resistance and DC matching errors to their noise[30,39,40,41]. In the past decade, as the maturity of analogue MOS amplifier technology has progressed, a series of high-performance current mirrors in MOS technology has been developed to meet different requirements[42,43,44]. In the characterization of these current mirrors, an ideal current ratio is usually assumed, thus greatly simplifying the design of current mirrors.[30,31]. But the performance of most analog circuits is limited by non-idealities of current mirror. In the design of precision analogue circuits, such as high resolution current A/D and D/A converters, the DC matching errors will be more important than mismatches in MOS transistors because they represent a systematic error, whereas mismatches in MOS devices give random errors [45,46,47]. However, there had been no rigorous analysis in the literature of the relative merits of the different mirrors in terms of their
design parameters. In [48] analytical determination of output resistance and current ratio or DC matching errors in MOS current mirrors was presented but the results were in terms of mismatch between the input and output voltage of the mirror and limited to the strong inversion region of operation of MOS transistor. Further, design parameters of current mirror transistors for reduced matching error was not considered. For example, a simple current mirror is often replaced with a Wilson current mirror so as to achieve a much higher output resistance [31], without regard for the transistor design parameters, which suffers from asymmetrical biasing. To overcome the problem, another transistor is simply added to the circuit and the resulting new circuit is thus named the improved Wilson current mirror [31], without consideration of what quantitative improvement is really achieved.

The design of current mirror involves different conflicting design specifications (noise, bandwidth, input and output resistances, power dissipation, accuracy, THD, etc) while only three design transistor parameters are available (DC current, width, length). The single equation ACM model derived in [10] for MOS transistor was recently used [49] to study the design tradeoffs for a simple current mirror. In the present work, the analysis (DC matching error, output impedance) of the simple current mirror, the Wilson current mirror and the improved Wilson current mirror are considered. The analysis is performed using the ACM model, resulting in expressions in terms of the Inversion Coefficients (IC) of the transistors (eq 1.4) that are valid in all regions (weak, moderate and strong inversion) of operation. A theoretical formula, accounting for parameter mismatch errors, and simulation results establish that the use of minimum length and width transistors can result in larger current mismatch in Wilson current mirror. This indicates a tradeoff between area and current error for the current mirror.
5.1 ANALYSIS OF SIMPLE CURRENT MIRROR.

For the simple current mirror in Fig 5.1 we derive the following parameters that are valid for all inversion levels.

\[ J_{in} \rightarrow \quad J_{out} \]

\[ M_1 \quad W/L \]

\[ M_2 \quad W/L \]

Fig 5.1: Simple Current Mirror (1:1)

5.1.1 Output resistance

Output resistance is one of the most important performance parameters for a current mirror. The simple current mirror consists of only two nMOS transistors. Since enhancement-mode MOS transistors remain in the saturation mode of operation when the gate is shorted to the drain and the gate-to-source voltage exceeds the threshold voltage, both devices will remain in the saturated mode when the output \( V_{out} \) at the output node is larger than the value \( V_{out\,(min)} = V_{in} - V_t \).

The output conductance of the circuit is \( g_o = g_{db2} \) and the output resistance is

\[ r_o = \frac{1}{g_{db2}} = \frac{V_A L}{I_d} \]

where \( V_A \) is the Early Voltage in V/\( \mu \)m.
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![Diagram of simple current mirror](image)

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$$r_o = \frac{1}{g_{ds2}} = \frac{V_A}{I_d}$$

where $V_A$ is the Early Voltage in $V/\mu m$.
5.1.1 Input Resistance ($R_{in}$)

The expression for terminal voltages of the MOSFET in saturation in terms of the inversion coefficient is derived in [10] as

$$\frac{V_p - V_S}{\phi_t} = \left[ \sqrt{1 + IC} - 2 + \ln(\sqrt{1 + IC} - 1) \right] \text{ for nMOS}$$

$$= \left( \left( \sqrt{1 + IC} - 1 \right) - 1 + \ln(\sqrt{1 + IC} - 1) \right) \quad (5.1)$$

$$\frac{V_{Dsat} - V_p}{\phi_t} = \left[ \ln(\sqrt{1 + IC} - 1) - 5 \right] \text{ for nMOS} \quad (5.2)$$

The input resistance is

$$R_{in} = \frac{\partial V_{in}}{\partial I_{in}}$$

$$= \frac{n \phi_t}{I_s} \left[ \frac{1}{2 \sqrt{1 + IC}} + \frac{1}{\sqrt{1 + IC} - 1} - \frac{1}{2 \sqrt{1 + IC}} \right]$$

$$= \frac{n \phi_t}{I_s} \frac{1}{2 \sqrt{1 + IC} - 1} \quad (5.3)$$

5.1.1 DC matching errors.

The conventional current mirror is frequently used for identity operations where the ratio of output current to input current is unity. Any departure of the current ratio from unity will directly cause accuracy errors in the circuit, especially in current A/D and D/A converters [36,37,47], current comparators and current Schmitt triggers [34,35,50]. A basic parameter of the current mirror is the direct current transfer ratio, which in precision designs, is required to have a value of unity with as small a tolerance as possible. The ACM [10] model facilitates the development of a practically useful formula, for estimating the nominal value of and the tolerance limits on it, arising from mismatches.
in operating conditions and dc parameters of the MOS transistors used, at
different inversion levels.

(a) Current offset due to $V_p$ mismatch

Let $V_p$ mismatch (ie $V_T$ mismatch for fixed gate voltage) result in a
change in the term

$$(\sqrt{1+IC} - 1) \rightarrow \alpha(\sqrt{1+IC} - 1)$$

Considering $\alpha(\sqrt{1+IC} - 1) \equiv I_{out}$ and $(\sqrt{1+IC} - 1) \equiv I_{in}$

Hence $\alpha = \frac{I_{out}}{I_{in}}$ is the current ratio.

Using equation (5.1) we obtain

$$\frac{\Delta V_T}{n} = \phi_t((\sqrt{1+IC} - 1) - 1 + \ln(\sqrt{1+IC} - 1)) - \alpha(\sqrt{1+IC} - 1) + 1 - \alpha \ln(\sqrt{1+IC} - 1)$$

$$= \phi_t((1 - \alpha)(\sqrt{1+IC} - 1) + \ln(1/\alpha))$$

where $\Delta V_T$ is the mismatch in threshold voltage between matched transistors
M1 and M2

For large current ratios, neglecting $(1/\alpha)$ we get

$$\frac{\Delta V_T}{n} = \phi_t((1 - \alpha)(\sqrt{1+IC} - 1)) \quad (5.3)$$

Also

$$\alpha - 1 = \frac{I_{out} - I_{in}}{I_{in}} = \frac{\Delta I}{I} = -\frac{\Delta V_T}{n\phi_t} \frac{\sqrt{1+IC} - 1}{IC}$$
The DC matching error ($\varepsilon$) is defined as the difference between current ratio ($\alpha$) and unity, or

$$\varepsilon = \alpha - 1 = -\frac{\Delta V_T}{n\phi_t} \frac{\sqrt{1 + IC} + 1}{IC}$$

(5.4)

The error due to mismatch of threshold voltages for the matched transistors is higher at low inversion levels of transistor and reduces considerably as the transistors move to strong inversion,

(b) Current error due to finite output resistance.

Let $R_{in1}$ and $R_{in2}$ be the input impedance of the current mirror and that of the second current mirror connected in cascade, respectively.

Consider

$$\frac{I_{in}}{R_{in1}} = \frac{1}{\alpha}$$

and

$$\frac{I_{out}}{R_{out} || R_{in2}} = \frac{1}{\alpha}$$

(5.5)

but $R_{in1} = R_{in2}$ for identical current mirrors in cascade.

Hence

$$\frac{I_{in} - I_{out}}{I_{in}} = 1 - \frac{I_{out}}{I_{in}} = 1 - \frac{R_{in2}}{R_{out} || R_{in2}} = 1 - \frac{R_{out} + R_{in2}}{R_{out} || R_{in2}} = \frac{R_{in2}}{R_{out}}$$

$$= \frac{n\phi_t}{2} \frac{1}{\sqrt{1 + IC} - 1} \frac{1}{\sqrt{1 + IC} + 1} = \frac{n\phi_t}{2} \frac{IC}{2LV_A} \sqrt{1 + IC} - 1$$

(5.6)

Error can be reduced by increasing length but this reduces BW and increases area. Fig 5.2 shows the plot for the current gain error for the simple current mirror at different inversion levels.
Fig 5.2: Plot of current gain errors in simple current mirror as a function of transistor inversion level.
5.2 ANALYSIS OF WILSON CURRENT MIRROR

Fig 5.3 shows a standard Wilson current mirror, comprising closely matched MOS transistors M1, M2 and M3 driven by an input current $I_{in}$ and producing an output current $I_{out}$ which differs from $I_{in}$ due to the asymmetrical biasing.

The current ratio is given as

$$\alpha = \frac{I_{out}}{I_{in}} = 1 + \frac{(\Delta I)'}{I} + \frac{(\Delta I)''}{I} + \frac{(\Delta I)'''}{I}$$  \hspace{1cm} (5.7)

In eq(5.7), the drain current differential $(\Delta I)'$, caused by asymmetrical biasing of M1 and M2 due to differences in the matched transistors parameters, when they are operated at the same drain voltage, can be conveniently expressed in terms of a pinch-off offset voltage as applied to a simple current mirror above and in [49].

$$\left(\Delta I\right)' = -\frac{V_p}{n\phi_t} \left(\sqrt{1 + IC + 1}\right)$$ \hspace{1cm} (5.8)

$(\Delta I)'$ is the current differential that results due to the finite and asymmetrical output resistances seen at the drain of M1 and M2.

Hence

$$\left(\Delta I\right)' = \frac{n\phi_t}{2LV_{ds}} \frac{IC}{\sqrt{1 + IC - 1}}$$ \hspace{1cm} (5.9)

$(\Delta I)'$ is the current differential that results due mismatch in $S=W/L$ ratio of transistors M1 and M2, where W and L are respectively the width and length of the transistors. Since $W/L$ is directly proportional to the drain current, assuming the gate biasing of the two transistors equal, $(\Delta I)'$ can be represented as

$$(\Delta I)' = I \frac{\Delta S}{S}$$
Both \( (\Delta I)' \) and \( (\Delta I)'' \) are functions of inversion coefficient \((IC)\): the first term decreases while the second term increases with an increase in \( IC \).

Hence

\[
\alpha = 1 - \frac{n \phi_t}{2 L V_A} (\sqrt{1 + IC} + 1) \pm \frac{\Delta V_p}{n \phi_t} \frac{1}{\sqrt{1 + IC} - 1} \pm \frac{\Delta S}{S} \quad (5.10)
\]

The nominal value for \( \alpha \) is less than unity by an amount \( \frac{n \phi_t}{2 L V_A} (\sqrt{1 + IC} + 1) \), which might well approach the magnitude of the tolerance on \( \alpha \) resulting from \( S \) and \( V_p \) mismatches. Thus if

\[
L = 2 \mu m, \quad V_A = 5V / \mu m, \quad IC = 100, \quad \frac{\Delta S}{S} = 0.01 \quad \Delta V_p = 0.25mV \quad \text{then}
\]

\[
\alpha = 0.9856 \pm 0.01106
\]

The nominal value for \( \alpha \) can be made to approach unity by increasing the channel length of the transistors and simultaneously the width thus maintaining a constant inversion coefficient but increasing the area occupied by the transistors. Increasing only \( L \) will increase the inversion coefficient and hence the nominal value of \( \alpha \). Increasing only widths of the transistors result in lowering the inversion coefficient and hence decreasing the nominal error but increasing the effect of mismatch due to \( V_p \).

The nominal value can be made to approach unity more closely by the addition of the diode-strapped matched transistor \( M4 \) in fig5.4. This ensures that the output resistances at the drain of \( M1 \) and \( M2 \) are matched, eliminating the term \( (\Delta I)'' \). This 4 transistor current mirror is called the improved Wilson current mirror.
Fig 5.3  Wilson Current Mirror

Fig 5.4  Improved Wilson Current Mirror

<table>
<thead>
<tr>
<th>Circuit No.</th>
<th>$I_{in}$</th>
<th>$I_{out}$</th>
<th>$W$</th>
<th>$L$</th>
<th>IC</th>
<th>$\alpha$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.36468e-5</td>
<td>1.3437e-5</td>
<td>10 $\mu m$</td>
<td>2 $\mu m$</td>
<td>79</td>
<td>0.98</td>
</tr>
<tr>
<td>2</td>
<td>1.35675e-5</td>
<td>1.3496e-5</td>
<td>20 $\mu m$</td>
<td>2 $\mu m$</td>
<td>79</td>
<td>0.9947</td>
</tr>
<tr>
<td>3</td>
<td>1.45049e-5</td>
<td>1.4318e-5</td>
<td>20 $\mu m$</td>
<td>2 $\mu m$</td>
<td>42</td>
<td>0.987</td>
</tr>
<tr>
<td>4</td>
<td>9.57242e-6</td>
<td>9.3629e-6</td>
<td>2 $\mu m$</td>
<td>2 $\mu m$</td>
<td>280</td>
<td>0.978</td>
</tr>
</tbody>
</table>

Table 1. Simulation results for the Wilson Current Mirror in Fig 5.3. All the transistors have the same L and W values
The error in the nominal value of $\alpha$ if $M4$ is omitted has been previously quantified for monolithic bipolar transistor Wilson current mirror by Hart and Baker [40]. We have quantified the error for the MOS version of the Wilson current mirror and the formula derived is valid for all levels of inversion (weak, moderate and strong) of the MOS transistors.

5.3 RESULTS AND CONCLUSION:

Simulation results for determination of the nominal value of neglecting the $Vp$ and $S$ mismatch is given in Table 5.1. The current ratio is obtained as 0.98 at sr no 1. Increasing $L$ and $W$ while maintaining $IC$ (inversion coefficient) constant gives an improvement in the current ratio and hence a decrease in the nominal error value. Comparing the result at sr. no, 3 with that at sr. no. 1 indicates an improvement in current ratio with reducing $IC$ and constant $L$. The result at sr. no 4 compared to that at sr. no 1 indicates an increase in the current error for increase in IC. A technique for the design of current mirror with reduced current error is thus presented.