LIST OF FIGURES

Figure 2.1: The symbol of CCII 15
Figure 2.2: The CMOS structure of the MOCCII [16] 15
Figure 2.3: The versatile first order filter 16
Figure 2.4: Frequency response of low-pass and high-pass filter section 18
Figure 2.5: Frequency response of all-pass filter section 18
Figure 2.6: The multifunctional biquadratic filter 19
Figure 2.7: Simulated and experimental high-pass and band-pass filter responses 21
Figure 2.8: Simulated and experimental low-pass and band-reject filter responses 21
Figure 2.9: The MOCCII based CM-EPSO circuit 22
Figure 2.10: The phaser diagram of CM-EPSO 23
Figure 2.11: The wave-shapes of the designed CM-EPSO of Fig. 2.9 23
Figure 2.12: The wave-shapes of the designed VM-EPSO 24
Figure 2.13: The VM-FPSQO circuit using CMOS MOCCII 24
Figure 2.14: Output waveforms of VM-FPSQO 25
Figure 2.15: Frequency variation of VM-FPSQO with R3 26
Figure 2.16: CCII based bi-phase amplifier 26
Figure 2.17: The precision rectifier circuit 27
Figure 2.18: DC transfer characteristics of the precision rectifier 30
Figure 2.19: Input and output waveform at 10KHz 30
Figure 2.20: Input and output waveforms at 100KHz 30
Figure 2.21: Input and output waveforms at 1MHz 30

Figure 3.1: Schematic symbol of the DVCC 35
Figure 3.2: CMOS implementation of the DVCC with only Z+ output [59] 35
Figure 3.3: Block diagram of DVCC with its parasitic elements 37
Figure 3.4: FD first-order filter all-pass filter-I 37
Figure 3.5: Proposed first order FD all-pass filter-II 39
Figure 3.6: Frequency response of FD all pass filter-I of Fig. 3.4 42
Figure 3.7: Time domain response of FD filter-I of Fig. 3.4 43
Figure 3.8: Magnitude and phase response of the proposed first order filter-II of Fig. 3.5 43
Figure 3.9: Time-domain response of FD APF-II of Fig. 3.5 43
Figure 3.10: THD performance of the FD APF-II of Fig. 3.5 44
Figure 3.11: Results of hardware verification of first-order all-pass filter-II circuit of Fig. 3.5 44
Figure 3.12: Input and output differential signals of the second order APF-II of Fig. 3.5 44
Figure 3.13: Proposed second-order FD all-pass/notch filter section 45
Figure 3.14: Magnitude and phase responses of the proposed second-order FD APF 48
Figure 3.15: Gain and phase plots of the proposed second-order FD notch filter 48
Figure 3.16: Results of hardware verification of notch implemented using the circuit of Fig. 3.13 48
Figure 3.17: The MO-DVCC based VM-FPSO
Figure 3.18: Proposed four phase FD sinusoidal oscillator
Figure 3.19: The wave-shapes of FPSO of Fig. 3.17
Figure 3.20: Frequency response of FPSO with $R_2$
Figure 3.21: Four-phase waveforms of the proposed oscillator shown in Fig. 3.18
Figure 3.22: Precision rectifier-I using a DVCC-based bi-phase amplifier
Figure 3.23: Precision rectifier-II using a DVCC-based bi-phase amplifier
Figure 3.24: Input and output waveform of the precision rectifier-I at 10 KHz
Figure 3.25: Input and output waveform of the precision rectifier-I at 100 KHz
Figure 3.26: Input and output waveform of the precision rectifier-I at 1MHz
Figure 3.27: Input and output waveform of the precision rectifier-II at 1MHz

Figure 4.1: The symbol of DX-MOCCII
Figure 4.2: The CMOS structure of the DX-MOCCII [54]
Figure 4.3: The symbol of DD-DXCCII
Figure 4.4: CMOS implementation of DD-DXCCII [95]
Figure 4.5: The versatile first order filter section
Figure 4.6: Tunable first-order VM filter
Figure 4.7: Frequency response of low-pass and high-pass filter sections
Figure 4.8: Phase and gain plot of all-pass response of Fig. 4.5
Figure 4.9: Time domain response of the proposed all-pass filter section
Figure 4.10: THD variation of the all-pass section with signal amplitude at 1.59MHz
Figure 4.11: Realization of DXCCII using AD844
Figure 4.12: Comparison of theoretical and experimental results for HP, LP and AP responses
Figure 4.13: Experimental quadrature waveforms for AP filter section and X-Y of two voltage outputs
Figure 4.14: Phase and gain plot at different $V_C$
Figure 4.15: Input and output wave-shapes at 3MHz
Figure 4.16: THD variation of all-pass filter at 3MHz of Fig. 4.6
Figure 4.17: Second order current-and transresistance-mode filter
Figure 4.18: Simulated gain responses of CM multifunctional filter
Figure 4.19: Gain and phase plot of CM multifunctional filter
Figure 4.20: Simulated gain response of notch CM multifunctional filter
Figure 4.21: The input and output waveforms of the BP response for an 100 $\mu$A (peak-to-peak) sinusoidal input current at 1.57 MHz.
Figure 4.22: Band-pass and low-pass response in transresistance-mode
Figure 4.23: Tunable n$^{th}$ order all-pass filter
Figure 4.24: Gain and phase plot of tunable 3$^{rd}$ order all-pass filter
Figure 4.25: Phase plot of 1$^{st}$ and 3$^{rd}$ order all-pass filter
Figure 4.26: Group delay frequency response of the 1$^{st}$ and 3$^{rd}$ order all-pass filter
Figure 4.27. The DX-MOCCII based CM-FPSO circuit
Figure 4.28. Modified MO-DXCCII based CM-FPSO
Figure 4.29. Wave-shapes of the designed CM-FPSO
Figure 4.30. THD variation of the output of the CM-FPSO for different oscillation frequency
Figure 4.31. Frequency tuning of CM-FPSO with C
Figure 4.32. Wave-shapes of the designed VM-FPSO
Figure 4.33. Proposed CM and VM three phase oscillator
Figure 4.34. Simulated output waveshapes of the CM for the three phase oscillator
Figure 4.35. Simulated output waveshapes of the VM for the three phase oscillator
Figure 4.36. Frequency tuning of three phase oscillator with C
Figure 4.37. Proposed DXCCII based mixed-mode multiphase oscillator
Figure 4.38. Simulated three phase voltage outputs
Figure 4.39. Simulated three phase current outputs
Figure 4.40. Obtained frequency variation with capacitor values for the proposed circuit
Figure 4.41. THD for different frequencies of oscillation for $V_{\text{out-2}}$

Figure 5.1: Symbol of DPCCII with current gain N
Figure 5.2: The CMOS implementation of a 3-bit DCCCII with current gain N [144]
Figure 5.3: Symbol of DPCCII with current gain N$^{-1}$
Figure 5.4: The CMOS implementation of a 3-bit DPCCII with current gain N$^{-1}$[144]
Figure 5.5: Electrical symbol of CCCII
Figure 5.6: Current division network (CDN) [148]
Figure 5.7: CMOS realization of CDC [148]
Figure 5.8: Symbol of DCCDVC
Figure 5.9: CMOS implementation of DCCDVC
Figure 5.10: The digitally controlled current-mode first order multifunctional filter
Figure 5.11: CMOS implementation of a 3-bit DPCCII of Fig. 5.10
Figure 5.12: Frequency response of the digitally programmable LP and HP filters
Figure 5.13: Gain and phase response of the digitally programmable all-pass filter
Figure 5.14: Proposed digitally programmable biquadratic filter
Figure 5.15: Tuning of low-pass filter function with digital control word
Figure 5.16: Tuning of high-pass filter function with digital control word
Figure 5.17: Tuning of band-pass filter function with digital control word
Figure 5.18: Pole-Q variation with digital control word at 385KHz
Figure 5.19: Proposed digitally controlled biquadratic filter
Figure 5.20: Tuning of high-pass filter function with digital control word
Figure 5.21: Tuning of low-pass filter function with digital control word
Figure 5.22: Tuning of band-pass filter function with digital control word
Figure 5.23: Pole-Q variations with digital control word
Figure 5.24: High-pass variations in Trans-admittance mode
Figure 5.25: Low-pass variations in Trans-admittance mode
Figure 5.26: Band-pass variations in Trans-admittance mode
Figure 5.27: Band-pass output at 12MHz
Figure 5.28: Fourier spectrum of band-pass output at 12MHz
Figure 5.29: CMRR frequency response of low-pass filter
Figure 5.30: OTA equivalent of digitally controlled FD voltage- and transadmittance-mode
biquadratic filter [79]
Figure 5.31: Proposed digitally programmable mixed-mode quadrature oscillator
Figure 5.32: Quadrature voltage outputs
Figure 5.33: Quadrature current outputs
Figure 5.34: Obtained frequency spectrum for quadrature voltage outputs in the circuit of Fig. 5.31
Figure 5.35: Frequency control by the bias currents of the DPCCCIIs