CHAPTER 5

DIGITALLY PROGRAMMABLE MULTIFUNCTIONAL FILTERS

This chapter discusses the concept of digitally programmable multifunctional filters and oscillators using CCII and CCCII. A total of three filters and one oscillator have been proposed within this Chapter. The first two filters that operate at low voltages are first-order and second-order multifunctional type. The third filter is fully differential (FD) and operates in voltage- and transadmittance-mode simultaneously. Towards the end of the Chapter, a CCCII is used as a building block to design a digitally-controlled quadrature oscillator circuit.

5.1 Introduction

Recent trends indicate a rapidly increasing demand for programmable analog signal processing modules. Programmability significantly enhances the on-chip control of these modules as has been pointed out in [27, 79, 115-117]. Consequently, numerous other designs have been recently proposed that support this feature. Keeping with this trend, this Chapter proposes some programmable first-order and second-order filters as well as a programmable oscillator. The first-order and one of the realized second-order filters is a low-voltage CM multifunctional filter. Such low voltage analog circuits are in demand when designing portable systems [118, 119].

Biquadratic filters with voltage input and voltage and/or current outputs as well as those with current input and current and/or voltage outputs have often been termed as mixed-mode filters [120-132]. Mixed-mode filter circuits can be categorized either as single-input type or multiple-input type [120-125]. Among these, circuit designs presented in [120-123] can realize only one standard filter function in one mode at a time while the design in [124] realizes all-filter responses in two modes at a time. In contrast, the filter presented in [125] is capable of providing all-pass responses in both inverting and non-inverting mode. It also produces VM and CM outputs with a differential stage input. In some applications however, simultaneous outputs may be required with a single input. Literature survey has shown that comparatively little work has been done in the domain of single-input-type mixed-mode filters in contrast to multiple-input type mixed-mode filters. However, some notable designs which operate in all modes can be found in [126-130, 132]. These filters are single-input-type mixed-mode filters using different active elements such as (CFOAs) [130], CCCII [132], FDCCIIs [126] and current-controlled current conveyor trans-conductance amplifiers (CCCCTAs) [128]. They provide all output
functions in different modes. However, all of these circuits exhibit low input impedance except for those
designed in [128, 129]. Study of mixed-mode filters with a single-input reveal a lack of circuits that
realize FD inverting and non-inverting low-pass, high-pass and band-pass filter functions in voltage and
transadmittance mode and offering high input impedance terminals.

At present, there is a growing interest in designing FD analog filters [62, 65, 70, 79, 133]. FD
filters play a very important role in communication systems. For example, many instrumentation signals
are differential in nature. They are processed under a filtering action before going to the differential
amplifier stage. If single-ended filters are used then noise is also propagated along with the required
signal which can lead to a severe reduction in the CMRR. On the other hand, FD filters increase the
signal-to-noise ratio. These filters exhibit a larger dynamic range, better rejection to power-supply noise
and reduced harmonic distortion when compared to single-ended input/output where unintended noise
and signals may be processed along with the desired signal.

Purely from a design perspective, the circuit proposed in [133] includes three FDCCIIs, six
resistors and four capacitors. It generates only VM low-pass and band-pass responses. The circuit
described in [65] shows a VM FD filter which provides high-pass, band-pass and low-pass outputs
simultaneously and contains five OTAs and three capacitors. The circuit presented in [70] has three
OTAs, six capacitors and is capable of FD CM low-pass output. The FD VM filter in [62] employed
three DO-DDCCs, two capacitors and five resistors. This filter generates high-pass, band-pass and low-
pass outputs. The circuit of [79] employs five digitally-controlled CMOS fully-balanced output
transconductor (DCBOTA), one resistor, two capacitors and offers digitally-controlled FD VM high-
pass, band-pass and low-pass responses simultaneously.

It is to be noted that most of the previous work is concerned with the design of FD filters that
operate either in VM or CM. In contrast, one of the proposed second-order filters (different from the one
described above) is a voltage- and transadmittance-mode FD filter with a digital control facility. The
filter so designed provides FD voltage- and transadmittance mode low-pass, high-pass and band-pass
responses simultaneously either in inverting or non-inverting form.

Looking at the design of oscillators, literature is replete with both VM and CM quadrature
oscillators [108, 134-141]. Some of them provide VM outputs while others generate CM signals.
However, not much work has been reported on mixed-mode quadrature oscillators. The quadrature
oscillator in [136] uses three resistors and two capacitors with an FDCCI to provide two VM and two
CM outputs in phase quadrature. Although the quadrature oscillator of [136] uses only a single active
element and exhibits non-interactive frequency control, it lacks electronic tunability. The quadrature
oscillator of [137] uses two CCCIIIs and two grounded capacitors to generate quadrature CM and phase-
shifted voltage outputs. Electronic control of the frequency of oscillation as well as orthogonal control of frequency is also possible. However, current outputs are not suitable for driving high impedance loads. To generate load-insensitive CM outputs, additional output stages may be required, as employed in the proposed design. The circuit of [134] provides two quadrature current outputs and two phase-shifted voltage outputs using one plus-type and two minus-type CCCIs. The use of a floating capacitor in [134] adds to the circuit’s IC fabrication complexity. The circuit in [108] provides four-quadrature current outputs at high impedance and can be electronically tuned. It employs only grounded capacitors, but is categorized as a third-order oscillator. The oscillator circuit of [18] which generates multiphase current outputs at high impedance is electronically tunable and uses grounded capacitors. However, the circuit employs one translinear conveyor and three capacitors for each output of the n-phase oscillator. The circuits of [138, 141] are able to provide sinusoidal oscillations of up to the KHz range; though the component count for the circuits compares unfavorably with the proposed circuit. The oscillator of [140] is able to provide only VM quadrature outputs. The circuit of [139], although being easier to design and implement, is able to generate only CM outputs. Additional buffers would be required if VM outputs are desired.

CM oscillators with high-output impedance are of great interest because, apart from incorporating the well-known advantages of CM processing, they make it easy to drive loads without using a buffering device [137]. However, the recent circuit design trend is towards mixed-mode circuits that provide/use both VM and CM signals on the same chip. This added versatility in analog signal processing applications has led to the development of quadrature oscillator circuits that can provide both VM and CM outputs simultaneously. For such circuits, the current-controlled conveyor has emerged as the active device of choice as these translinear conveyors may be employed for realizing oscillators exhibiting electronic tunability and resistor-less realizations. Other features of interest for such circuits are orthogonal control of the condition of oscillation and frequency of oscillation, low component count and the use of grounded passive components from the point of view of contemporary integrated circuit implementation. Further, majority of the controllable current conveyors offer electronic control by an externally supplied bias current. However, digital control is a desirable feature in hybrid systems containing both analog and digital systems on the same chip.

The following section explains the technique reported in [142] to provide digital control (programmability) within CMOS implementations of CCII and goes on to propose a new technique to achieve programmability within a CMOS implementation of CCCII.
5.2 Digitally Programmable CCII

The digitally programmable CCII (DPCCII) [142] with gain $N$ is shown in Fig. 5.1 and its CMOS implementation is shown in Fig. 5.2.

![Digital control word](image)

**Figure 5.1. Symbol of DPCCII with current gain N**

![CMOS implementation](image)

**Figure 5.2. The CMOS implementation of a 3-bit DCCCII with current gain N [142]**

The idea behind the design of the proposed DPCCII is to control the current transfer gain parameter $N$. This is achieved by replacing the Z-terminal transistors of the CCII presented in Chapter 2 with transistor arrays associated with switches (PMOS M6A-M8A and NMOS M16A-M18A in Fig. 5.2). The gain parameter $N$ can take values from 1 to $(2^n - 1)$, where $n$ represents the number of transistor
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arrays. The concept of using transistor arrays to control the transconductance of basic transistors in a digitally-controlled balanced-output transconductor was introduced in [143]. This idea has been improved upon to implement a current summing network (CSN) at the Z-terminal as outlined in [142]. The CSN consists of n transistor pairs, whose N-MOS aspect ratios are given by:

\[ \left( \frac{W}{L} \right)_{N_i} = 2^i \left( \frac{W}{L} \right)_{15} \quad i = \{0,1, ..., n - 1\} \]  

(5.1)

Similarly, for the P-MOS array, the aspect ratios are:

\[ \left( \frac{W}{L} \right)_{P_i} = 2^i \left( \frac{W}{L} \right)_{5} \quad i = \{0,1, ..., n - 1\} \]  

(5.2)

Consequently, the current at the Z-terminal, if flowing out of the DPCCII block, can be expressed by:

\[ I_Z = \sum_{i=0}^{n-1} a_i 2^i (I_{M5} - I_{M15}) \]  

(5.3)

Therefore, the proposed DPCCII provides a current transfer gain equal to:

\[ N = \frac{I_Z}{I_X} = \sum_{i=0}^{n-1} a_i 2^i \]  

(5.4)

Parameter \( a_i \) represents the digital code-bit applied to the \( i^{th} \) branch in the CSN and is responsible for enabling and disabling the current flowing in that particular branch.

The symbol of a digitally-controlled CCII with current gain \( N^{-1} \) is shown in Fig. 5.3 and its CMOS implementation is shown in Fig. 5.4 [142]. The design idea presented previously can again be employed to implement a DPCCII with a current gain of less than unity. However, the transistor arrays are placed on the X-terminal and the CSN is moved to the input side. The Z-terminal gets only a replica of the smallest current in the array.

Figure 5.3. Symbol of DPCCII with current gain \( N^{-1} \)
Figure 5.4. The CMOS implementation of a 3-bit DPCCII with current gain $N^{-1}$ [142]

As previously discussed, the CSN consists of $n$ transistor pairs with the same aspect ratios as described in equations (5.1) and (5.2). The current at the X-terminal, flowing out the DPCCII block, is therefore given by:

$$I_X = \sum_{i=0}^{n-1} a_i 2^i (I_{M5} - I_{M15})$$

(5.5)

As a consequence, the DPCCII provides a current transfer gain equal to:

$$\frac{I_Z}{I_X} = \frac{1}{\sum_{i=0}^{n-1} a_i 2^i}$$

(5.6)

Here, parameter $a_i$ is responsible for enabling or disabling the current flow in the $i^{th}$ branch of the CSN.

The current fed to the X-terminal is always $N$ times greater than the current received at the Z-terminal.

The transfer matrix of DPCCII with current gain $N$ and current gain $N^{-1}$ can be expressed as:

$$
\begin{bmatrix}
I_Y \\
V_Y \\
I_Z \\
V_Z
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & |V_Y| \\
1 & 0 & 0 & |I_X| \\
0 & \pm N^m & 0 & |V_Z|
\end{bmatrix}
$$

(5.7)
where, $N$ is an $n$-bit digital control word ($N = \sum_{i=0}^{n-1} a_i 2^i$), the plus sign corresponds to $I_{Z+}$, and the minus sign to $I_{Z-}$. The power integer is $m = 1$ when the current gain is $N$, and $m = -1$ when the current gain is $N^{-1}$.

### 5.3 Digitally Current-Controlled Differential Voltage Conveyor (DCCDVC)

A current controlled conveyor (CCCII), [144] shown in Fig. 5.5, is characterized by the following port relationships:

$$i_Y = 0; V_Z = V_Y + I_X R_X, \text{and } i_Z = p I_X$$

(5.8)

![Figure 5.5. Electrical Symbol of CCCII](image)

In the above equation, $p = +1$ for a positive current-controlled conveyor and $p = -1$ for a negative current-controlled conveyor. A multi-output current controlled conveyor has several outputs of $Z+$ and $Z-$ type. The resistance $R_X$ appearing in equation (5.8) is the intrinsic $X$-terminal resistance of the CCCII [145]. It is related to the bias current of the CCCII as:

$$R_X = \frac{1}{g_{m19} + g_{m20}}$$

(5.9)

Where  $g_m = \sqrt{2\beta I_B}, \quad \beta = \mu C_{OX}(W/L)$

(5.10)

In equation (5.10) $\mu, C_{OX}, W$ and $L$ are the surface mobility, oxide capacitance, channel width and length of MOS transistors respectively and where $g_{m19}$ and $g_{m20}$ are the transconductances of $M_{19}$ and $M_{20}$ respectively in Fig. 5.9. Thus $R_X$ is controlled via $I_B$ if CMOS CCCIIIs are used. Since $g_{m19} = g_{m20} = g_m$, equation (5.9) becomes:

$$R_X \approx \frac{1}{\sqrt{8\mu C_{OX}(W/L)I_B}}$$

(5.11)

As can be seen from (5.11), the resistance $R_X$ can be adjusted by using a supplied bias current $I_B$. The DCCDVC is similar to the CCCII [146] except that the intrinsic resistance ($R_X$) is digitally controlled by varying the bias current with the help of a digital control word and its input stage ($Y$- port) is modified.
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to be similar to that of the DVCC[147]. In DCCDVC, the bias current is controlled by incorporating a
current division network (CDN)[148] which consists of \( n \) current division cells (CDCs) shown in Fig. 5.6.

![Figure 5.6. Current division network (CDN) [148]](image)

The CDC is a three-terminal network shown in Fig. 5.7. The output currents \( I_{\text{out,1}} \) and \( I_{\text{out,2}} \) can be varied
as fractions of the Input current \( I_B \) and are represented by the following relationships.

\[
I_{\text{out,1}} = \alpha I_B \quad (5.12)
\]

\[
I_{\text{out,2}} = (1 - \alpha) I_B \quad (5.13)
\]

where

\[
\alpha = \frac{1}{2^n} \sum_{i=0}^{n-1} 2^i a_i \quad (5.14)
\]

Control word \( a_i = [a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0] \) can be applied to the CDN externally and \( n \) is the number of
bits. The DCCDVC is described by the port relations given in equation (5.15) and its symbol is shown
in Fig. 5.8. The CMOS implementation of digital current-controlled differential voltage conveyor is
shown in Fig. 5.9.

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For the DCCDVC, the expression of the digitally-controlled, intrinsic X-terminal resistance, \( R_{XD} \) is derived from equation (5.11) by replacing \( I_B \) with \( aI_B \) can be given as:

\[
R_{XD} = \left[ 8\mu_n C_{ox} \frac{W}{L} \alpha I_B \right]^{-1/2}
\]

(5.16)

Where \( \alpha \) is given in (5.14).

5.4 Low-Voltage Digitally-Programmable Multifunctional Filters

This section presents two CM digitally-programmable filters operating at low voltages. The first is a reconfigurable continuous time first-order multifunctional filter while the second is a second-order biquadratic filter.
First-Order Digitally-Programmable Multifunctional Filter

The proposed low-voltage CM first-order multifunctional filter uses a CCII, a DPCCII and a grounded resistor and capacitor. Its schematic diagram is shown in Fig. 5.10. The DPCCII uses an inverse N-block and its CMOS implementation is shown in Fig. 5.11.

Figure 5.10. The digitally controlled current-mode first order multifunctional filter

Figure 5.11. CMOS implementation of a 3-bit DPCCII of Fig. 5.10
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By putting \( m = -1 \) in equation (5.7), and analyzing the circuit of Fig. 5.10, the current transfer functions \( T_{LP}, T_{HP} \) and \( T_{AP} \) for low-pass, high-pass and all-pass responses can respectively be obtained as:

\[
T_{LP} = \frac{I_{LP}}{I_{IN}} = \frac{N/RC}{s + N/RC} \quad (5.17)
\]

\[
T_{HP} = \frac{I_{HP}}{I_{IN}} = \frac{s}{s + N/RC} \quad (5.18)
\]

\[
T_{AP} = \frac{I_{AP}}{I_{IN}} = \frac{s - N/RC}{s + N/RC} \quad (5.19)
\]

From equations (5.17)-(5.19) it is evident that the pole frequency is:

\[
\omega_0 = \frac{N}{RC} \quad (5.20)
\]

Equation (5.20) show that the pole frequency is directly proportional to the digital control word \( N \).

**Effect of Non-Idealities**

Taking the non-idealities of CCIs into account, the relationship of the terminal voltages and currents can be rewritten as:

\[
V_X = \beta_k V_Y, \quad I_{Z+} = a_{k1}I_X, \quad I_{Z-} = -a_{k2}I_X \quad (5.21)
\]

In equation (5.21) \( \beta_k \) is the voltage transfer gain from terminal-Y to terminal-X for the \( k \)th CCII and \( a_{k1}, a_{k2} \) are the current-transfer gains for the \( k \)th CCII from X to \( Z+ \) and \( Z- \) respectively. Using equation (5.21), the non-ideal transfer functions can be obtained as:

\[
T_{LP} = \frac{I_{LP}}{I_{IN}} = \frac{\beta_1 a_{11}N}{\beta_2 a_{22}RC} \frac{s + \beta_1 a_{12}N}{s + \beta_2 a_{22}RC} \quad (5.22)
\]

\[
T_{HP} = \frac{I_{HP}}{I_{IN}} = \frac{s a_{11}N}{a_{22}RC} \frac{s + \beta_1 a_{12}N}{s + \beta_2 a_{22}RC} \quad (5.22)
\]

\[
T_{AP} = \frac{I_{AP}}{I_{IN}} = \frac{\beta_2 a_{21}}{\beta_{12} a_{22}} \left[ \frac{s - \beta_1 a_{12}N}{\beta_2 a_{22}RC} \right] \frac{s + \beta_1 a_{12}N}{s + \beta_2 a_{22}RC} \quad (5.24)
\]

From equations (5.22), (5.23) and (5.24) the pole frequency of filter becomes:

\[
\omega_{0,n} = \frac{\beta_1 a_{13}N}{\beta_2 a_{23}RC} \quad (5.25)
\]

From equation (5.25), it is obvious that the non-idealities in the transfer functions affect the pole-frequency.
Design and Verification

The digitally-programmable CM first-order multifunctional filter of Fig. 5.10, is designed and verified by PSPICE simulation with a supply voltage of ± 0.75V using CMOS TSMC 0.25µm technology parameters. The CMOS DPCCII with 3-bit current summing network at port-X (i.e. m = −1) of Fig. 5.11 is used. The aspect ratios of the transistors used in DPCCII are given in the Table 5.1. These aspect ratios are valid for CCII as well. The filter pole frequency is obtained as \( \omega_0 = N/RC \). Initially, the filter is designed for a pole frequency of 159.1 KHz with \( N = 1 \), \( R = 1k\Omega \) and \( C = 1nF \). The pole frequency is controlled through a digital control word \( N \). The observed low-pass and high-pass frequency responses of the filter for different control words (\( N=1, 2, 4, 7 \)) is given in Fig. 5.12. The simulated frequencies are found to be 158.1 KHz, 318.1 KHz, 630.9 KHz and 1.11 MHz with respect to theoretical frequency values of 159.15 KHz, 318.3 KHz, 636.6 KHz and 1.27 MHz respectively. The gain and phase plot of the all-pass filter for different control words (\( N =1, 2, 4, 7 \)) are shown in Fig. 5.12, which are in close conformity with the design.

Table 5.1. MOS Aspect ratio for DPCCII of Fig. 5.11

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Aspect ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>M_1, M_2, M_31, M_12</td>
<td>5/0.25</td>
</tr>
<tr>
<td>M_3, M_4, M_33, M_14</td>
<td>0.5/0.5</td>
</tr>
<tr>
<td>M_5, M_6, M_6A, M_15, M_16, M_16A</td>
<td>25/0.25</td>
</tr>
<tr>
<td>M_7, M_7A, M_17, M_17A</td>
<td>50/0.25</td>
</tr>
<tr>
<td>M_8, M_8A, M_18, M_18A</td>
<td>100/0.25</td>
</tr>
<tr>
<td>M_19, M_26, M_21, M_22, M_23, M_24</td>
<td>25/0.25</td>
</tr>
</tbody>
</table>

Figure 5.12. Frequency response of the digitally programmable LP and HP filters
Low-Voltage Digitally-Programmable Second-Order Filter

The proposed digitally programmable CM second-order filter is shown Fig. 5.14. The circuit uses three digitally programmable CCIIs, two grounded capacitors and four grounded resistors. DPCCIIs (1) and (2) have a gain of \( N \) while DPCCI (3) has a gain of \( N^{-1} \).

![Proposed digitally programmable biquadratic filter](image)

Figure 5.14. Proposed digitally programmable biquadratic filter

Analysis of the above circuit using equation (5.7) yields the following transfer functions:

\[
T_{LP} = \frac{I_{LP}}{I_{IN}} = \frac{(N_1N_2)(C_1C_2R_1R_2)}{D(S)}  
\]

\[
T_{BP} = \frac{I_{BP}}{I_{IN}} = \frac{s(N_1R_3)(N_4C_2R_1R_4)}{D(S)}  
\]

\[
T_{HP} = \frac{I_{HP}}{I_{IN}} = \frac{s^2}{D(S)}  
\]

with \( D(S) = s^2 + \frac{N_1R_3}{N_2C_2R_1R_4} + \frac{N_4N_2}{C_1C_2R_1R_2} \)
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Equations (5.26) to (5.29) represents low-pass, band-pass and high-pass transfer functions respectively.

The filter gain parameters are:

\[ H_{HP} = 1, \quad H_{BP} = 1, \quad H_{LP} = 1 \quad (5.30) \]

and the pole frequency and pole-Q are given as:

\[ \omega_0 = \frac{N_1 N_2}{\sqrt{C_1 C_2 R_1 R_2}} \quad (5.31) \]

\[ Q = \frac{N_3 R_4}{r_3 \sqrt{N_1 C_1 R_2}} \quad (5.32) \]

From equation (5.31) and (5.32) it is clear that the pole frequency and pole-Q can be digitally controlled independent of each other. Assuming \( R_1 = R_2 = R_3 = R_4 = R \), \( C_1 = C_2 = C \) and \( N_1 = N_2 = N \), equations (5.31) and (5.32) reduce to:

\[ \omega_0 = \frac{N}{RC} \quad (5.33) \]

\[ Q = N_3 \quad (5.34) \]

Equation (5.34) shows that the pole-Q is directly proportional to the control word applied at DPCCII ③.

**Non-Ideal Study**

Taking the non-idealities of CCIIs into account as mentioned in Section 2.3, the circuit shown in Fig. 5.14 is analysed and the non-ideal transfer functions are obtained as:

\[ T_{LP,n} = \frac{I_{LP}}{I_{IN}} = \frac{\beta_1 \beta_2 \alpha_{11} \alpha_{12} N_1 N_2}{D_n(s)} / (R_1 R_2 C_1 C_2) \quad (5.35) \]

\[ T_{BP,n} = \frac{I_{BP}}{I_{IN}} = \frac{s \beta_3 \alpha_{21} \beta_3 \alpha_{22} N_3}{D_n(s)} / (C_2 R_1 R_2) \quad (5.36) \]

\[ T_{HP,n} = \frac{I_{HP}}{I_{IN}} = \frac{s^2}{D_n(s)} \quad (5.37) \]

where

\[ D_n(s) = s^2 + s \beta_1 \beta_2 \alpha_{21} \alpha_{22} N_1 N_2 + \beta_1 \beta_2 \alpha_{11} \alpha_{12} N_1 N_2 \quad (5.38) \]

In equations (5.35) to (5.38), \( \beta_i \) is the voltage gain from Y and X terminal of DPCCII-\( i \) and \( \alpha_{ij} \) and \( \alpha_{ni} \) are the current transfer gains from X terminal to Z+ and Z− respectively where \( i = 1, 2, 3 \). The pole-frequency and pole-Q of the proposed filter, affected in the presence of non-idealities are now:
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\[
\omega_{o,n} = \sqrt{\frac{\beta_1 \beta_2 a_{11} a_{22} N_1 N_2}{C_1 C_2 R_1 R_2}}
\]  
(5.39)

\[
Q_n = \frac{N_3 R_4}{a_{21} \alpha_{23} \beta_3 R_3} \sqrt{\frac{\beta_2 a_{11} a_{22} N_2 C_2 R_1}{\beta_1 N_1 C_1 R_2}}
\]  
(5.40)

The passive sensitivities of \(\omega_{o,n}\) and \(Q_n\) are given as:

\[
S_{\omega_{o,n}}^{R_1 R_2 C_4 C_2} = \frac{1}{2}, \quad S_{\beta_1, \beta_2, a_{11}, a_{22}, N_1, N_2}^{\omega_{o,n}} = \frac{1}{2}
\]
\[
S_{R_2 a_{21}, a_{22}, C_2 R_1}^{Q_n} = \frac{1}{2}, \quad S_{\beta_1, \beta_2, a_{11}, a_{22}, N_1, N_2}^{Q_n} = -\frac{1}{2}
\]
\[
S_{a_{21}, a_{22}, R_3}^{Q_n} = -1, \quad S_{N_3 R_4}^{Q_n} = 1
\]  
(5.41)

From equation (5.41) it is clear that the sensitivities are less than or equal to unity in magnitude.

**Parasitic Study**

The effect of parasitics due to the presence of CCII within the proposed circuit is analyzed which reveals port-Z parasitics in the form of series resistance \(R_Z\), port-Y parasitics in the form of \(R_Y/C_Y\) and port-X parasitics in the form of series resistance \(R_X\). The modified transfer functions taking into account the above parasitics can then be expressed as:

\[
T_{LP,P} = \frac{I_{LP}}{I_{IN}} = \frac{(N_1 N_2) [s C_p R_3 + 1]}{(C_1 C_2 R_1 R_2')}
\]  
(5.42)

\[
T_{BP,P} = \frac{I_{BP}}{I_{IN}} = \frac{s (N_1 R_3) (N_3 C_2 R_1') R_4')}{D_p(s)}
\]  
(5.43)

\[
T_{HP,P} = \frac{I_{HP}}{I_{IN}} = \frac{s^2 [s C_p R_3 + 1]}{D_p(s)}
\]  
(5.44)

where \(D_p(s) = s^3 C_p R_3 + s^2 + s \left[ \frac{N_1 R_3}{N_3 C_2 R_1 R_4'} + \frac{N_1 N_2 C_p R_3}{C_1 C_2 R_1 R_2'} + \frac{N_1 N_2}{C_1 C_2 R_1 R_2'} \right] + \frac{N_1 N_2}{C_1 C_2 R_1 R_2'}
\]  
(5.45)

where \(R_1' = R_1 + R_\xi\), \(R_2' = R_2 + R_\xi\), \(R_3' = R_1 + R_\xi\), \(C_1' = C_1 + C_2 + C_Y\), \(C_2' = C_2 + 3(C_2 + C_Y)\).

Since the parasitic capacitances \(C_Z\), \(C_Y\) are in the range of \(\Omega\) and the port-Y parasitic resistances in the range of \(\Omega\), these may be neglected from the above equations. However, the same cannot be said for the parasitic capacitances \(C_Z\), \(C_Y\). They appear in parallel with \(R_\xi\), and thus result in undesired pole/zero in the transfer functions. But, the inclusion of these poles/zeros will not affect the dominant pole frequency of the circuit and would only restrict the high frequency performance.
Design and Verification

The proposed filter, shown in Fig. 5.14, is verified by designing it for a variable pole frequency by selecting different control words. The supply voltages are taken as \( V_{DD} = V_{SS} = \pm 0.75V \) and the aspect ratios are as shown in Table 5.1. The element values chosen are \( R_1 = R_2 = R_3 = R_4 = R = 1K\Omega \) and \( C_1 = C_2 = C = 0.4nF \). The filter responses are obtained by applying the same control words \( (N_1 = N_3) \) to DCCCIIs \( \mathbb{1} \) and \( \mathbb{2} \). Fig. 5.15 and 5.16 shows the low-pass and the high-pass responses. The band-pass response is depicted in Fig. 5.17. All the responses are obtained for the control word \( N = 1, 2, 4, 7 \) and corresponds to curves A, B, C and D in Fig. 5.15 to Fig. 5.17. In addition, all the responses have a gain of unity. The simulated pole frequencies obtained are 385KHz, 786KHz, 1.58MHz and 2.7MHz while the corresponding theoretical frequency values are 397.8KHz, 795.7KHz, 1.59MHz and 2.78MHz respectively. The variation of pole-Q by varying \( N_3 \) (as 1, 2, 4 and 7) at 385KHz frequency is shown in Fig. 5.18 and the values of pole-Q obtained through simulation are 1, 1.98, 3.85 and 6.7 while the corresponding theoretical values are 1, 2, 4 and 7 respectively.

![Figure 5.15. Tuning of low-pass filter function with digital control word](image1)

![Figure 5.16. Tuning of high-pass filter function with digital control word](image2)
5.5 Digitally-Controlled Fully-Differential Voltage- and Transadmittance-Mode Biquadratic Filter

The proposed digitally-controlled FD biquadratic filter is shown in Fig. 5.19. It employs five DCCDVCs (described in section 5.3), one resistor and two capacitors.

Analysis of the above circuit shown in Fig. 5.19 yields the following VM transfer functions:
From equation (5.49), the pole-configuration.

The above equations (5.46)-(5.48) indicate that the proposed filter produces high-pass, band-pass and low-pass functions. The digitally-controllable gain constants $H_{HP}$, $H_{BP}$ and $H_{LP}$ are as below:

$$H_{HP} = \frac{R}{R_{XD1}}, \quad H_{BP} = \frac{R_{XD3}}{R_{XD1}}, \quad H_{LP} = \frac{R_{XD2}}{R_{XD1}}$$

(5.50)

In addition to the VM transfer functions, FD transadmittance-mode transfer functions $HP$, $BP_1$, $BP_2$ and $LP$ are obtained as:

$$I_{HP} = \frac{I_{03} - I_{04}}{V_{id}} = \frac{s^2(2R/R_{XD1}R_{XD4})}{D(s)}$$

(5.51)

$$I_{BP1} = \frac{I_{05} - I_{06}}{V_{id}} = \frac{s(2R/C_1R_{XD1}R_{XD4}R_{XD5})}{D(s)}$$

(5.52)

$$I_{LP} = \frac{I_{01} - I_{02}}{V_{id}} = \frac{(C_2C_1R_{XD1}R_{XD2}R_{XD4}R_{XD5})}{D(s)}$$

(5.53)

$$I_{BP2} = \frac{I_{07} - I_{08}}{V_{id}} = \frac{s(2R/C_1R_{XD1}R_{XD3}R_{XD4})}{D(s)}$$

(5.54)

$$K_{HP} = \frac{2R}{R_{XD1}R_{XD4}}, \quad K_{BP1} = \frac{2R_{XD3}}{R_{XD1}R_{XD5}}, \quad K_{LP} = \frac{2}{R_{XD1}}, \quad K_{BP2} = \frac{2}{R_{XD3}}$$

(5.55)

where $K_{HP}$, $K_{BP1}$, $K_{LP}$ and $K_{BP2}$ are the digitally-controllable gain constants in transadmittance-mode configuration.

From equation (5.49), the pole-$\omega_0$ and pole-$Q$ of the filter are calculated as:

$$\omega_0 = \frac{R}{\sqrt{C_1C_2R_{XD2}R_{XD4}R_{XD5}}}$$

(5.56)

$$Q = R_{XD3} \frac{C_1R_{XD4}}{\sqrt{C_2R_{XD2}R_{XD5}}}$$

(5.57)

The passive sensitivities can be found as:
Taking into consideration the non-idealities of the DCCDVC, the terminal relations in equation (5.15) can be expressed as:

\[
\begin{align*}
S_{c_1,R_{XD2},R_{XD4},R_{XD5}}^q &= -\frac{1}{2}, \\
S_{c_2}^q &= \frac{1}{2}, \\
S_R^q &= \frac{1}{2}, \\
S_{R_{XD2},R_{XD4},R_{XD5}}^q &= -\frac{1}{2}
\end{align*}
\] (5.58)

\[
S_{R_{XD3}}^q = 1, \quad S_{c_1}^q = \frac{1}{2}, \quad S_{c_2}^q = -\frac{1}{2}, \quad S_{R_{XD2},R_{XD4},R_{XD5}}^q = -\frac{1}{2}
\]

From equation (5.58), it can be observed that all sensitivities are low. Selecting \(R_{XD1} = R_{XD5} = R_{XD}\) and \(C_1 = C_2 = C\), equations (5.55) and (5.56) reduce to:

\[
\omega_0 = \frac{1}{CR_{XD}} \sqrt{\frac{R}{R_{XD2}}}
\] (5.59)

\[
Q = R_{XD3} \sqrt{\frac{1}{RR_{XD2}}}
\] (5.60)

Equations (5.59) and (5.60) reveal that the pole-\(\omega_0\) and pole-\(Q\) can be independently controlled by digitally varying the intrinsic resistances \(R_{XD}\) and \(R_{XD3}\) respectively.

**Effect of Non-Idealities**

Taking into consideration the non-idealities of the DCCDVC, the terminal relations in equation (5.15) can be expressed as:

\[
\begin{bmatrix}
V_X \\
I_{V_1} \\
I_{V_2} \\
I_{Z^+} \\
I_{Z^-}
\end{bmatrix} =
\begin{bmatrix}
R_{XD} & \beta_1 & \beta_2 & 0 & 0 & I_X \\
0 & 0 & 0 & 0 & 0 & V_{V_1} \\
0 & 0 & 0 & 0 & 0 & V_{V_2} \\
\alpha_1 & 0 & 0 & 0 & 0 & V_{Z^+} \\
-\alpha_2 & 0 & 0 & 0 & 0 & V_{Z^-}
\end{bmatrix}
\] (5.61)

Using (5.61), the circuit shown in Fig. 5.19 yields the following non-ideal differential output voltages and currents:

\[
V_{HP} = V_{01} - V_{02} = (V_{11} - V_{12}) \frac{s^2(R/R_{XD1})}{D_n(s)}
\] (5.62)

\[
V_{BP} = V_{03} - V_{04} = (V_{11} - V_{12}) \frac{s(\beta_{14}a_{14}R)}{D_n(s)}
\] (5.63)

\[
V_{LP} = V_{05} - V_{06} = \frac{\beta_{14}a_{14}a_{15}R}{D_n(s)}
\] (5.64)

\[
I_{MHP} = I_{03} - I_{04} = (V_{11} - V_{12})(s^2(a_{14} + a_{24})(\beta_{14}R/R_{XD1}R_{XD4}))
\] (5.65)

\[
I_{MBP1} = I_{07} - I_{08} = (V_{11} - V_{12}) \frac{s(\alpha_{13} + \alpha_{23})(\beta_{13}a_{14}a_{15}R)}{D_n(s)}
\] (5.66)

\[
I_{MLP} = I_{01} - I_{02} = (V_{11} - V_{12}) \frac{\beta_{13}\beta_{14}a_{14}a_{15}R}{D_n(s)}
\] (5.67)
From equation (5.62) to (5.68) the non-ideal differential-mode gain $A_{DM}$ and common-mode gain $A_{CM}$ can be expressed as:

$$I_{MBP2} = I_{DS} - I_{B6} = \left(V_{11} - V_{12}\right) \frac{s\left(a_{15} + a_{23}\right) \left(\frac{\beta_{15} + \beta_{21}a_{14}R}{C_{1}R_{XD1}R_{XD2}R_{XD4}R_{XD5}}\right)}{D_n(s)}$$

$$A_{DM-HP} = 0.5(\beta_{11} + \beta_{21})a_{11} \frac{s^2(R/R_{XD1})}{D(s)}$$

$$A_{CM-HP} = (\beta_{11} - \beta_{21})a_{11} \frac{s^2(R/R_{XD1})}{D(s)}$$

$$A_{DM-BP} = 0.5(\beta_{11} + \beta_{21}) \frac{s\left(\frac{\beta_{14}a_{11}a_{14}R}{C_{1}R_{XD1}R_{XD4}}\right)}{D_n(s)}$$

$$A_{CM-BP} = (\beta_{11} - \beta_{21}) \frac{s\left(\frac{\beta_{14}a_{11}a_{14}a_{15}R}{C_{1}C_{2}R_{XD1}R_{XD4}R_{XDS}}\right)}{D_n(s)}$$

$$A_{DM-LP} = 0.5(\beta_{11} + \beta_{21}) \frac{s\left(\frac{\beta_{14}a_{11}a_{14}a_{15}R}{C_{1}C_{2}R_{XD1}R_{XD4}R_{XDS}}\right)}{D_n(s)}$$

$$A_{CM-LP} = (\beta_{11} - \beta_{21}) \frac{s\left(\frac{\beta_{14}a_{11}a_{14}a_{15}R}{C_{1}C_{2}R_{XD1}R_{XD4}R_{XDS}}\right)}{D_n(s)}$$

$$A_{DM-MHP} = 0.5(\beta_{11} + \beta_{21}) \frac{s^2(a_{14} + a_{24})(\beta_{14}a_{11}R/R_{XD1}R_{XD4})}{D_n(s)}$$

$$A_{CM-MHP} = (\beta_{11} - \beta_{21}) \frac{s^2(a_{14} + a_{24})(\beta_{14}a_{11}R/R_{XD1}R_{XD4})}{D_n(s)}$$

$$A_{DM-MBP1} = 0.5(\beta_{11} + \beta_{21}) \frac{s(a_{13} + a_{23})\left(\frac{\beta_{13}a_{14}a_{11}a_{14}R}{C_{1}C_{2}R_{XD1}R_{XD3}R_{XD4}}\right)}{D_n(s)}$$

$$A_{CM-MBP1} = (\beta_{11} - \beta_{21}) \frac{s(a_{13} + a_{23})\left(\frac{\beta_{13}a_{14}a_{11}a_{14}R}{C_{1}C_{2}R_{XD1}R_{XD3}R_{XD4}}\right)}{D_n(s)}$$

$$A_{DM-MBP2} = 0.5(\beta_{11} + \beta_{21}) \frac{s(a_{15} + a_{25})\left(\frac{\beta_{15}a_{14}a_{11}a_{14}R}{C_{1}C_{2}R_{XD1}R_{XD4}R_{XDS}}\right)}{D_n(s)}$$

$$A_{CM-MBP2} = (\beta_{11} - \beta_{21}) \frac{s(a_{15} + a_{25})\left(\frac{\beta_{15}a_{14}a_{11}a_{14}R}{C_{1}C_{2}R_{XD1}R_{XD4}R_{XDS}}\right)}{D_n(s)}$$

where $D_n(s) = s^2 + s \frac{\beta_{13}\beta_{14}a_{22}a_{14}a_{15}R}{C_{1}C_{2}R_{XD1}R_{XD2}R_{XD4}R_{XDS}} + \frac{\beta_{12}\beta_{14}a_{22}a_{14}a_{15}R}{C_{1}C_{2}R_{XD1}R_{XD2}R_{XD4}R_{XDS}}$.

From equation (5.81) the non-ideal values of the pole frequency- $\omega_{0,n}$ and pole-$Q_n$ are obtained as:

$$\omega_{0,n} = \sqrt{\frac{\beta_{12}\beta_{14}a_{22}a_{14}a_{15}R}{C_{1}C_{2}R_{XD1}R_{XD2}R_{XD4}R_{XDS}^2}}, \quad Q_n = \frac{R_{XD1}}{\beta_{13}a_{23}^2} \sqrt{\frac{\beta_{12}\beta_{14}a_{22}a_{14}a_{15}C_{1}R_{XD1}}{C_{1}C_{2}R_{XD2}R_{XD4}R_{XDS}}^2}$$
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From equation (5.82) it is clear that the effect of non-idealities for the circuit parameters \( \varepsilon_{0,\alpha} \) and pole-Q, can be made negligible by pre-distortion of \( R, C \) and \( C_s \). The CMRR for all filter responses in voltage- and transadmittance-mode as depicted from equations (5.69) to (5.80) can be represented as:

\[
CMRR = \frac{0.5(\beta_{11} + \beta_{21})}{(\beta_{11} - \beta_{21})}
\]  

(5.83)

Equation (5.83) shows that the CMRR is inversely proportional to the difference in voltage transfer gain from the \( Y_1 \) and \( Y_2 \) terminals of the DCCDVC-1, which for an integrated realization would be highly matched. Thus a very high value of CMRR can be achieved.

Parasitics Study

In this section the parasitics associated with the DCCDVC are considered. The DCCDVC comprises of resistances and capacitances connected in parallel at terminals \( Y \) and \( Z \) i.e. \( R_{Y}/C_{Y} \), \( R_{Z}/C_{Z} \) and \( R_{X} \) at terminal \( X \) where \( i = 1 \) to 5 corresponds to the \( i \)th DCCDVC. Due to the presence of these parasitics, the passive components values are changed to:

At node A:  \[ C_{1p} = C_{Z1}/C_{Z2}/C_{Z3}/C_{Y1}, R_{1p} = R_{Z1}/R_{Z2}/R_{Z3}/R_{Y1}, Z_{p1} = C_{1p}/R_{1p} \]

At node B:  \[ C_{2p} = C_{Z4}/C_{Y5}, R_{2p} = R_{Z4}/R_{Y5}, Z_{p2} = C_{2p}/R_{2p} \]  

(5.84)

At node C:  \[ C_{3p} = C_{Z5}/C_{Y3}, R_{3p} = R_{Z5}/R_{Y3}, Z_{p3} = C_{3p}/R_{3p} \]

Since integrator blocks DCCDVC \( 4 \) and \( 5 \) are identical, the parasitics associated with DCCDVC are also identical i.e \( Z_{p2} = Z_{p3} \).

On re-analyzing the proposed filter associated with the above capacitances, the VM and transadmittance-mode transfer gain expressed in equations (5.46) to (5.48) and (5.51) to (5.54) are modified to:

\[
\begin{align*}
\frac{V_{hp}}{V_{id}} &= \frac{V_{o1} - V_{o2}}{V_{id}} = s^2 \frac{k}{R_{X1}} + s \frac{k}{2R_{X1}Z_{p2}} \left( \frac{C_1 + C_2}{C_1 C_2} \right) + \frac{k}{4C_1 C_2 R_{X1} Z_{p2}^2} \\
\frac{V_{bp}}{V_{id}} &= \frac{V_{o3} - V_{o4}}{V_{id}} = \frac{k}{C_1 R_{X1} R_{X4}} + \frac{k}{2C_1 C_2 R_{X1} R_{X4} Z_{p2}} \\
\frac{V_{lp}}{V_{id}} &= \frac{V_{o5} - V_{o6}}{V_{id}} = \frac{2Z_{p2}}{R_{X5} (2S C_2 Z_{p2} + 1)} \left[ s \frac{k}{C_1 R_{X1} R_{X4}} + \frac{k}{2C_1 C_2 R_{X1} R_{X4} Z_{p2}} \right] \\
\frac{I_{hp}}{V_{id}} &= \frac{I_{o3} - I_{o4}}{V_{id}} = \frac{2}{R_{X3}} \left[ s \frac{k}{R_{X1}} + s \frac{k}{2R_{X1}Z_{p2}} \left( \frac{C_1 + C_2}{C_1 C_2} \right) + \frac{k}{4C_1 C_2 R_{X1} Z_{p2}^2} \right] \\
\frac{I_{bp1}}{V_{id}} &= \frac{I_{o7} - I_{o8}}{V_{id}} = \frac{2}{R_{X3}} \left[ s \frac{k}{C_1 R_{X1} R_{X4}} + \frac{k}{2C_1 C_2 R_{X1} R_{X4} Z_{p2}} \right] \\
\end{align*}
\]

(5.85) to (5.89)
Under the influence of parasitic elements, the pole-frequency and pole-Q of the proposed filter are modified to:

\[ \omega'_0 = \omega_0 \sqrt{r} \]  

(5.93)

and

\[ Q' = Q \frac{R \sqrt{r}}{\left( \frac{R X D_3 R X_D 4 (C_1 + C_2)}{2 C_2 Z_{p2}} + k \right)} \]  

(5.94)

where

\[ r = \frac{R + R X_3 R X_4 k}{R X_3 R X_4 Z_{p2}} + \frac{R X_3 R X_4 R X_5}{4 R X_3 R X_4 Z_{p2}} \]  

(5.95)

From equations (5.85)-(5.94) it is clear that the filter gains and parameters are influenced by parasitic elements. With \( Z_{p1} \gg R \) and \( Z_{p2} \gg R_X \), \( k \) and \( r \) are approximated as \( k = R \) and \( r = 1 \). Consequently, equations (5.93) and (5.94) are modified to:

\[ \omega'_0 \approx \omega_0 \approx \frac{R}{\sqrt{C_1 C_2 R X_3 R X_4 R X_5}} \]  

(5.96)

\[ Q' \approx Q \approx \frac{R X_3 R X_4}{\sqrt{C_2 R X_3 R X_4}} \]  

(5.97)

Equations (5.96) and (5.97) prove that the effect of parasitic impedances can be ignored and hence the filter response can be assumed to be ideal.

**Design and Verification**

The performance of the proposed circuit shown in Fig. 5.19 is verified by simulation. The DCCDVC is simulated using 0.5\( \mu \)m CMOS technology parameters. Supply voltages are kept as \( V_{dd} = -V_{ss} = 2.5\text{V} \) and \( V_{ss} = -1.6\text{V} \) [144]. The proposed filter is designed with \( R = 1\text{K}\Omega \) and \( C_1 = C_2 = 150\text{pF} \).
Variation in the pole-frequencies of the filter in both voltage and transadmittance mode at different control words are shown in Table 5.2 and Table 5.3 respectively. Table 5.2 shows the variation of high-pass responses with the different control words while Table 5.3 shows the low-pass and band-pass responses. Table 5.2 shows the pole-frequency variation after applying the digital control word to the DCCDVCs. Table 5.2 and 5.3 depicts the variation of high-pass, band-pass and low-pass response by varying control words $a_{i2}$, $a_{i4}$ and $a_{i5}$ (keeping $a_{i4} = a_{i5}$). In Tables 5.2 and 5.3, for each of the given values of pole-frequency, the set of control words chosen for $a_{i2}$, $a_{i4}$ and $a_{i5}$ are the same. The condition to obtain unity-gain for the low-pass output is $a_{i4} = a_{i5}$. Similarly, the conditions to get unity gain for a band-pass output is $a_{i3} = a_{i4}$ as depicted in Table 5.3. This table also shows that the variation in frequency by varying $a_{i2}$, $a_{i4}$ and $a_{i5}$ from 1.2MHz to 12MHz with a unity gain having a pole-Q equal to 1.11.

Simulated frequency responses of the high-pass filter are shown in Fig. 5.20 which indicates that the variation in frequency from 1.2MHz to 12MHz corresponds to the digital control word as depicted in Table 5.2. The obtained VM low-pass and band-pass responses corresponding to Table 5.3 are shown in Fig. 5.21 and Fig. 5.22 respectively. The variation of pole-Q is presented in Fig. 5.23. The high-pass output for the transadmittance mode, as shown in Fig. 5.24, is obtained using the digital control words of Table 5.2. Fig. 5.25 and Fig. 5.26 show the low-pass and band-pass outputs in transadmittance mode respectively. The time domain response of VM band-pass output is shown in Fig. 5.27 which is obtained by applying a 200mV peak-peak input at a frequency of 12MHz. The THD at this signal frequency was found to be 1.8%. Its Fourier spectrum is shown in Fig. 5.28 which proves that harmonics of negligible magnitude are present at 36MHz and 48MHz. The CMRR analysis of the proposed circuit is also performed. The FD nature of the circuit is especially desirable for common-mode signals. CMRR variation for low pass output at 12MHz output is shown in Fig. 5.29. This is obtained by ensuring that mismatch in the aspect ratio of the input transistors at the differential stage of Fig. 5.9 i.e. $M_1$ and $M_3$ is limited to 0.1%. Figure 5.29 shows a very high CMRR, thus emphasizing a FD operation.

Table 5.2. Variation of frequency with control word for HP in voltage- and transadmittance-mode

<table>
<thead>
<tr>
<th>Curve</th>
<th>Control word $(a_{i4}, a_{i5})$</th>
<th>Control word $(a_{i2})$</th>
<th>Control word $(a_{i3})$</th>
<th>Control word $(a_{i1})$</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>00000001 0.004</td>
<td>00000001 0.004</td>
<td>00000011 0.004</td>
<td>00000001 0.004</td>
<td>1.2</td>
</tr>
<tr>
<td>B</td>
<td>00100001 0.128</td>
<td>00000001 0.004</td>
<td>00000001 0.004</td>
<td>00000001 0.004</td>
<td>3</td>
</tr>
<tr>
<td>C</td>
<td>10010001 0.566</td>
<td>00000001 0.004</td>
<td>00000010 0.004</td>
<td>00000001 0.004</td>
<td>6</td>
</tr>
</tbody>
</table>
Table 5.3. Variation of frequency with control word for LP and BP in voltage- and transadmittance-mode

<table>
<thead>
<tr>
<th>Curve</th>
<th>Frequency (MHz)</th>
<th>Control word ( a_i2 ) ( a_i4 ) ( a_i5 )</th>
<th>Control word ( a_i3 )</th>
<th>( a_i3 )</th>
<th>( a_i5 )</th>
<th>( a_i4=0 )</th>
<th>( a_i3-0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.2</td>
<td>000000001 0.004 00000001 0.004</td>
<td>00000011 0.004</td>
<td>00000011 0.012</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>3</td>
<td>00100001 0.128 00000001 0.004</td>
<td>00000001 0.004</td>
<td>00000001 0.004</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>6</td>
<td>1001001 0.566 00000001 0.004</td>
<td>00000010 0.004</td>
<td>00000010 0.0078</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>12</td>
<td>11111111 0.996 11111111 0.996</td>
<td>00101111 0.089</td>
<td>00101111 0.089</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 5.4. Variation of BP filter pole-Q with control word at 12MHz for \( a_i2=0 \) \( a_i4=0 \) \( a_i5=0.996 \)

<table>
<thead>
<tr>
<th>Curve</th>
<th>Control word ( a_i2 )</th>
<th>( a_j )</th>
<th>Pole-Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>00011111</td>
<td>0.121</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>00001111</td>
<td>0.058</td>
<td>1.2</td>
</tr>
<tr>
<td>C</td>
<td>00001000</td>
<td>0.031</td>
<td>1.4</td>
</tr>
<tr>
<td>D</td>
<td>00000001</td>
<td>0.004</td>
<td>2.3</td>
</tr>
</tbody>
</table>

Figure 5.20. Tuning of high-pass filter function with digital control word
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Figure 5.21. Tuning of low-pass filter function with digital control word

Figure 5.22. Tuning of band-pass filter function with digital control word

Figure 5.23 Pole-Q variations with digital control word

Figure 5.24 High-pass variations in Trans-admittance mode
Figure 5.25 Low-pass variations in Trans-admittance mode

Figure 5.26 Band-pass variations in Trans-admittance mode

Figure 5.27 Band-pass output at 12MHz

Figure 5.28 Fourier spectrum of band-pass output at 12MHz
OTA Equivalent Circuit

The circuit of Fig. 5.19 is also implemented by using a digitally-programmable operational transconductance amplifier [79] as shown in Fig. 5.30.

5.6 Digitally-Programmable Mixed-Mode Quadrature Oscillator

The current-controlled current conveyor of Fig. 5.5 can be converted into a digitally-programmable current controlled conveyor (DPCCII) by incorporating the current division network (CDN) shown in the circuit of CCCII [144] (as discussed in Section 5.3). The DPCCII is characterized by the following port relationship:

\[ i_Y = 0; \quad V_X = V_Y + i_X R_{XD}, \quad \text{and} \quad i_Z = pi_X \]  

(5.98)
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where

\[ R_{XD} = \left[ 8\mu_mC_{ox}\frac{W}{L}aI_B \right]^{1/2} \]  

(5.99)

where \( I_B \) is the bias current applied at the input of the CDN. From equation (5.99), it can be seen that \( R_{XD} \) can be digitally controlled by varying the control parameter \( a \) for a fixed value of the bias current.

The proposed digitally programmable mixed-mode quadrature oscillator is shown in Fig. 5.31. Two voltage outputs in phase quadrature are obtained at the nodes marked ‘\( V_{01} \)’ and ‘\( V_{02} \)’. Two current-mode quadrature outputs are obtained at the high impedance nodes marked ‘\( I_{01} \)’ and ‘\( I_{02} \).

![Diagram of the proposed digitally programmable mixed-mode quadrature oscillator](image)

**Figure 5.31. Proposed digitally programmable mixed-mode quadrature oscillator**

The characteristic equation of the above circuit is:

\[ s^2 + s \left[ \frac{1}{R_{XD2}C_2} - \frac{1}{R_{XD1}C_1} \right] + \frac{1}{R_{XD1}R_{XD2}C_1C_2} = 0 \]

(5.100)

Using (5.100), the frequency and condition of oscillation (FO and CO respectively) can be obtained as:

**FO:** \( \omega_o = \frac{1}{\sqrt{R_{XD1}R_{XD2}C_1C_2}} \)  

(5.101)

**CO:** \( R_{XD1} \leq R_{XD2} \)  

(5.102)

Selecting \( C_1 = C_2 = C \), equation (5.101) reduces to

**FO:** \( \omega_o = \frac{1}{C\sqrt{R_{XD1}R_{XD2}}} \)  

(5.103)

The above equation shows that the frequency of oscillation can be independently controlled by varying \( C \) without affecting the condition of oscillation. The current outputs, separated in phase by 90°, can be written as:

\[ I_{02} = -jkI_{01} \]

(5.104)

where the constant ‘\( k \)’ is defined as:

\[ k = \frac{1}{\omega_o R_{XD1}C_2} \]

(5.105)

It can be deduced that for \( k = 1 \), equal amplitudes may be obtained for the quadrature current outputs.
The two voltage outputs are related as:

\[ V_2 = +jmV_1 \]  

where \( m = \frac{1}{\omega_0 R X D1 C_1} \)  

Equation (5.106) shows that the two voltage outputs will be in phase quadrature and will have equal amplitudes for \( m = 1 \), according to (5.107).

**Design and Verification**

The proposed oscillator is simulated by using \( C_1 = C_2 = 20\)pF and \( I_{b1} = I_{b2} = 225\)μA. The supply voltages are kept at ±2.5V. The frequency of oscillation obtained through simulation for a given control word \([0 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1]\) is found to be 19.32 MHz and the obtained quadrature voltage and current waveforms is shown in Fig. 5.32 and Fig. 5.33.

The performance of the proposed oscillator is analysed by plotting the FFT for the generated outputs. The obtained frequency spectrum is shown in Fig. 5.34. The THD is found to be 4% at 19.32MHz through simulation. Digital control of the frequency of oscillation using the control words of the two DPCCCIIs is also explored. Towards this end, the digital control parameter (\( a \)) is varied for the two DPCCCIIs. The values of oscillation frequency obtained for various choices of control words is presented in Table 5.5.

The entries in Table 5.5 can also be plotted graphically to give an indication of the linear range of operation of the proposed oscillator. From Fig. 5.35, it can be seen that the frequency varies linearly with the control word with values ranging from 11.78 MHz to 19.32 MHz.

<table>
<thead>
<tr>
<th>Control word ([a_7 \ a_6 \ a_5 \ a_4 \ a_3 \ a_2 \ a_1 \ a_0])</th>
<th>Digital Control Parameter (( a ))</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00001111</td>
<td>0.058</td>
<td>11.78</td>
</tr>
<tr>
<td>00010100</td>
<td>0.078</td>
<td>12.37</td>
</tr>
<tr>
<td>00011111</td>
<td>0.121</td>
<td>13.55</td>
</tr>
<tr>
<td>00110010</td>
<td>0.195</td>
<td>15.42</td>
</tr>
<tr>
<td>00111111</td>
<td>0.246</td>
<td>16.44</td>
</tr>
<tr>
<td>01111111</td>
<td>0.496</td>
<td>19.32</td>
</tr>
<tr>
<td>11111111</td>
<td>0.996</td>
<td>20.20</td>
</tr>
</tbody>
</table>
Figure 5.32. Quadrature voltage outputs

Figure 5.33. Quadrature current outputs

Figure 5.34. Obtained frequency spectrum for quadrature voltage outputs in the circuit of Fig. 5.31
5.7 Conclusion

In this Chapter, a novel digitally programmable CM first-order multifunctional filter using DPCCII and CCCII is presented. The realized filter can provide first-order CM low-pass, high-pass and all-pass responses without any component matching constraints. The pole frequency of the continuous time filter is directly proportional to an N-bit digital control word which offers programmability.

Next, a low-voltage digitally-programmable second-order multifunctional filter is realized. Notable features of the filters include operation at low voltage which is a desirable feature in the era of low power electronics. Secondly, filter pole frequency and pole-Q are independently controlled. Filter pole-Q is proportional to the control word applied to DPCCII-(3).

The third realized filter is a voltage-and transadmittance-mode biquadratic filter with digital control of filter parameters employing a new active element. The active element used is a DCCDVC which exhibits differential signal handling capability and digital tunability of the conveyor’s X-terminal resistance making it an ideal choice for fully integrated controlled filters. The operation of the proposed circuit in voltage-and transadmittance-mode makes the new circuit versatile. Non-idealities of the active element are also considered along with the parasitics involved, so as to evaluate the actual performance of the proposed filter. The results obtained are as per theoretical predictions and promise wide utility of the circuit with future scope of actual fabrication in CMOS technology.

Finally, this Chapter presents a digitally-programmable mixed-mode oscillator with which quadrature current outputs at high impedance and quadrature voltage outputs at low impedance are available simultaneously. The generated quadrature waveforms exhibited low harmonic distortion. Digital control of the frequency of oscillation is also demonstrated. The linearly tunable range of frequency was found to be approximately from 11.78MHz – 19.32MHz. The designed oscillator is CMOS compatible and suitable for monolithic implementation by virtue of grounded capacitors only.