CHAPTER 4
ANALOG SIGNAL PROCESSING MODULES USING DXCCII

This chapter presents first- and second- order CM and VM multifunctional filters with a single input. The approach adapted within this chapter results in a first-order CM multifunctional filter and a VM tunable all-pass filter. The former employs only a single active device (DXCCII) and four grounded passive components while the latter is designed with a single DD-DXCCII, one capacitor and a MOS resistor operating in the triode region. With the help of a tunable first order filter, an \( n \)-order filter is also designed by cascading \( n \)-stages. The proposed CM filter is implemented in hardware with the DXCCII realized using CFOAs (AD-844).

A cascadable second-order universal CM biquadratic filter is also designed which provides the entire CM functions i.e. high-pass, band-pass, low-pass, all-pass and band-reject. In addition, it also produces transresistance mode band-pass and low-pass filter functions simultaneously.

Finally, current-, voltage- and mixed-mode multiphase oscillators are designed in this Chapter.

4.1 Introduction

Numerous CM [29, 82-89] and VM filters [90-92] based on different active devices such as OTA, CCII, DVCC and CCCII have been proposed in literature. A few of them are discussed in Section 2.1 and 3.1. However, another active device, the dual-X second generation current conveyor (DXCCII) [54] is a better alternative when designing continuous-time tunable filters [93, 94]. The availability of normal and inverted X-outputs makes the device much more versatile in comparison to CCII, its counterpart. The DXCCII is therefore preferred for obtaining simpler and compact filter structures. This is the primary motivation behind the designs presented in this Chapter.

The proposed CM first-order filter section employs a DXCCII which provides low-pass, high-pass and all-pass outputs with a single current input. The filter section uses only two grounded resistors and capacitors each and a dual-X second generation multi-output current conveyor (DX-MOCCII). This filter section is then utilized to realize a CM four-phase sinusoidal oscillator (CM-FPSO). The CM-FPSO current outputs are loaded with equal-valued resistors to realize a voltage mode four-phase sinusoidal oscillator (VM-FPSO).
Regarding VM designs, as a first step, a tunable VM first-order filter is realized using differential difference dual-X second generation current conveyor (DD-DXCCII) [95]. The first-order all-pass filter employs only one passive component and does not require matching components.

It should be noted (see Section 1.3), that filters can be categorized to be of first-order, second-order or \(n\)th order. Higher the order of the filter, closer is the response to ideal characteristics. Consequently an \(n\)th-order all-pass filter is also realized. The phase at the pole-frequency of \(n\)th-order filters exhibit a large rate of change when compared to first- and second-order all-pass filters.

In both the above-mentioned designs, tuning of pole-frequency is possible by varying the gate potential of the triode MOSFET. However, it is obvious that both the filters fail to exhibit a universal behaviour. Thus a universal filter is also realized as discussed below.

A cascadable second-order CM universal filter is realized with a single current input. The filter employs two active devices and four passive components. All the passive components are grounded which facilitates IC implementation. In addition to CM outputs, two transresistance mode low-pass and band-pass responses are simultaneously obtained without requiring additional components. The CM band-pass output of this filter section is utilized to realize CM and VM three-phase oscillator simultaneously without needing additional components. The realized oscillator exhibits independent frequency control.

Next, the DXCCII is also utilized to realize a CMOS compatible third-order three-phase sinusoidal oscillator which offers mixed-mode operation. Technical literature is replete with numerous realizations of multiphase oscillators [18, 89, 96-110] using a variety of active devices but relatively few of them offer the facility of mixed-mode operation.

All the SPICE simulations of proposed circuits in this chapter were verified using TSMC 0.25µm CMOS device model parameters.

4.2 Dual-X Second Generation Multi-Output Current Conveyor (DX-MOCCII)

The DXCCII is a combination of a conventional CCII and an inverting CCII (ICCII) [1, 2]. It is more versatile as it combines the features of both. The DX-MOCCII can be characterized by the following matrix with \(i = 1, 2\)

\[
\begin{bmatrix}
I_Y \\
V_{XP} \\
V_{XN} \\
I_{Zpl} \\
I_{Zni}
\end{bmatrix}
= 
\begin{bmatrix}
0 & 0 & 0 \\
1 & 0 & 0 \\
-1 & 0 & 0 \\
0 & 1 & 0 \\
0 & 1 & 0
\end{bmatrix}
\begin{bmatrix}
V_Y \\
I_{xp} \\
I_{xn}
\end{bmatrix}
\]  

(4.1)
The electrical symbol of DX-MOCCII is shown in Fig. 4.1. It has two X terminals, namely \( X_p \) (non-inverting X terminal) and \( X_n \) (inverting X terminal). The \( X_p \) and \( X_n \) terminal currents are reflected at the \( Z_p \) and \( Z_n \) terminals respectively. (It is worth emphasizing that for this device, there is no direct relation between the \( Z_p \) and \( Z_n \) terminal currents.)

The CMOS implementation of the DX-MOCCII is given in Fig. 4.2 [54].

\[ \begin{align*}
\begin{bmatrix}
I_Y \\
V_{XP} \\
V_{XN} \\
I_{ZP} \\
I_{ZN}
\end{bmatrix} &=
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
\beta_p & 0 & 0 & 0 & 0 \\
-\beta_n & 0 & 0 & 0 & 0 \\
\alpha_p & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \alpha_n & 0
\end{bmatrix}
\begin{bmatrix}
V_Y \\
I_{XP} \\
I_{XN} \\
V_{ZP} \\
V_{ZN}
\end{bmatrix}
\end{align*} \] (4.2)

Figure 4.1 Symbol of DX-MOCCII

Figure 4.2 The CMOS structure of the DX-MOCCII [54].

Non Idealities Associated with DXCCII

This section presents the non-ideal relationship of voltages and currents within the DXCCII. The matrix equation defining a non-ideal DXCCII may be given as:
where $\beta_p(\beta_n)$ is the voltage transfer-gain from the Y-port to $X_p(X_n)$ port and $\alpha_p(\alpha_n)$ is the current transfer gain from the $X_p$ port to $Z_p$ port ($X_N$ port to $Z_N$ port) (ideally, these transfer gains are unity in magnitude).

**Parasitics Associated with DXCCII**

The parasitics associated with Y-port and $Z_p(Z_N)$-port of DXCCII has a parallel combination of a high-valued resistance with a low-valued capacitance i.e. $R_Y/C_Y$ and $R_{ZP}/C_{ZP}$ ($R_{ZN}/C_{ZN}$) respectively. The $X_p(X_N)$-port has a low value resistance $R_{XP}(R_{XN}).$

### 4.3 Differential Difference-DXCCII (DD-DXCCII)

This section describes a device termed as the differential difference dual-X current conveyor (DD-DXCCII) [95]. The DD-DXCCII is similar to the DXCCII with the only difference being that it has three input Y ports as found in the differential difference current conveyor (DDCC) [111]. The proposed symbol of the DD-DXCCII is shown in Fig. 4.3. The CMOS implementation of DD-DXCCII is shown in Fig. 4.4.

![Figure 4.3 Symbol of DD-DXCCII](image)

The DD-DXCCII can be characterized by the following matrix:

\[
\begin{bmatrix}
 I_{Y1} \\
 I_{Y2} \\
 I_{Y3} \\
 V_{XP} \\
 V_{XN} \\
 I_{Zp} \\
 I_{Zn}
\end{bmatrix} =
\begin{bmatrix}
 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 \\
 \beta_1 & -\beta_2 & \beta_2 & 0 & 0 \\
 -\beta_1 & \beta_2 & -\beta_3 & 0 & 0 \\
 0 & 0 & 0 & \alpha_p & 0 \\
 0 & 0 & 0 & 0 & \alpha_n
\end{bmatrix}
\begin{bmatrix}
 V_{Y1} \\
 V_{Y2} \\
 V_{Y3} \\
 I_{XP} \\
 I_{XN}
\end{bmatrix}
\]

(4.3)

Where $\beta_1$, $\beta_2$, and $\beta_3$ are the voltage transfer gain from port $Y_1$, $Y_2$ and $Y_3$ to port $X_p(X_n)$ respectively, while $\alpha_p(\alpha_n)$ are the current transfer gain from port X to port Z.
4.4 First-Order Current and Voltage-Mode Filters

This section describes two first-order filters. One operates as a CM multifunctional filter while the other operates as a VM all-pass filter.

**Realization of First-Order CM Multifunctional Filter:**

The proposed first-order CM filter section is shown in Fig. 4.5.

Analysis of the above circuit yields the following transfer functions:

\[
\frac{I_{LP}}{I_{IN}} = \frac{1/R_2C_1}{s + 1/R_1C_1} \quad (4.4)
\]

\[
\frac{I_{HP}}{I_{IN}} = \frac{sC_2/C_1}{s + 1/R_1C_1} \quad (4.5)
\]
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\[ I_{LP} = \frac{C_2 (s - 1/R_2 C_2)}{C_1 (s + 1/R_1 C_1)} \]  
\[ I_{IN} = \frac{1}{R_1 C_1} \]  \hspace{1cm} (4.6)

It needs to be mentioned that the analytical expressions in equations (4.4), (4.5) and (4.6) may also be obtained by the application of the computational approach presented in [112, 113]. The filter realizes CM low-pass, high-pass and all-pass sections as exhibited from equations (4.4), (4.5) and (4.6) respectively with the pole frequency as:

\[ \omega_0 = \frac{1}{R_1 C_1} \]  \hspace{1cm} (4.7)

The phase angle of the all-pass filter is computed as:

\[ \angle \phi = \pi - \arctan \frac{R_1 C_1 - \arctan R_2 C_2}{\omega} \]  \hspace{1cm} (4.8)

From equation (4.8), it is obvious that pole-\( \omega_0 \) sensitivities are unity in magnitude. Assuming \( R_1 = R_2 = R \) and \( C_1 = C_2 = C \), the expressions given in equations (4.4) through (4.6) simplify to:

\[ \frac{I_{LP}}{I_{IN}} = -\frac{1/R C}{(s + 1/R C)} \]  \hspace{1cm} (4.9)

\[ \frac{I_{HP}}{I_{IN}} = \frac{s}{(s + 1/R C)} \]  \hspace{1cm} (4.10)

\[ \frac{I_{AP}}{I_{IN}} = \frac{(s - 1/R C)}{(s + 1/R C)} \]  \hspace{1cm} (4.11)

\[ \omega_0 = \frac{1}{R C} \]  \hspace{1cm} (4.12)

\[ \angle \phi = \pi - 2\arctan \frac{1}{RC} \]  \hspace{1cm} (4.13)

It is to be noted that the CM filter is quite versatile and exhibits a low-pass, high-pass and an all-pass gain of unity in magnitude. The outputs are available at high-impedance nodes, which is a desirable feature for cascading applications. The assumption that \( R_1 = R_2 = R \) and \( C_1 = C_2 = C \) imposes matching conditions on the passive components and if not satisfied, may lead to phase and magnitude errors. For state-of-the-art integration processes, the tolerances attainable during the fabrication of resistors are in the range of 1 to 5%. Similarly, capacitors are also in the range of 5 to 10%. Therefore, it is clear that the matching conditions of equations (4.4-4.6) and (4.8) are not prohibitive.

**Non-Ideal Study**

Using the non-ideal port relations given in equation (4.2) and the transfer functions of the first-order low-pass, high-pass and all-pass filter sections given in (4.4), (4.5) and (4.6) respectively, the following non-ideal transfer functions can be obtained:

\[ \frac{I_{LP}}{I_{IN}} = -\alpha \beta \frac{1/C_2 R_2}{s + 1/C_2 R_2} \]  \hspace{1cm} (4.14)
Equations (4.14) through (4.16) reveal that the pole frequency remains unaltered even in the presence of device non-idealities for all realized filter functions.

**Parasitic Study**

The effect of device parasitics on the performance of the proposed circuits is also analyzed. For this purpose, the parasitic elements associated with the various ports of the DXCCII are identified. From the circuit depicted in Fig. 4.5, the external capacitor $C_1$ connected on the Y-port merges with the parasitic capacitor (~fF) and the effect of the parasitic Y-port resistance (~MΩ) can be neglected since it appears in parallel with the externally connected resistance $R_1$ at the Y-port. Similarly, the parasitic resistance appearing at the $X_n$ terminal may be neglected as it appears in series with a much higher externally connected resistance $R_2$. However, the same cannot be said for the parasitic resistance at the $X_P$ terminal since it appears in series with the capacitor $C_2$ and therefore results in undesired poles/zeros in the transfer functions. But, the inclusion of these poles/zeros will not affect the dominant pole frequency of the circuit and would only restrict the high frequency performance.

**Realization of Tunable VM First-Order All-Pass Filter**

The proposed tunable VM first-order filter is shown in Fig. 4.6. It employs a single DD-DXCCII, a single capacitor and an NMOS transistor operating in the triode region.

![Figure 4.6 Tunable first-order VM filter](image)

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The transfer function of an all-pass filter can be given as:

\[ T_{AP} = \frac{V_{OUT}}{V_{IN}} = \frac{s - 2/R_mC}{s + 2/R_mC} \quad (4.17) \]

Here, \( R_M \) is the resistance of the triode MOS transistor (M) of Fig. 4.6 and is given by\[94\].

\[ R_M = \left[ \mu_n C_{ox} \left( \frac{W}{L} \right) (V_C - V_T) \right]^{-1} \quad (4.18) \]

where \( \mu_n \), \( C_{ox} \), \( V_T \) and \( (W/L) \) are the MOS transistor parameters. From equation (4.17) the pole frequency \( \omega_0 \) can be expressed as:

\[ \omega_0 = \frac{2}{R_mC} \quad (4.19) \]

From equation (4.19) it is clear that the pole-frequency of the all-pass filter can be tuned by varying the resistance \( (R_M) \) of the triode MOS resistor (M). The phase angle of the all-pass filter can finally be expressed as:

\[ \angle \phi = \pi - 2 \tan^{-1} \left( \frac{\omega CR_M}{2} \right) \quad (4.20) \]

The delay of first order filter (i.e. negative derivative of the phase) can be expressed as:

\[ D(\omega) = -\frac{d\phi}{d\omega} = \frac{CR_M}{1 + \left( \frac{\omega CR_M}{2} \right)^2} \quad (4.21) \]

**Non-Ideal Study**

Considering the device non-idealities of DD-DXCCII as expressed in equation (4.3), the non-ideal transfer gain of the all-pass filter can be expressed as:

\[ T_{AP,n} = \frac{V_{OUT}}{V_{IN}} = \frac{s - 2\alpha_1 \beta_3}{s + 2\alpha_1 \beta_3} \quad (4.22) \]

From equation (4.22) the non-ideal pole frequency can be expressed as:

\[ \omega_{0,n} = \frac{2\alpha_1 \beta_3}{R_mC} \quad (4.23) \]

Equation (4.23) shows that due to non-ideal voltage and current transfer gain, the pole frequency does get affected.

**Parasitic Study**

The parasitics associated with the actual DD-DXCCII are the same as that of the DXCCII (expressed in Section 4.2). In Fig. 4.6, \( Y_1 \) and \( Z_5 \) port parasitics are in parallel i.e. \( R_{17}/R_{27}/C_{17}/C_{27} \), \( Y_3 \) and \( Z_8 \).
port resistances and capacitances are also in parallel i.e. $R_{Y1}/R_{Z1}/C_{Y1}/C_{Z1}$. The $X_P$ and $X_N$ parasitic i.e. $R_{XP}$ and $R_{XN}$ merge with the resistance of triode MOSFET. The proposed circuit is re-analyzed by taking into account the above parasitics (assuming $R_M >> (R_{XP}+R_{XN})$). The non-ideal transfer gain due to parasitics then becomes:

$$T_{AP,P} = \frac{V_{OUT}}{V_{IN}} = \left(\frac{C + C'}{C}\right)\left(\frac{s - 2/R_M(C + C')}{s + 2/R_M C}\right)$$

(4.24)

Where $C' = C_{Y1}/C_{Z1}$ and since $C >> C'$, the transfer function reduces to:

$$T_{AP,P} = \frac{V_{OUT}}{V_{IN}} = \left(\frac{s - 2/R_M C}{s + 2/R_M C}\right)$$

(4.25)

From equation (4.25) it is clear that the pole frequency is unaffected in the presence of parasitics.

**Comparative Study**

A comparison is made between the proposed circuit and the design reported in [114]. Both the circuits are composed of a single active device and a single passive component. In addition, the circuit presented in [114] uses only a single active element i.e. the DDCC and a single capacitor. However, its gain is reduced at $\omega = 0$ while in the proposed circuit, it remains constant. Another advantage of the proposed design is that even in the presence of parasitics, the filter pole frequency remains unaffected while it is not so in the case of the filter presented in [114]. Finally, tunability in [114] is achieved by applying two control voltages ($\pm V_C$) on two MOS transistors, while in the proposed circuit only one control voltage and one MOS transistor is needed.

**Design and Verification**

To verify the proposed theory, the first order filter section of Fig. 4.5 is designed for a pole frequency of $f_0 = 1.59$MHz. Taking $R_1 = R_2 = R = 10K\Omega$, equation (4.7) results in $C_1 = C_2 = C = 10pF$. The CMOS DX-MOCCII of Fig. 4.2 is used. The supply voltages are taken as $V_{DD} = -V_{SS} = 1.25V$ and $V_B = -0.3V$ [54]. The MOS transistor aspect ratios for the CMOS DX-MOCCII are given in Table 4.1. The observed low-pass and high-pass responses are shown in Fig. 4.7. The magnitude and phase responses of the all-pass filter section are shown in Fig. 4.8. The time domain response of the proposed all-pass filter shown in Fig. 4.9 is obtained by applying a sine wave with amplitude of 50$\mu$A at 1.59MHz. The output so obtained is 88.9º phase-shifted, which corresponds to the theoretical value of 90º. The THD of the all-pass filter section for a wide range of signal amplitudes is presented in Fig. 4.10 and is found to be around 1% for amplitude of 200 $\mu$A.
Table 4.1 MOSFET dimensions of the DX-MOCCII of Fig. 4.2

<table>
<thead>
<tr>
<th>MOS Transistors</th>
<th>W (µm)/ l(µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M₁, M₂, M₄, M₅, M₁₅, M₁₆, M₁₇, M₁₈</td>
<td>2/0.25</td>
</tr>
<tr>
<td>M₁₉, M₂₈, M₂₂, M₂₄</td>
<td></td>
</tr>
<tr>
<td>M₃, M₆, M₇, M₈, M₉, M₁₀</td>
<td>4/0.25</td>
</tr>
<tr>
<td>M₁₁, M₁₂, M₁₃, M₁₄, M₁₅, M₂₁</td>
<td>16/0.25</td>
</tr>
</tbody>
</table>

Figure 4.7. Frequency response of low-pass and high-pass filter sections

Figure 4.8. Phase and gain plot of all-pass response of Fig. 4.5
Experimental Verification of First-Order Filter Section

The performance of the proposed multi-functional filter is further tested by a hardware implementation of the circuit. Commercially available CFOAs (AD844s) is used to emulate the DXCCIIIs. As shown in Fig. 4.11, four AD844 chips and two discrete resistances are connected to yield a DXCCII. The realized DXCCIIIs are then used to set up the circuits of the proposed low-pass, high-pass and all-pass filters with $C_1 = C_2 = 1\text{nF}$ and $R_1 = R_2 = 4.7 \text{K}\Omega$ which correspond to a pole frequency of 33.86 KHz. The biasing supplies are kept at ±10 Volts.

The experimental results obtained for the different filter functions are shown in Fig. 4.12. The pole frequency obtained during experimental verification is 31 kHz which is within 8% of the designed value of 33.86 KHz. Further, time domain waveforms of the output of the AP filter are presented in Fig. 4.13 with a 90° phase difference between the input and output signal waveforms. It may be mentioned that although the proposed circuit has CM outputs, the experimental results shown in Fig. 4.13 are VM counterparts ($V_{in}, V_{out}$) of the actual CM signals ($I_{in}, I_{AP}$). This is done to facilitate display of the signal waveforms on an oscilloscope. The presence of phase quadrature between the input and output waveforms is shown as an XY plot. The measured frequency at this point is 31 kHz which is close to the designed value of 33.86 KHz. The deviations of the measured pole-frequency from the designed
frequency may be attributed to the parasitics associated with the AD844. More specifically, the parasitic resistance appearing at the $X_P$ terminal of the DXCCII implemented using AD844 (~50Ω) causes deterioration of the high frequency response.

![Diagram of DXCCII using AD844](image)

**Figure 4.11.** Realization of DXCCII using AD844

![Graph comparing theoretical and experimental results](image)

**Figure 4.12** Comparison of theoretical and experimental results for HP, LP and AP responses

![Experimental quadrature waveforms](image)

**Figure 4.13** Experimental quadrature waveforms for AP filter section and X-Y of two voltage outputs
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It may further be mentioned that although the experimental results are given for signals in the KHz range, the proposed circuit itself is capable of satisfactory operation at much higher frequencies. The restriction on the operating frequencies exists due to the non-availability of CMOS DXCCIIIs in an integrated form. Therefore, the upper limit of operating frequencies, in this case, is governed by the characteristics of the AD844 and should not be an issue if a dedicated CMOS DXCCII becomes available.

The proposed circuit of Fig. 4.6 realizes a first-order all-pass filter at different pole frequencies. Aspect ratios of the MOS transistors are given in Table 4.2 with the DC-biasing levels as $V_{DD} = -V_{SS} = 1.25$V and $V_B = -0.3$V [54]. The dimensions of the NMOS transistors $M$ in the proposed filter is selected by fixing $(W/L) = (0.5 \mu m/0.25 \mu m)$. Selecting $C = 0.05$ nF and $R_M = 1.5\Omega$, $2\Omega$, $3\Omega$ at different control voltages $V_c = 2.1$V, $1.55$V and $1.08$V results in a theoretical pole-frequency of $f_o = 4.2$ MHz, $3.1$MHz and $2.1$MHz respectively. The observed pole-frequencies are found to be $4.1$MHz, $3$MHz and $2$MHz.

The phase and gain plots for various gate voltages of transistor $M$ are shown in Fig. 4.14. The phase is found to vary from 0 to 180° with a value of 90° at the pole frequency. The time domain response is shown in Fig. 4.15 which is obtained by applying a sinusoidal signal of 50mV peak amplitude at 3 MHz. The output is found to be shifted 90° from the input. The THD is found to be 1.6% for peak-to-peak amplitude of 100mV at 3MHz. The variation of the THD at the pole frequency of 3MHz is shown in Fig. 4.16 which verifies that the THD values are below 3% for sinusoidal input of up to 300mV peak-to-peak.

<table>
<thead>
<tr>
<th>MOS Transistors</th>
<th>W (μm) / l(μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$, $M_3$, $M_7$, $M_5$, $M_{15}$, $M_{16}$, $M_{17}$, $M_{18}$, $M_{20}$</td>
<td>2 / 0.25</td>
</tr>
<tr>
<td>$M_4$, $M_6$, $M_8$, $M_9$, $M_{10}$</td>
<td>4 / 0.25</td>
</tr>
<tr>
<td>$M_{11}$, $M_{12}$, $M_{13}$, $M_{14}$</td>
<td>16 / 0.25</td>
</tr>
<tr>
<td>$M_{21}$, $M_{22}$, $M_{23}$, $M_{24}$</td>
<td>1 / 0.25</td>
</tr>
<tr>
<td>$M_{25}$, $M_{26}$, $M_{27}$</td>
<td>5 / 0.25</td>
</tr>
<tr>
<td>$M_{28}$, $M_{29}$, $M_{30}$</td>
<td>3 / 0.25</td>
</tr>
</tbody>
</table>
4.5 Cascadable Current-Mode Universal Filter

The proposed cascadable second-order CM universal filter is shown in Fig. 4.17 and employs a single DD-DXCCII and a DXCCII, two grounded resistors, two grounded capacitors and a single MOSFET operating in the triode region. It also provides band-pass and low-pass outputs in transresistance-mode simultaneously along with CM outputs without the need of additional components. All the components are grounded which is ideal for IC implementation.
Figure 4.17. Second order current-and transresistance-mode filter

Analysis of the proposed filter yields the following transfer functions:

\[
\begin{align*}
\frac{i_{01}}{i_{in}} &= \frac{s/C_1 R_1}{D(s)} \\
\frac{i_{02}}{i_{in}} &= -\frac{s^2}{D(s)} \\
\frac{i_{03}}{i_{in}} &= \frac{2/C_1 C_2 R_1 R_M}{D(s)} \\
\frac{i_{04}}{i_{in}} &= -\frac{2/C_1 C_2 R_1 R_M}{D(s)} \\
\frac{v_{01}}{i_{in}} &= \frac{s/C_1}{D(s)} \\
\frac{v_{02}}{i_{in}} &= \frac{1/C_1 C_2 R_1}{D(s)}
\end{align*}
\]

where \[D(s) = s^2 + \frac{s}{C_1 R_2} + \frac{1}{C_1 C_2 R_1 R_2}\] (4.32)

Thus the filter realizes CM band-pass, high-pass, low-pass and inverting low-pass functions as exhibited from equations (4.26) to (4.29) respectively. The inverting all-pass filter function is obtained by adding \(I_{01}, I_{02}\) and \(I_{04}\); and an inverting notch filter response is obtained by adding \(I_{02}\) and \(I_{04}\). Equation (4.30) and (4.31) shows that in addition to the CM outputs, the transresistance mode low-pass and band-pass responses are also simultaneously obtained without the need of external passive components. Equation (4.26) to (4.32) can be used to derive the gain constants \(H_{HF}, H_{BP}, H_{LP1}, H_{LP2}\) and \(K_{HF}, K_{LP}\) for the current- and transresistance-mode respectively as:

\[
\begin{align*}
H_{HF} &= -1, \quad H_{BP} = \frac{R_2}{R_1}, \quad H_{LP1} = \frac{2R_2}{R_M}, \quad H_{LP2} = -\frac{2R_2}{R_M} \\
K_{LP} &= R_2, \quad K_{BP} = R_2
\end{align*}
\]

(4.33)

(4.34)

From equation (4.32) the pole-frequency \(\omega_p\) and pole-Q can be expressed as:
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\[ \omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_2}} \]  
\[ Q = \sqrt{\frac{C_1R_2}{C_2R_1}} \]  

Non-Ideal Analysis

To account for the non-idealities associated with an actual DD-DXCCII, from equation (4.3), it is clear that two parameters are introduced i.e. \( \alpha_k \) and \( \beta_i \) \((k = p, n \text{ and } i = j = 1, 2)\), where \( \alpha_k \) and \( \alpha_i \) are current-transfer gains from port-\( X_p \) to port-\( Z_p \) and port-\( X_n \) to port-\( Z_n \) respectively. Parameters \( \beta_k \) and \( \beta_i \) are the voltage-transfer gains from \( V_i \) to \( X_p \) and \( V_2 \) to \( X_p \) respectively. The modified non-ideal transfer gain in current- and transimpedance-mode can be expressed as:

\[ \frac{I_{g1}(s)}{I_{IN}(s)} = \frac{s}{\frac{C_1R_2\alpha_{n1}}{D_n(s)}} \]  
\[ \frac{I_{g2}(s)}{I_{IN}(s)} = -\frac{s^2}{D_n(s)} \]  
\[ \frac{I_{g3}(s)}{I_{IN}(s)} = \frac{2\alpha_p\alpha_{p2}\beta_{12}}{C_1C_2R_1R_M} \]  

where

\[ D(s) = s^2 + \frac{s}{C_1R_2\alpha_{n1}\beta_{11}} + \frac{\alpha_p\beta_{21}}{C_1C_2R_1R_2\alpha_{n2}\beta_{11}} \]

From equations (4.37) to (4.42) the pole frequency and pole-Q are obtained as:

\[ \omega_{0,n} = \sqrt{\frac{\alpha_p\beta_{21}}{C_1C_2R_1R_2\alpha_{n1}\beta_{11}}} \]  
\[ Q_n = \sqrt{\frac{\alpha_{n1}\alpha_p\beta_{11}\beta_{21}\alpha_{p2}}{C_2R_1}} \]

From equations (4.43) and (4.44) it is evident that the non-ideal values of \( \omega_{0,n} \) and \( Q_n \) will not deviate significantly from their ideal values depicted in equations (4.35) and (4.36), assuming that \( \alpha_p, \alpha_{n1}, \beta_{11}, \beta_{21} \) are close to unity. Further, it can be also be deduced that all passive sensitivities of \( \omega_{0,n} \) and \( Q_n \) are not more than unity in magnitude.
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Design and Verification

To verify the proposed theory, the second-order CM multifunctional filter of Fig. 4.17 was designed for a pole frequency of $f_0 = 1.58$ MHz and pole-Q = 1. Taking $R_1 = R_2 = 10k\Omega$, equation (4.32) results in $C_1 = C_2 = 10pF$. The supply voltages are taken as $V_{DD} = -V_{SS} = 1.25V$ and $V_B = -0.3V$ [54]. In order to set the low-pass to be unity, the aspect ratio of the triode MOSFET is taken to be $W/L = 0.25\mu m/0.35\mu m$ and the gate voltage is kept at 1.2V (At these values, low-pass gain expressed in equation (4.33) is equal to unity). The frequency response of band-pass, high-pass and low-pass section is shown in Fig. 4.18. The simulated frequency is found to be 1.57 MHz. The gain and phase plot of the inverting all-pass filter are shown in Fig. 4.19. By adding a high-pass and a low-pass output, an inverting notch response is obtained as shown in Fig. 4.20. To test the time-domain response of the proposed filter, a sinusoidal input current with 100 $\mu$A peak-to-peak amplitude and frequency of 1.57 MHz is applied to the filter. The BP response of the output is shown in Fig. 4.21 which is obtained by applying a 100 $\mu$A (peak-to-peak) sinusoidal input current at 1.57 MHz. As expected, a zero phase difference appears between input and output signals while their amplitudes are equal. In transresistance mode, the simulated responses for band-pass and low-pass are depicted in Fig. 4.22.

![Figure 4.18 Simulated gain responses of CM multifunctional filter](image1)

![Figure 4.19. Gain and phase plot of CM multifunctional filter](image2)
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Figure 4.20. Simulated gain response of notch CM multifunctional filter

Figure 4.21. The input and output waveforms of the BP response for an 100 μA (peak-to-peak) sinusoidal input current at 1.57 MHz.

Figure 4.22. Band-pass and low-pass response in Transresistance-mode

Tunable $n^{th}$-order Voltage-Mode All-Pass Filter

It is well known that higher-order filters exhibit a larger rate of phase change at constant magnitude when compared to a first-order filter [5]. They can also be used as a group delay equalizer in video and communication applications. These features are the motivating factor behind realizing higher-order filters in this work. The proposed $n^{th}$-order all-pass filter is presented in Fig. 4.23, which is obtained by cascading $n$-stages of the first-order filter described in Section 4.4. The proposed filter employs $n$-stages of DD-DXCCII and $n$-capacitors, voltage buffers and MOS resistors operating in the triode region.

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Figure 4.23. Tunable $n^{th}$ order all-pass filter

Analysis of the above circuit yields the following transfer function

$$T_{AP}(s) = \frac{V_{OUT}}{V_{IN}} = \frac{(s - 2/R_{M1}C_1)(s - 2/R_{M2}C_2)(s - 2/R_{M3}C_3) \cdots (s - 2/R_{Mn}C_n)}{(s + 2/R_{M1}C_1)(s + 2/R_{M2}C_2)(s + 2/R_{M3}C_3) \cdots (s + 2/R_{Mn}C_n)} \quad (4.45)$$

From equation (4.45) the pole frequency $\omega_0$ can be expressed as:

$$\omega_0(n) = \frac{2^n}{(R_{M1}, R_{M2} \ldots R_{Mn}, C_{M1}, C_{M2} \ldots C_{Mn})^{\frac{1}{2}}n} \quad (4.46)$$

**Design and Verification**

A third-order all-pass filter is also designed by taking $n = 3$. The phase and gain plot of the tunable third-order filter is shown in Fig. 4.24 from which the phase is found to vary from 180° to −360° with a value of −90° at the pole frequency. The dimensions of the NMOS transistors $M_i$ in the proposed filter is fixed at $(W/L)_i = (0.5 \, \mu m/0.25 \, \mu m)$ where $i=1,2,3$. Selecting $R_{M1} = 1.5 \, k\Omega$, $2 \, k\Omega$, $3 \, k\Omega$ at $V_{ds} = 2.1V$, $1.55V$, $1.08V$ and $C_1 = C_2 = C_3 = 0.05 \, nF$ results in a theoretical pole-frequency of $f_p = 4.2 \, MHz$, $3.1 \, MHz$ and $2.1 \, MHz$ respectively. The frequency values obtained through simulation are $4.1 \, MHz$, $3.0 \, MHz$ and $2.0 \, MHz$. The phase and group delay response of the first- and third-order filter at $R_{M1} = 3 \, k\Omega$ and $C_1 = C_2 = C_3 = 0.05 \, nF$ are shown in Fig. 4.25 and Fig. 4.26 respectively. The phase curve shows the variation of phase from 180° to 0° for the first-order filter and 180° to −360° for the third-order filter. The group delay of the first-order and the third-order filter is 8.7µs and 26.1µs (three times that of the first order filter) respectively. This clearly shows that the group-delay increases with the order of the filter.
4.6 Voltage and Current-Mode Sinusoidal Oscillators

This section proposes three sinusoidal oscillators. The first two oscillators (which are second-order oscillators) are designed to operate in CM and VM with one of them generating four phases and the other generating three phases simultaneously. The third oscillator is a third-order mixed-mode three phase oscillator capable of generating voltage and current sinusoidal output signals.
**Four-Phase Sinusoidal Oscillator Realization**

The CM first-order filter section of Fig. 4.5 is used to realize a CM four-phase sinusoidal oscillator by cascading the all-pass output with DX-MOCCII based non-inverting current mode integrator as shown in Fig. 4.27.

![Figure 4.27. The DX-MOCCII based CM-FPSO circuit](image)

Fig. 4.27 yields the characteristic equation of the proposed oscillator as

\[ s^2 + s \left( \frac{1}{R_1C_1} - \frac{1}{R_3C_3} \right) + \frac{1}{R_2R_3C_2C_3} = 0 \]  \hspace{1cm} (4.47)

which results in the condition of oscillation (CO) as:

\[ R_1C_1 \geq R_3C_3 \]  \hspace{1cm} (4.48)

and the frequency of oscillation (FO) as:

\[ \omega_0 = \sqrt{\frac{1}{R_2R_3C_2C_3}} \]  \hspace{1cm} (4.49)

From equations (4.48) and (4.49) it is clear that the frequency of the oscillation is independently controlled by varying \( R_2 \) and/or \( C_2 \). The proposed oscillator includes six passive components and the DX-MOCCII requires four output stages (two \( Z_n \) and two \( Z_p \)). To reduce the number of passive components and the number of output stages within the DX-MOCCII, a modification of the original circuit is proposed as shown in Fig. 4.28. It can be noted that a MOSFET M operating in the triode region replaces a passive resistor \( R_3 \). The characteristic equation of the oscillator can be obtained through analysis:
where \( g_m \) is the transconductance of the MOS transistor \( M \) of Fig. 4.28 and is given by [94]:

\[
g_m = \mu_n C_{ox} \frac{W}{L} (V_g - V_T)
\]

which results in the following CO:

\[
2g_m \geq \frac{C_3}{R_1C_2}
\]

The FO may be given by:

\[
\omega_0 = \sqrt{\frac{2g_m}{R_2C_1C_3}}
\]

From equation (4.52) and (4.53), it is clear that \( C_1 \) and/or \( R_2 \) provides independent control of the frequency of oscillation without disturbing the condition of oscillation. From Fig. 4.28 the four current outputs of the CM-FPSO at the oscillating frequency can be expressed as:

\[
I_{o1} = -\frac{\pi}{4}I_{o3}, \quad I_{o2} = -\frac{3\pi}{4}I_{o3}, \quad I_{o4} = \frac{\pi}{2}I_{o3}
\]

Design and Verification

The realized four-phase sinusoidal oscillator of Fig. 4.28 was designed for an oscillating frequency of \( f_0 = 1.74 \text{MHz} \). Taking \( R_1 = R_2 = R = 6 \Omega \), and \( C_1 = C_2 = C_3 = C \) equation (4.53) results in \( C = 20 \text{ pF} \). It is to be noted that the oscillations were set by trimming the resistor \( R \). The observed wave-shapes of CM-FPSO are as shown in Fig. 4.29. The THD was measured to be 3.5% which is a low value.
THD variation with frequency is presented in Fig. 4.30. It may be observed that the THD remains low for frequencies of up to 10 MHz, beyond which it tends to increase. Assuming $C_1 = C_3 = C$, the variation in the frequency of oscillation by varying $C$ is shown in Fig. 4.31, which illustrates independent frequency control. Next, current outputs of the designed CM-FPSO were loaded with a same valued resistor $R_L = 1K\Omega$ and the resulting wave-shapes of the VM-FPSO are shown in Fig. 4.32. Figure 4.29 and 4.32 shows some deviation in magnitudes due to the effect of non-ideal transfer gains.

![Wave-shapes of the designed CM-FPSO](image1)

*Figure 4.29. Wave-shapes of the designed CM-FPSO*

![THD variation of the output of the CM-FPSO for different oscillation frequency](image2)

*Figure 4.30. THD variation of the output of the CM-FPSO for different oscillation frequency*
Comparative Study

The proposed circuit is compared with similar reported circuits based on the use of active/passive components and types of responses obtained. This comparison is listed in Table 4.3. It may be noted that most of the available circuits operate at low frequencies [82-89]. In addition, most of the circuits provide only an all-pass response [82, 84-89]. In contrast, the proposed circuit exhibits high frequency operation, multiple responses (low-pass, high-pass and all-pass), minimum grounded passive components, minimum active devices and a multi-phase oscillatory feature.
Table 4.3: Comparison of proposed and existing circuits

<table>
<thead>
<tr>
<th>Ref. no.</th>
<th>Filter Responses</th>
<th>Oscillator</th>
<th>Filter pole/Oscillator Frequency ($f_o$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[29] 1-CDBA N N Y 2 1 1 N - - - - 1.59-MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[82] 1-CCII N N Y 4 2 - N - - - - 159.2-KHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[85] 1-CCIII N N Y 2 1 1 Y 2-CCOA 6 2 2 155-KHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[87] 1-CCII N N Y 1 - 1 N - - - - 100-KHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[86] 2-CDTA N N Y 1 - - N - - - - 153-KHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[88] 1-CCIII N N Y 2 1 1 Y 2-CCII 6 2 1 159-KHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[84] 2-CCII N N Y 4 1 1 Y 3-CCII 6 - - - 5-KHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[89] 2-MOCCI Y Y Y 2 - - Y 4-MOCCI 4 - - - 358-KHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Proposed Circuit 1-DXCCII Y Y Y 4 - - Y 2-DXCCII, MOS 5 - - 1.59-MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**ANALOG SIGNAL PROCESSING MODULES USING DXCCII**

**DD-DXCC Based Current- and Voltage-Mode Three-Phase Oscillator**

In this section a CM and VM three-phase sinusoidal oscillator is presented by providing a direct feedback from the non-inverting band-pass output to the input. This oscillator is derived from the second-order current-and transadmittance-mode filter of Fig. 4.17. Fig 4.33 presents a DD-DXCCII and DXCCII-based oscillator employing only grounded passive components.

![Figure 4.33. Proposed CM and VM three phase oscillator](image)

Analysis of the proposed oscillator circuit yields the following characteristic equation:

\[ s^2 + s \left( \frac{1}{C_1 R_2} - \frac{1}{R_1} \right) + \frac{1}{R_1 R_2 C_1 C_2} = 0 \]  \hspace{1cm} (4.55)

which results in the following CO:

\[ CO: \quad R_2 \geq R_1 \]  \hspace{1cm} (4.56)

The FO may be given as:

\[ FO: \quad \omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \]  \hspace{1cm} (4.57)

From equation (4.56) and (4.57) it is clear that \( C_1, C_2 \) provides independent control of the frequency of oscillation without disturbing the condition of oscillation. Assuming \( R_1 = R_2 = R \) and \( C_1 = C_2 = C \), the FO simplifies to:

\[ FO: \quad \omega_o = \frac{1}{RC} \]  \hspace{1cm} (4.58)

From Fig. 4.33 the three current outputs and voltage outputs at the oscillating frequency can be expressed as:

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\[ I_{02} = -\frac{\pi}{2} I_{01}, \quad I_{03} = -\frac{\pi}{2} I_{01} \]

\[ V_{04} = -\pi V_{01}, \quad V_{02} = -\frac{\pi}{2} V_{01} \]

(4.59)

It may be pointed out that the DXCCII shown in Fig. 4.33 is needed only when I_{03} is required and can be avoided only if current outputs in phase quadrature are needed and which are available at I_{01} and I_{02}.

**Design and Verification**

The realized three-phase oscillator of Fig. 4.33 is designed with \( C_1 = C_2 = C = 30 \, \text{pF} \) and \( R_1 = R_2 = 10 \, \text{K}\Omega \). The frequency of oscillation obtained from equation (4.58) is \( f_0 = 530 \, \text{KHz} \), whereas the simulated oscillation frequency is found to be \( f_0 = 512 \, \text{KHz} \). For this purpose, passive element values are taken as \( C_1 = C_2 = C = 30 \, \text{pF}, \, R_1 = 10 \, \text{K}\Omega \) and \( R_2 = 10.59 \, \text{K}\Omega \). It is to be noted that \( R_2 \) is chosen to be slightly greater than \( R_1 \) to bring the poles to the right half of the S-plane in order to build up oscillation which are sustained by the circuit. The simulated CM and VM wave-shapes are shown in Fig. 4.34 and 4.35 respectively. At the oscillating frequency THD is found to be 2%. The oscillator is then tuned by varying the capacitance \( C \) and the variation in the oscillation is shown in Fig. 4.36.

Figure 4.34. Simulated output wave-shapes of the CM for the three phase oscillator

Figure 4.35. Simulated output wave-shapes of the VM for the three phase oscillator
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![Graph](image)

**Figure 4.36. Frequency tuning of three phase oscillator with C**

**DXCCII Based Mixed-Mode Three-Phase Oscillator**

This section presents the design of a mixed-mode three phase sinusoidal oscillator (MTSO) as depicted in Fig. 4.37. The basic building blocks of the MTSO are two lossy integrators and an inverting lossless integrator. Each of these sections is realized using a single DXCCII, a grounded resistor, grounded capacitors along with a MOSFET biased in the triode region (acting as a resistor). The value of the transconductance obtained for the triode MOSFETs in Fig. 4.37 is given by \[94\].

![Diagram](image)

**Figure 4.37. Proposed DXCCII based mixed-mode multiphase oscillator**

The characteristic equations for the third-order oscillator shown in Fig. 4.37 is given by:

\[
s^3 + s^2 \left( \frac{1}{C_1R_1} + \frac{1}{R_2C_2} \right) + \frac{s}{R_1 R_2 C_1 C_2} + \frac{8g_{m1}g_{m2}g_{m3}}{C_1 C_2 C_3} = 0
\]

(4.60)

from which the frequency of oscillation (FO) and condition of oscillation (CO) may be obtained as:

\[
\text{FO: } \omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}
\]

(4.61)

\[
\text{CO: } 8g_{m1}g_{m2}g_{m3}R_1 R_2 \geq \frac{(C_1 R_1 + R_2 C_2)}{R_1 R_2 C_1 C_2} C_3
\]

(4.62)
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Assuming equal valued resistors ($R_1 = R_2 = R$) and capacitors ($C_1 = C_2 = C_3 = C$), the expression in (4.61) to (4.62) simplify to:

$$F_O: \omega_o = \frac{1}{RC}$$  \hspace{1cm} (4.63)

$$C_O: R = \frac{3}{\sqrt{4g_{m1}g_{m2}g_{m3}}}$$  \hspace{1cm} (4.64)

The two lossy integrators will introduce a phase shift of ($\pi/2$) each and the inverting lossless integrator will further provide a phase shift of ($3\pi/2$) thereby making the total phase around the feedback loop to be equal to ($2\pi$). This is in compliance with the standard Barkhausen criterion for oscillation.

**Design and Verification**

The proposed mixed-mode sinusoidal oscillator is simulated by setting $V_{DD} = -V_{SS} = 1.25V$ and $V_B = -0.3V$ [54]. The values of the passive elements are kept as $C_1 = C_2 = 90pF$ and $R_1 = R_2 = 1K\Omega$ resulting in a designed theoretical frequency of 1.76 MHz. To fulfill the condition of oscillation, as given in equation (4.64), the aspect ratios of the triode MOSFETs (M1 to M3) are $W_1/L_1= W_2/L_2 = W_3/L_3 = 1.25\mu m/0.25\mu m$ and the gate voltages are kept at 1.1 V. The frequency of oscillation thus obtained is found to be 1.7 MHz (which is very close to the designed value of 1.76 MHz) and the obtained three-phase voltage and current waveforms are shown in Fig. 4.38 and 4.39 respectively. The difference in amplitude is due to the presence of lossy integrators. The variation in frequency with the value of capacitance is also explored. It is evident from Fig. 4.40 that the variation in frequency of oscillator with $C_2 = C_3 = C_1$ is in accordance with equation (4.63). The performance of the proposed oscillator is analysed by plotting the THD for the generated outputs as depicted in Fig. 4.41. It can be observed that for the proposed oscillator, the THD remains within 5% for an operating frequency of up to 6MHz.

![Figure 4.38. Simulated three phase voltage outputs](image)
4.7 Conclusion

A versatile CM first-order filter section employing DX-MOCCII, two grounded resistors and two grounded capacitors is initially proposed in this Chapter. This filter section is then utilized to realize a programmable CM four-phase sinusoidal oscillator. The CM oscillator outputs are loaded with equal...
valued resistors to realize VM four-phase sinusoidal outputs. All the realizations use grounded capacitors and resistors and are hence suited for monolithic implementation.

Hardware implementation of the proposed filter structure given in Fig. 4.5 is also carried out using AD844s. Theoretical and experimental results are found to be in agreement thereby ascertaining the feasibility of the proposed work. A comparative analysis (Table 4.3) proves the superiority of the proposed circuit with similar reported designs.

Next, a tunable VM first-order filter of Fig. 4.6 is realized using a single active element and one passive component. The all-pass gain of the designed filter remains constant over a wide range of frequencies (10KHz-100MHz). Another notable feature of this filter is that it can be used for the design of a filter of any order by cascading in stages. Tunability of pole-frequency as a feature is also supported in this filter.

Lastly, a cascadable second-order universal CM biquadratic filter is realized. The features of this circuit are: (i) minimum active elements, (ii) all passive components are grounded, (iii) transresistance mode band-pass and low-pass responses are obtained without the need of external passive components, and (iv) presence of high output impedance offers easy cascadability which is useful in realizing higher order filters. The same filter section is utilized to realize a CM and VM three-phase oscillator without the need of additional components.

The filters designed in this Chapter lack digital tunability. Designs based on building blocks that support these features are discussed in the next Chapter.