CHAPTER 2
ANALOG SIGNAL PROCESSING MODULES USING CCII

In this chapter, a novel first-order multi-output current-mode (CM) filter and a second-order voltage-mode (VM) bi-quadratic filter are realized using CCII as the active device (basic building block). The all-pass section of the first-order filter is utilized to design a CM multiphase oscillator. Next, a bi-phase amplifier is designed, which in turn, is used to realize a precision rectifier.

The design presented in this chapter realizes a CM first-order and a VM second-order filter. The CM first-order filter provides load-insensitive low-pass (LP), high-pass (HP), and all-pass (AP) outputs simultaneously with a single current input. The versatile filter section employs only one grounded resistor, one grounded capacitor and two multi-output second generation current conveyors (MOCCIIs). The second-order VM multifunctional filter employs one current feedback operational amplifier (CFOA), two resistors, two capacitors and one buffer. The circuit realizes low-pass (LP), high-pass (HP), band-pass (BP), band-reject (BR) responses. The circuit also exhibits two output responses (HP and BP) simultaneously. The other two responses (LP and BR) can be selected with the help of a switch.

Towards the end of this Chapter a bi-phase amplifier is proposed which acts as a prime building block for a precision rectifier.

All simulations are performed using PSPICE and model parameters were obtained from the MIETEC 0.5 μm CMOS process [16]

2.1 Introduction

Current conveyors have become very popular since they offer higher performance and greater functional versatility when used as analog building blocks [17-31]. Several first-order VM all-pass sections (APSs) using current conveyors have been presented in technical literature [17, 21, 22, 31]. However, CM circuits are also receiving much attention due to their inherent advantages (see Section 1.3, Chapter 1) [19, 27-29]. Consequently, several first-order all-pass filters using different active components have been reported recently [25, 29]. Among these topologies, some require element-matching conditions even with
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a minimum component count [32] while others require a larger component count and complex circuitry [33].

In this Chapter, a CM versatile first-order filter section is realized which provides load insensitive low-pass, high-pass and all-pass outputs with a single current input. The versatile filter section uses only one grounded resistor and one grounded capacitor along with two multi-output second generation current conveyors (MOCCIIs). The all-pass section is then utilized to realize a CM eight-phase sinusoidal oscillator (CM-EPSO). The CM-EPSO current outputs are loaded with a resistor to realize a VM eight-phase sinusoidal oscillator (VM-EPSO). Sinusoidal oscillators find wide applications in communication, instrumentation and control system, for instance, as quadrature mixer and single side band generators, or for measurement purposes in vector generators and selective voltmeters.

Next, a new bi quadratic multifunctional filter is simulated and a hardware setup realized based on CCII+. Within the hardware design, the CCII+ is realized by using the AD844 chip which is a current feedback operational amplifier (CFOA). The CFOA has already been proven to be a functionally flexible and versatile building block. It possesses a higher bandwidth, high slew rate, greater linearity and dynamic range. In addition, it has a low impedance output which makes the circuit cascadable without the need of an additional buffer. As a result, it is gaining wider acceptance as a basic building block for designing voltage/current-mode signal processing circuits [34-39]. The realized filter offers features such as a low component count, muti-output bi-quadratic responses under a single input and low sensitivity figures. The filter is simulated as well as its behaviour is experimentally verified.

Precision rectifiers are important building blocks used in non-linear analog processing systems. In such rectifiers, the threshold voltage associated with silicon diodes is overcome and hence rectification is possible at relatively low signal levels. Precision rectifiers are important building blocks for a number of signal processing applications such as RMS to DC convertors in instrumentation and peak to floor detectors in ultrasonics [40]. Predictably, many precision rectifiers using current conveyors have been recently reported in literature [27, 35, 41-54]. Current conveyor-based precision rectifiers offer a number of advantages over other devices. However, many of them employ complex circuitry [41, 45-47].

A precision rectifier using a bi-phase amplifier is also discussed in this Chapter. The bi-phase amplifier is, in turn, based on a second-generation current conveyor (CCII+). The bi-phase mode of the amplifier is controlled with the help of an additional voltage controlled switch and a comparator to achieve half-wave and full-wave rectification. The realized precision rectifier has a simpler hardware and a wider operating frequency range.
2.2 Second Generation Current Conveyor (CCII)

The second-generation current conveyor (CCII) is one of the most functionally flexible and versatile analog building blocks [55]. Since its first introduction, by A. Sedra and K. Smith in 1970 [37], it has been used in high frequency analog signal applications such as filters [17] and CM oscillators [56]. The CCII is a three-terminal device whose properties are governed by the following equation:

\[ I_y = 0 \quad V_x = V_y, \quad I_z = \pm I_x \]  

(2.1)

Its symbol is shown in Fig. 2.1.

![Figure 2.1. The symbol of CCII](image)

The device comprises a low-impedance current input/voltage output terminal \( X \), a high-impedance voltage input terminal \( Y \) and a current output terminal \( Z \). The current supplied to \( X \) is conveyed to the output terminal \( Z \) with either a positive polarity (in CCII+) or a negative polarity (in CCII−). By convention, positive is taken to mean that both \( I_X \) and \( I_Z \) are flowing simultaneously towards or away from the conveyor [16]. The CMOS implementation of the MOCCII is given in Fig. 2.2.

![Figure 2.2. The CMOS structure of the MOCCII](image)
2.3 First-Order Current-Mode Filter

The filter realized in this section uses only a single grounded resistor and a capacitor along with two multi-output second generation current conveyors (MOCCII), as shown in Fig. 2.3.

![Figure 2.3 The versatile first order filter](image)

The transfer function of the proposed filter can be given by:

\[
\frac{I_{LP}}{I_{in}} = \frac{1/RC}{s + 1/RC} \quad (2.2)
\]

\[
\frac{I_{HP}}{I_{in}} = \frac{s}{s + 1/RC} \quad (2.3)
\]

\[
\frac{I_{AP}}{I_{in}} = \frac{s - 1/RC}{s + 1/RC} \quad (2.4)
\]

The filter thus realizes CM low-pass, high-pass and all-pass functions with a pole frequency of:

\[
\omega_0 = \frac{1}{RC} \quad (2.5)
\]

It can be noted that the versatile CM filter has a LP, HP and AP gain that are unity in magnitude. The outputs are available at high impedance terminals, which is desirable for cascading applications.

**Non-Ideal Analysis:**

The analysis shown above contains the transfer functions and related circuit parameters derived assuming that all the analog building blocks are ideal in nature with unity voltage and current gains. However, an actual implementation of any analog building block is bound to have non-idealities associated with it in the form of voltage and current gain deviating from an ideal value. This
necessitates re-analysis of the circuit in the presence of non-ideal behaviour and is discussed in the following paragraph.

Taking the non-idealities of the CCIIs into account, the relationship given in equation (2.1) can be modified as:

\[ V_x = \beta V_y, \quad i_y = 0 \quad \text{and} \quad i_x = \pm \alpha i_x \]  \hspace{1cm} (2.6)

where the voltage transfer gains \( \beta \) from \( Y \) to \( X \) deviate from unity by an amount equal to voltage transfer errors. Similarly, the current transfer gains \( \alpha \) from \( X \) to \( Z \) deviate from unity by the current transfer errors. These errors are expected to be quite low for an integrated CCII, thus making voltage and current transfer gains approach unity at the operating frequency value. With these non-idealities in consideration, equations (2.2) to (2.4) are modified to:

\[
\begin{align*}
\frac{I_{LP}}{I_{in}} &= \frac{\alpha_1 \beta_1}{\alpha_2 \beta_2 RC} \frac{D(s)}{D(s)} \\
\frac{I_{HP}}{I_{in}} &= \frac{s}{D(s)} \\
\frac{I_{AP}}{I_{in}} &= \frac{s - \alpha_1 \beta_1}{\alpha_2 \beta_2 RC} \frac{D(s)}{D(s)}
\end{align*}
\]  \hspace{1cm} (2.7) \hspace{1cm} (2.8) \hspace{1cm} (2.9)

where

\[ D(s) = s + \frac{\alpha_1 \beta_1}{\alpha_2 \beta_2 RC} \]  \hspace{1cm} (2.10)

The non ideal pole frequency of the first order section of Fig. 2.3 can be expressed as:

\[ \omega_{0,n} = \frac{\alpha_1 \beta_1}{\alpha_2 \beta_2 RC} \]  \hspace{1cm} (2.11)

Thus, from equations (2.11), it is clear that there is an insignificant deviation of the non-ideal pole-frequency for the first order filter section shown within Fig. 2.3.

**Design and Verification**

The proposed first-order filter section was verified with design values of \( R = 1\Omega \) and \( C = 0.1\text{nF} \) resulting in pole frequency \( f_0 = 1.59 \text{ MHz} \) which is obtained using equation (2.5). The supply voltages are taken to be \( V_{DD} = -V_{SS} = 2.5V \) and \( V_{in} = -1.79V \) [16]. The MOS transistor aspect ratio for the CMOS MOCCII is given in Table 2.1.

The observed and theoretical responses for LP and HP are shown in Fig. 2.4, the AP gain and phase responses are shown in Fig. 2.5. It can be seen that they are in close conformity with the design.
Table 2.1 MOSFET dimensions of the MOCCI shown in Fig. 2.2

<table>
<thead>
<tr>
<th>TRANSISTOR</th>
<th>W (μm)</th>
<th>L (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M₁, M₂</td>
<td>0.8</td>
<td>0.5</td>
</tr>
<tr>
<td>M₃, M₄</td>
<td>14.4</td>
<td>0.5</td>
</tr>
<tr>
<td>M₅, M₆, M₁₆, M₂₀</td>
<td>4</td>
<td>0.5</td>
</tr>
<tr>
<td>M₇</td>
<td>10</td>
<td>0.5</td>
</tr>
<tr>
<td>M₈, M₉, M₁₇, M₂₁</td>
<td>45</td>
<td>0.5</td>
</tr>
<tr>
<td>M₁₀, M₁₁, M₁₂, M₁₈, M₂₂</td>
<td>9.6</td>
<td>0.9</td>
</tr>
<tr>
<td>M₁₃, M₁₄, M₁₅, M₁₉, M₂₁</td>
<td>45</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Figure 2.4 Frequency response of low-pass and high-pass filter section

Figure 2.5 Frequency response of all-pass filter section
2.4 Second-Order Voltage-Mode Filter

This section proposes a new voltage mode multifunctional biquadratic filter (MBF) circuit using a single 
CFOA as shown in Fig. 2.6. Analysis of the circuit shows that with \( V_B = 2.5 \text{V} \) and node P grounded, 
the two VM transfer functions are:

\[
\frac{V_{o1}}{V_{in}} = \frac{s^2}{D(s)} \quad (2.12)
\]

\[
\frac{V_{o2}}{V_{in}} = -\frac{s}{R_1C_2 D(s)} \quad (2.13)
\]

Figure 2.6 The multifunctional biquadratic filter

Equations (2.12) and (2.13) realize HP and BP filter responses respectively. Setting \( V_B = 0 \text{V} \) results in 
\( V_F = V_{in} \). The circuit then yields the two transfer functions as:

\[
\frac{V_{o1}}{V_{in}} = \frac{s^2 + \frac{1}{R_1R_2C_1C_2}}{D(s)} \quad (2.14)
\]

\[
\frac{V_{o2}}{V_{in}} = -\frac{\frac{1}{R_1C_2}}{D(s)} \quad (2.15)
\]

where \( D(s) = s^2 + s \frac{1}{R_1C_1} + \frac{1}{R_1R_2C_1C_2} \quad (2.16) \)

Equations (2.14) and (2.15) represent the BR and LP biquadratic functions respectively. The pole 
frequency \( (\omega_0) \), pole-Q and the bandwidth (BW) respectively are expressed as:

\[
\omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}}, \quad BW = \frac{1}{R_1C_1}, \quad Q = \frac{R_1C_1}{\sqrt{R_2C_2}} \quad (2.17)
\]

The various filter gains i.e. the high-pass (\( H_{HP} \)), band-pass (\( H_{BP} \)), band-reject (\( H_{BR} \)) and low-pass gain 
(\( H_{LP} \)) from equations (2.12) to (2.15) can be expressed as:
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\[ H_{HP} = H_{LP} = H_{RR} = 1 \quad \text{and} \quad H_{BP} = \frac{R_1 C_1}{R_2 C_2} \]  

(2.18)

**Non-Ideal Analysis**

The proposed filter of Fig. 2.6 is re-analyzed using equation (2.6) which yields the following non-ideal voltage transfer functions. If \( V_B = 2.5V \) then \( V_P = 0 \), then:

\[
\frac{V_{a1}}{V_{in}} = \frac{s^2}{D_n(s)} \]  

(2.19)

\[
\frac{V_{a2}}{V_{in}} = -\frac{s \alpha}{D_n(s)} \]  

(2.20)

Setting \( V_B = 0V \) results in \( V_P = V_{in} \). The circuit then yields the two transfer functions as:

\[
\frac{V_{a1}}{V_{in}} = \frac{s^2 + \frac{\alpha}{R_1 R_2 C_1 C_2}}{D_n(s)} \]  

(2.21)

\[
\frac{V_{a2}}{V_{in}} = -\frac{\alpha}{R_1 R_2 C_1 C_2} \]  

(2.22)

where

\[
D_n(s) = s^2 + s \frac{1}{R_1 C_1} + \frac{\alpha}{R_1 R_2 C_1 C_2} \]  

(2.23)

The non-ideal values of the pole frequency- \( \omega_{0,n} \) and pole-Q, are:

\[
\omega_{0,n} = \sqrt{\frac{\alpha}{R_1 R_2 C_1 C_2}} \quad , \quad Q_n = \sqrt{\frac{\alpha R_1 C_1}{R_2 C_2}} \]  

(2.24)

**Design and Verification**

The circuit is designed for a cut-off frequency of \( f_0 = 5 \text{KHz} \) and with a quality factor of unity. By using equation (2.17) and the assumption that \( R_1 = R_2 = R \) and \( C_1 = C_2 = C = 10 \text{nF} \), results in \( R = 3.3 \text{K}\Omega \).

For experimental verification, an AD844, and a \( \mu \text{A} 741 \) were chosen as a CFOA and additional buffer respectively, along with an NPN transistor with \( R_P = 33 \text{K}\Omega \). The simulated and experimental HP and BP filter responses so obtained are shown in Fig. 2.7, while the BR and the LP responses are shown in Fig. 2.8. It is clear from Fig. 2.7 and Fig. 2.8 that the experimental and simulated results are in close conformity with the design.
2.5 Voltage- and Current-Mode Multi-Phase Oscillators

This section describes two multi-phase oscillators. One of them operates in CM and VM while the other operates in VM only.

Multiphase oscillators, capable of producing multiple signals that are equally separated in phase, constitute an important functional block in many communication, power electronics, measurement and instrumentation systems. Various multiphase oscillator designs have been proposed [16, 22, 26, 28, 30, 57]. These circuits exhibit functionalities such as CM outputs, quadrature outputs, multiphase outputs, etc. Other features include orthogonal control of the condition and frequency of
oscillation, low component count and the use of grounded passive components from the point of view of monolithic integration.

**Current-Mode And Voltage-Mode Oscillator:**

The CM first-order filter section of Fig. 2.3 is used to realize a CM multi-phase sinusoidal oscillator by cascading the all-pass output with an MOCCI based non-inverting CM integrator, as shown in Fig. 2.9. Analysis of the oscillator yields the following characteristic equation:

\[
s^2 + s \left[ \frac{1}{R_1C_1} - \frac{1}{R_2C_2} \right] + \frac{1}{R_1R_2C_1C_2} = 0 \tag{2.25}
\]

which results in the condition of oscillation as:

\[
R_1C_1 \geq R_2C_2 \tag{2.26}
\]

![Figure 2.9 The MOCCI based CM-EPSO circuit](image)

and the frequency of oscillation as:

\[
\omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}} \tag{2.27}
\]

Assuming \(R_1 = R_2 = R\) and \(C_1 = C_2 = C\), equation (2.27) reduces to:

\[
\omega_0 = \frac{1}{RC} \tag{2.28}
\]

From Fig. 2.9, the various current outputs can be expressed as:

\[
\begin{align*}
I_{o2} &= \frac{I_{o3}}{\sqrt{2}} \angle -\frac{\pi}{4}, \\
I_{o3} &= I_{o1} \angle \frac{\pi}{2}, \\
I_{o4} &= \frac{I_{o5}}{\sqrt{2}} \angle -\frac{3\pi}{4}, \\
I_{o5} &= I_{o1} \angle -\frac{\pi}{2}, \\
I_{o6} &= \frac{I_{o7}}{\sqrt{2}} \angle -\frac{3\pi}{4}, \\
I_{o7} &= I_{o1} \angle \frac{\pi}{2}
\end{align*} \tag{2.29}
\]
Thus it is evident from equation (2.29), that the oscillator of Fig. 2.9 realizes a CM eight-phase sinusoidal oscillator (CM-EPSO). The magnitude of the output currents are $I_{o1} = I_{o3} = I_{o5} = I_{o7}$, $I_{o2} = I_{o4} = I_{o6} = I_{o8}$ and $I_{o2} = (1/\sqrt{2}) I_{o1}$. The phaser diagram is shown in Fig. 2.10. It can be observed that just by loading the current outputs of CM-EPSO with appropriate resistors; a VM eight phase sinusoidal oscillator (VM-EPSO) with equal magnitudes is realized.

![Phaser Diagram of CM-EPSO](image)

**Figure 2.10 The phaser diagram of CM-EPSO**

**Design and Verification**

The oscillator is designed for an oscillating frequency $f_0 = 1.59$ MHz. Assuming $R_1 = R_3 = R = 1.0\, \text{k}\Omega$, equation (2.28) results in $C = 0.1\, \text{nF}$. It is clear that the oscillations were set by trimming resistor $R_t$. Simulation of CM-EPSO results in waveforms depicted in Fig. 2.11 which show the oscillation frequency to be equal to 1.4 MHz. This value is $\sim 12\%$ in error with the theoretical value. Such errors occur at high frequencies as a result of parasitic capacitances.

![Wave-_shapes of the designed CM-EPSO of Fig. 2.9](image)

**Figure 2.11 The wave-shapes of the designed CM-EPSO of Fig. 2.9**
Next, the current outputs of the designed CM-EPSO were loaded with resistors \( R_1 = R_3 = 7\, \text{K}\Omega \), \( R_2 = R_4 = 10\, \text{K}\Omega \), \( R_5 = R_7 = 6.7\, \text{K}\Omega \) and \( R_6 = R_8 = 9.6\, \text{K}\Omega \). The observed wave-shapes of the VM-EPSO are shown in Fig. 2.12, which verify the theory.

![Figure 2.12 The wave-shapes of the designed VM-EPSO](image)

**Voltage-Mode Four-Phase Oscillator**

This section presents a tunable VM four phase sinusoidal quadrature oscillator (VM-FPSQO) using two multi-output second generation current conveyors (MOCCII) as shown in Fig. 2.13.

![Figure 2.13 The VM-FPSQO circuit using CMOS MOCCII](image)

Analyzing the oscillator yields the characteristic equation as:

\[
s^2 + s \left( \frac{1}{R_1} \frac{1}{C_2} \right) + \frac{1}{R_2 R_3 C_1 C_2} = 0 \tag{2.30}
\]

Equation (2.30) results in the condition of oscillation as:

\[
R_1 \geq R_2 \tag{2.31}
\]

and the frequency of oscillation as:

\[
\text{Frequency} = \frac{1}{2\pi \sqrt{\frac{1}{R_1 C_2}}} \tag{2.32}
\]
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\[ \omega_0 = \sqrt{\frac{1}{R_2 R_3 C_1 C_2}} \]  

(2.32)

It is clear from (2.31) and (2.32) that \( R_3 \) can independently control the frequency of oscillation without disturbing the condition of oscillation. With \( R_2 = R_3 = R \), and \( C_1 = C_2 = C \) the frequency of oscillation given in (2.32) reduces to:

\[ \omega_0 = \frac{1}{RC} \]  

(2.33)

The four voltage outputs of the VM-FPSQO of Fig. 2.13 at the oscillating frequency can be expressed as:

\[ V_{o2} = -jV_{o1}, \quad V_{o3} = -V_{o1}, \quad V_{o4} = jV_{o1} \]  

(2.34)

Design and Verification

To verify the proposed theory, the VM-FPSQO of Fig. 2.13 is designed for an oscillating frequency of \( f_0 = 1 \)MHz. The supply voltages are taken as \( V_{DD} = -V_{SS} = 2.5 \)V and \( V_{BB} = -1.79 \)V [16]. The MOS transistor aspect ratio for the CMOS MOCCII is given in Table 2.1. Assuming \( R_1 = R_2 = R_3 = R_4 = R = 6 \)k\( \Omega \), equation (2.33) results in \( C_1 = C_2 = 26 \)pF. The observed wave shapes of VM-FPSQO are shown in Fig. 2.14, which are in close conformity with the design. The VM-FPSQO is also tuned by varying \( R_3 \) and the observed variation of frequency is shown in Fig. 2.15, which demonstrates single resistance control of the oscillator pole frequency.

![Figure 2.14 Output waveforms of VM-FPSQO](image-url)
2.6 Precision Rectifier

This section presents a bi-phase amplifier which, in turn, is utilized to realize a precision rectifier. The realized bi-phase amplifier is shown in Fig. 2.16. The amplifier uses a voltage-controlled switch $S$. When $S$ is open, the output voltage $V_o$ can be expressed as:

\[ V_o = \frac{V_{in}}{R_3} \]

![Figure 2.16 CCII based bi-phase amplifier](image)
When $S$ is closed, the voltage at node $P$ is zero. Now by selecting $R_2=2R_1$, the output voltage becomes:

$$V_0 = -V_{in}$$  \hfill (2.36)

From equations (2.35) and (2.36), it is clear that the circuit of Fig. 2.16 realizes a bi-phase amplifier. To realize a precision rectifier, the switch $S$ of the bi-phase amplifier is implemented using a P-MOS transistor along with a CCII+ based non-inverting comparator as shown in Fig. 2.17.

During the positive half of the cycle, the comparator output is high and the switch is open thus leading to $V_0 = V_{in}$. During the negative half of the cycle, the comparator output is low and the switch is closed. Hence the bi-phase amplifier behaves in an inverting mode leading to $V_0 = -V_{in}$. Consequently, full wave rectification is achieved. By shorting resistor $R_3$, the same circuit behaves as a half wave rectifier. This is possible since during the negative half of the cycle, node $P$ is grounded which results in $V_0 = 0$. Thus the precision rectifier of Fig. 2.17 operates as a full-wave as well as a half-wave rectifier.

**Non-Ideal Analysis**

The above analysis is done without taking into account the non-ideal transfer gain and the parasitics associated with the analog building blocks (CCII+). In reality, however, there are parasitic resistances and capacitances at the X, Y and Z terminals and the Y and Z terminals respectively. These parasitic impedances cause additional poles or zeros in the transfer functions, which are effective at low and high frequencies. For instance, the parasitic resistances in series with external capacitors connected to the X terminals of the CCII+s affect the performance of the filter at high frequencies. Similarly, high-frequency performance is hampered due to the parasitic capacitances at terminals Z and Y of the conveyors, connected to external grounded resistors at the corresponding terminals. Apart from this, the
parasitic resistance at terminal Z of the current conveyor affects the low-frequency performance of the filter, if a grounded capacitor is connected to the Z terminal. Therefore, a more realistic performance analysis of the proposed circuit is necessary.

1. Non-ideal transfer gain

Re-analysis of the proposed circuit of Fig. 2.17 by taking into account the non-ideal relations of the CCII (given in equation (2.6)) yields the following relation:

During the positive half cycle:

$$\frac{V_{0,0}}{V_i} = \frac{R_2}{2R_1} \left[ \beta_{11} + 3\beta_1\alpha_{11} - 2\alpha_i \right] \left( 1 + \alpha_i \right)$$

(2.37)

During the negative half cycle:

$$\frac{V_{0,n}}{V_i} = -\frac{R_2}{R_1} \left( \frac{\alpha_i}{1 + \alpha_i} \right)$$

(2.38)

Selecting $R_2 = 2R_1$, equations (6) and (7) reduce to:

$$\frac{V_{0,0}}{V_i} = \left[ \beta_{11} + 3\beta_1\alpha_{11} - 2\alpha_i \right] \left( 1 + \alpha_i \right)$$

(2.39)

$$\frac{V_{0,n}}{V_i} = -2 \left( \frac{\alpha_i}{1 + \alpha_i} \right)$$

(2.40)

It is to be further noted that equations (2.39) and (2.40) reduce to equations (2.35) and (2.36) respectively for $\alpha_i = \beta_{11} = 1$.

2. Effect of parasitics

A CCII is characterised by the following parasitic port impedances. The parasitics are $R_X$, $R_Y//C_Y$ and $R_Z//C_Z$ for X-, Y- and Z ports respectively. Considering the X- and Y- terminal parasitics, the output voltage during the positive half cycle can be expressed as:

$$\frac{V_0'}{V_i} = -\frac{R_2 - R_X}{(2R_1 + R_X)} \left[ s + \frac{1}{C_Y R_Y} - \frac{(2R_1 + R_X)}{C_Y R_s (R_2 - R_X)} \right]$$

(2.41)

For a typical design $R_2 >> R_Y$ thus $R_s//R_Y \approx R_s$. By selecting $R_2 = 2R_1$, equation (2.41) reduces to:

$$\frac{V_0'}{V_i} = -\frac{(2R_1 - R_X)}{(2R_1 + R_X)} \left[ s + \frac{1}{C_Y R_Y} - \frac{(2R_1 + R_X)}{C_Y R_s (2R_1 - R_X)} \right]$$

(2.42)

During the negative half of the cycle the output voltage can be expressed as:
\[
\frac{V'_0}{V_i} = -\frac{(2R_1 - R_X)}{(2R_1 + R_X)} \left[ \frac{s + \frac{1}{C_Y r_{on}} - \frac{(2R_1 + R_X)}{C_Y R_3(R_2 - R_X)}}{s + \frac{R_3 + r_{on}}{C_Y R_3 r_{on}}} \right]
\]

where \( r_{on} \) is the ON resistance of MOSFET. Again, in equation (2.43) \( r_{on} \ll R_z \) thus \( r_{on} // R_z \approx r_{on} \). By selecting \( R_z = 2R_0 \), equation (2.43) reduces to:

\[
\frac{V'_0}{V_i} = -\frac{(2R_1 - R_X)}{(2R_1 + R_X)} \left[ \frac{s + \frac{1}{C_Y r_{on}} - \frac{(2R_1 + R_X)}{C_Y R_3(R_2 - R_X)}}{s + \frac{1}{C_Y r_{on}}} \right]
\]

Closer inspection of equations (2.42) and (2.44) for a typical design shows that the gain of the rectified output is not affected. This can be attributed to the fact that the parasitic \( R_X \) appears in series with the external resistance \( R_1 \) and since \( R_1 >> R_X \), \( R_X \) can be neglected. The pole and zero introduced due to parasitics are found to be symmetrical and approximately equal in magnitude, thus they may be the cause for certain phase errors. It is also to be noted that for open-switch as well as for closed-switch conditions (equation (2.42) and (2.44)), the path from port-Y to ground will contain \( R_Y \) or \( R_Y // r_{ON} \) respectively. Therefore both equations (2.42) and (2.44) show a ‘minus’ sign.

**Design and Verification**

To verify the proposed theory, the precision rectifier of Fig. 2.17 is designed and simulated. The PMOS switch is implemented with a \( W/L \) ratio of 0.35 \( \mu \text{m} / 0.35 \mu \text{m}. \) These \( W/L \) values ensure small ON resistance of switch (PMOS transistor) thereby making \( V_p \approx 0 \) (when the switch is on). For a bi-phase amplifier, selecting \( R_1 = 1\text{K}\Omega \) leads to \( R_z = 2\text{K}\Omega. \) \( R_3 \) and \( R_4 \) are selected as 150\( \Omega \) and 400\( \Omega \) respectively. The supply voltages are taken as \( V_{DD} = -V_{SS} = 2.5\text{V} \) and \( V_{BB} = -1.79\text{V} \) \[16\]. The MOS transistor aspect ratio for the CMOS CCII is given in Table 2.1.

The resulting DC transfer characteristics of the proposed precision rectifier are shown in Fig. 2.18. Its performance is also verified with a sinusoidal input of 20mV with peaks at 10 KHz, 100 KHz and 1 MHz. The results are depicted in Fig. 2.19-2.21. The distortions visible during the clock switching edge at increasing frequencies are mainly due to the switching limitation of the transistor. These may be reduced by employing high frequency transistors.
Figure 2.18 DC transfer characteristics of the precision rectifier

Figure 2.19 Input and output waveform at 10KHz

Figure 2.20 Input and output waveforms at 100KHz

Figure 2.21 Input and output waveforms at 1MHz
**ANALOG SIGNAL PROCESSING MODULES USING CCII**

*Comparison with Existing Precision Rectifiers:*

The precision rectifier proposed in this work is compared to similar circuits reported in literature. The results are depicted in Table 2.2.

<table>
<thead>
<tr>
<th>Reference No.</th>
<th>Reference</th>
<th>Feature</th>
<th>Active building block</th>
<th>Diodes</th>
<th>Resistors</th>
<th>HW/FW</th>
<th>Test Frequency</th>
<th>Amplitude Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>[42]</td>
<td>2 CCII, 2 OPAMP</td>
<td>4</td>
<td>2</td>
<td>N/Y</td>
<td>-</td>
<td>-</td>
<td>100KHz</td>
<td>±500mV</td>
</tr>
<tr>
<td>[44]</td>
<td>1 FDIO-OTA</td>
<td>4</td>
<td>1</td>
<td>Y/Y</td>
<td>-</td>
<td>-</td>
<td>500MHz</td>
<td>±500mV</td>
</tr>
<tr>
<td>[45]</td>
<td>2 CCII</td>
<td>4</td>
<td>2</td>
<td>N/Y</td>
<td>-</td>
<td>-</td>
<td>30MHz</td>
<td>-</td>
</tr>
<tr>
<td>[41]</td>
<td>2 CCII</td>
<td>4</td>
<td>2</td>
<td>N/Y</td>
<td>-</td>
<td>-</td>
<td>100KHz</td>
<td>±100mV</td>
</tr>
<tr>
<td>[46]</td>
<td>1 CCII, 2 OPAMP</td>
<td>2</td>
<td>3</td>
<td>N/Y</td>
<td>-</td>
<td>-</td>
<td>100MHz</td>
<td>±1V</td>
</tr>
<tr>
<td>[47]</td>
<td>CCII</td>
<td>-</td>
<td>1</td>
<td>Y/N</td>
<td>-</td>
<td>-</td>
<td>100MHz</td>
<td>±25mV</td>
</tr>
<tr>
<td>[48]</td>
<td>1 CCII, 2 MOS</td>
<td>-</td>
<td>1 or 0</td>
<td>Y/Y</td>
<td>-</td>
<td>-</td>
<td>100KHz</td>
<td>±10mV</td>
</tr>
<tr>
<td>[49]</td>
<td>CDTA</td>
<td>4</td>
<td>2</td>
<td>N/Y</td>
<td>-</td>
<td>-</td>
<td>5MHz</td>
<td>±50μA</td>
</tr>
<tr>
<td>[50]</td>
<td>2 CCII, 2 MOS</td>
<td>-</td>
<td>2</td>
<td>N/Y</td>
<td>-</td>
<td>-</td>
<td>20KHz</td>
<td>±20mV</td>
</tr>
<tr>
<td>[51]</td>
<td>3 CCCII</td>
<td>-</td>
<td>-</td>
<td>N/Y</td>
<td>-</td>
<td>-</td>
<td>100KHz</td>
<td>-</td>
</tr>
<tr>
<td>[52]</td>
<td>3 CCII</td>
<td>-</td>
<td>-</td>
<td>N/Y</td>
<td>-</td>
<td>-</td>
<td>1MHz</td>
<td>±80μA</td>
</tr>
<tr>
<td>[53]</td>
<td>2 CCII, 3 MOS</td>
<td>-</td>
<td>-</td>
<td>N/Y</td>
<td>-</td>
<td>-</td>
<td>250KHz</td>
<td>±50mV</td>
</tr>
<tr>
<td>[54]</td>
<td>DXCCII, 3MOS</td>
<td>-</td>
<td>-</td>
<td>N/Y</td>
<td>-</td>
<td>-</td>
<td>1MHz</td>
<td>±150mV</td>
</tr>
<tr>
<td>Proposed</td>
<td>2 CCII, 1 MOS</td>
<td>-</td>
<td>4</td>
<td>Y/Y</td>
<td>-</td>
<td>-</td>
<td>1MHz</td>
<td>±20mV</td>
</tr>
</tbody>
</table>

It may be noted that most of the available circuits are based on two current conveyors. Certain designs have also been reported [44, 47, 48, 54] which are based on a single current conveyor or OTA. One of these [47] performs only half-wave rectification. As far as the frequency range is concerned, the circuit proposed in [47] with half wave capability achieves good performance. Similarly the work proposed in [45] also exhibits good frequency performance but employs a larger number of diodes.

The circuits proposed in [48, 50] exhibit good precision in terms of voltage (10mV-20mV). However the operating frequency for the circuit in [50] is limited as compared to that in [48], though it may not be entirely fair to compare these circuits since they fall in the category of tunable precision rectifiers. However, as is clear from Table 2.2, the proposed circuit exhibits good precision, both half-wave and full-wave rectification with an operating frequency range of ~10KHz to ~1MHz with a signal amplitude of 20mV.

### 2.7 Conclusion

In this chapter, a novel CM versatile first-order filter section is realized which provides load insensitive low-pass, high-pass and all-pass outputs with a single current input. The versatile filter section uses only one grounded resistor and capacitor along with two multi-output second generation current conveyors. The all-pass filter section is utilized to realize a CM eight-phase sinusoidal oscillator.
The CM oscillator outputs are loaded with resistors to realize a VM eight-phase sinusoidal oscillator. The effects of non-idealities of the current conveyors are also studied and are found to have no detrimental effects on the realized multi-phase sinusoidal oscillator.

All realizations use grounded resistors and capacitors. Grounded resistors are replaced by the well-known method of MOSFET-based resistors [58] making it more suitable for monolithic implementation. Other notable features of the proposed filter are multi-output responses (LP, HP, AP), with no component matching conditions needed, lesser number of passive components, and a single input.

A new VM multifunctional bi-quadratic filter is also proposed and designed which employs a single current feedback amplifier along with two resistors, two capacitors, a buffer and a switch. The filter provides two outputs for each switching condition i.e. high-pass and band-pass for one switching condition and band-elimination and low-pass for the other switching condition.

A four phase voltage mode sinusoidal oscillator is also realized. It’s important features are: (i) grounded passive elements, (ii) single resistance control of frequency of oscillation, and (iii) independent control of frequency of oscillation and condition of oscillation.

A novel precision rectifier is also realized which is based on a VM bi-phase amplifier. To switch the bi-phase amplifier from non-inverting to inverting mode, a MOSFET switch and a CCII based comparator is used. The results prove that the circuit achieves half-wave as well as full-wave precision rectification. The simulated precision rectifier also exhibits a wide frequency range of operation and uses simple hardware. Improving the performance and high precision capability of the circuit is an area open for further research.

Analog signal processing modules designed within this Chapter cannot process differential signals. Only single-ended signals can be processed through these modules. As a result, these circuits are unable to offer the advantages associated with differential operation. This limitation can be overcome by making use of a differential difference current conveyor, as is discussed in the next Chapter.