Chapter 3

DESIGN OF ADIABATIC CIRCUIT

3.1 Introduction

The details of the initial experimental work carried out to understand the energy recovery adiabatic principle are presented in this section. This experimental work includes discrete solution of step charging towards adiabaticity, continuous solution of applying ramp type voltage, plotting energy recovery waveform of an adiabatic circuit and implementation of few previously published adiabatic logic style.

This research work is carried out in Cadence design environment called ICFB (Integrated Circuit Front to Back) version 5.1.41. The ICFB tool is an integrated design environment for custom IC designers. The Virtuoso Schematic Editor Product family is integrated with the Virtuoso Analog Design Environment, Virtuoso Spectre/HSPICE, and Virtuoso Layout Suite for the complete solution for front to back custom analog, digital, RF and mixed signal design flows. It provides capabilities that speed design entry of the largest and most complex custom designs, wire routing capabilities and supports multi-sheet designs. Besides it also provides the ability to design hierarchically. Cadence Virtuoso Analog Design Environment is the advanced design and simulation environment for the Virtuoso platform. It gives access to a parasitic estimation and comparison flow and optimization algorithms.

The simulations have been carried out using Spectre tool which uses transistor model Berkely BSim3v3 for calculating drain current, power dissipations etc. At deep sub-micron technologies leakage power becomes dominant. Since the objective of this research work on energy recovery adiabatic logic was to reduce dynamic power dissipation first, instead of selecting 45nm or 22nm technologies,
we selected 180nm technology for this research work. The transistors were selected from gpdk (general process design kit) 180nm library whereas other components such as power supplies were selected from the Design library. In this chapter besides the experimental details of the experiments performed by us, the theoretical details are also presented wherever required with relevant references from the literature.

3.2 Designing Adiabatic Circuit

The work on design of adiabatic circuit is divided into two parts; ‘understanding adiabatic principle’ and ‘understanding design of adiabatic logic style’. In the first part, the experiments of ‘step-charging CMOS inverter’ and ‘adiabatic amplifier’ were carried out. The discussions on these two experiments consolidate the theory of energy recovery principle. The experiments in the second part include the implementation of one full adiabatic logic style (SCRL), two quasi-adiabatic logic styles (CAL and ECRL) and cascading of adiabatic stages. The outcomes of this work helped us to formulate the design considerations which were taken into account while designing and implementing an adiabatic circuit.

3.2.1 Effect of step charging:

This experiment was performed to study the effect of step charging (refer Section 2.2.2-A) and confirm that the energy dissipation is inversely proportional to the number of steps taken to apply final value of $V_{DD}$.

### Circuit Description:

The working principle of step-charging is explained in Section 2.2.2-A. NMOS pass transistors are used to apply a step voltage to a conventional CMOS inverter as shown in Figure 3.1 below. $V_1$ ($0.33V_{DD}$), $V_2$ ($0.66V_{DD}$) and $V_3$ ($1.0V_{DD}$) are the three voltages applied at the source of respective transistors. The three transistors are switched on by control signals applied to their gates after predetermined time intervals as given in ‘input stimuli’ to charge the capacitor. This generates a step-like voltage which is applied across the inverter. The step voltage degrades by $V_{TN}$ in the last step which may be avoided by selecting ‘$V_3 = V_{DD} + V_{TN}$’. Energy dissipation is measured by integrating the power dissipated in the transient analysis period.

### Variables and Analysis:

<table>
<thead>
<tr>
<th>Variables</th>
<th>Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Initial value</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>1.8V</td>
</tr>
</tbody>
</table>
‘V<sub>DD</sub>’ is defined as a tool variable.

* In conservative mode, the accuracy of measurement is given more importance rather than speed of measurement.

**Input Stimuli:**

<table>
<thead>
<tr>
<th>Type</th>
<th>Signal</th>
<th>DC Signal</th>
<th>V&lt;sub&gt;DD&lt;/sub&gt;</th>
<th>V&lt;sub&gt;1&lt;/sub&gt; = 0.3 X ‘V&lt;sub&gt;DD&lt;/sub&gt;’</th>
<th>V&lt;sub&gt;2&lt;/sub&gt; = 0.6 X ‘V&lt;sub&gt;DD&lt;/sub&gt;’</th>
<th>V&lt;sub&gt;3&lt;/sub&gt; = 1.8V</th>
<th>V&lt;sub&gt;SS&lt;/sub&gt; = 0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse</td>
<td>Signal</td>
<td>Initial</td>
<td>Final</td>
<td>t&lt;sub&gt;d&lt;/sub&gt;</td>
<td>t&lt;sub&gt;r&lt;/sub&gt;</td>
<td>t&lt;sub&gt;f&lt;/sub&gt;</td>
<td>t&lt;sub&gt;on&lt;/sub&gt;</td>
</tr>
<tr>
<td>Pulse</td>
<td>VG1</td>
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<td>‘V&lt;sub&gt;DD&lt;/sub&gt;’</td>
<td>40ns</td>
<td>1ns</td>
<td>1ns</td>
<td>40ns</td>
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<tr>
<td>Pulse</td>
<td>VG2</td>
<td>0</td>
<td>‘V&lt;sub&gt;DD&lt;/sub&gt;’</td>
<td>80ns</td>
<td>1ns</td>
<td>1ns</td>
<td>40ns</td>
</tr>
<tr>
<td>Pulse</td>
<td>VG3</td>
<td>0</td>
<td>‘V&lt;sub&gt;DD&lt;/sub&gt;’</td>
<td>120ns</td>
<td>1ns</td>
<td>1ns</td>
<td>40ns</td>
</tr>
</tbody>
</table>

The various terms in above table have the usual meanings. (Refer Symbols and Meanings on page number ix). The experiment was performed with normal charging (requires one NMOS transistor), two step charging (requires two NMOS transistors) and three step charging. The energy dissipation results are as follows.

**Results:**

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Type of Charging</th>
<th>Energy Dissipated</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Normal</td>
<td>0.92pJ</td>
</tr>
<tr>
<td>2</td>
<td>Two-step charging</td>
<td>96aJ</td>
</tr>
<tr>
<td>3</td>
<td>Three-step charging</td>
<td>95aJ</td>
</tr>
</tbody>
</table>

**Observations and Comments:** It is obvious from the above table that the energy dissipation reduces as the number of steps (in charging) is increased. However it is further seen that the energy dissipation does not decrease linearly with number steps as is expected from theory. This can be attributed to the fact that the result reported here is for the total energy dissipated in the circuit including pass transistors required to generate the voltages for step charging and not only for the inverter. The decrease in the energy dissipation with increase in the number of steps is compensated by the energy dissipation taking place in the pass transistors eventually reducing the overall effect of energy reduction. The more striking and important observation is that step charging has reduced the energy dissipation by almost six orders.

**3.2.2 Adiabatic Amplifier:**

This experiment was performed to implement the adiabatic amplifier published by W Athas and et al [17]. To verify energy-recovery principle.

**Circuit Description:** A typical adiabatic switching circuit is as shown in Figure 3.2. It consists of two transmission gates, two NMOS clamps and ramp type...
Figure 3.1: Three Step Charging of CMOS Inverter
power-clock supply $V_A$. The ramp type of power-clock supply generates a constant current source. The operation of the circuit is divided into three phases viz Charging phase, Evaluation phase and Recovery phase. The load capacitor is adiabatically charged during the Charging phase i.e. when $V_A$ rises from zero to maximum. During the Evaluation time, output voltages are stable and can be used by next logic block(s). The load capacitor discharges into $V_A$ as it ramps down to zero during Recovery phase.

![Figure 3.2: Circuit Schematic of Typical Adiabatic Amplifier [2]](image)

The adiabatic amplifier is implemented in Virtuoso environment, first by designing the T-gate and inverter separately and then using their symbols in final design as shown in Figure 3.3. A PMOS transistor is added between the ramp power supply and the circuit to help in monitoring the direction of current flow. This is required to prove the energy recovery principle.

![Figure 3.3: Circuit Schematic of Typical Adiabatic Amplifier in Virtuoso](image)
A $V_{DD}$ of 5V was applied since the transistor sizes chosen was Microns. The ramp type voltage was simulated in such a way to give each of the charging, evaluation and recovery times as 40ns each. Ideally, the charging time and recovery time should be greater than three times the time constant of the adiabatic amplifier $3R_{Tg}C_L$ i.e the time constant of the adiabatic amplifier. The typical value of the ON-state resistance of 180nm MOS transistor is 1.3KΩ and the tool assumes a load capacitance of 2.5fF if no load capacitor is connected. Therefore, the reasonable estimation of the time constant of the adiabatic amplifier is 9.75ps. It has been observed that charging and discharging time of 40ns is large enough for the given circuit to adiabatically charge and discharge the capacitive load.

Variables and Analysis:

<table>
<thead>
<tr>
<th>Variables</th>
<th>Initial value</th>
<th>Type</th>
<th>Duration</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>5.0V</td>
<td>Transient, conservative</td>
<td>500ns</td>
<td>Output simulation</td>
</tr>
</tbody>
</table>

Input Stimuli:

<table>
<thead>
<tr>
<th>DC</th>
<th>Signal</th>
<th>X= $V_{DD}$</th>
<th>$V_{SS}$ =0V</th>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_f$</th>
<th>$t_{on}$</th>
<th>period</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse</td>
<td>Signal</td>
<td>Initial</td>
<td>Final</td>
<td>1ns</td>
<td>40ns</td>
<td>40ns</td>
<td>40ns</td>
<td>160ns</td>
</tr>
</tbody>
</table>

Input and Output Waveforms: Figure 3.4 shows the simulated input and output waveforms. The first waveform is the ramp type power-clock waveform $/va$. The current drawn by the adiabatic amplifier is shown in the second waveform $/M1/S$. The third and the forth waveforms are input $/x$ and output $/out1$ waveforms. The energy dissipation waveform is shown separately in Figure 3.5.

Results: The energy dissipated after three input cycles is 127pJ.

Observations and Comments: The current drawn by the circuit during the charging phase is positive i.e. it flows from the power-clock supply to the load when the power-clock voltage is ramping. The output voltage slowly changes its logic state. When the power-clock supply ramps down during the recovery phase the load adiabatically discharges into the power-clock supply. The current drawn by the circuit becomes negative indicating that it flows from the load back to the power-clock supply. The output voltage changes its state slowly. The current drawn remains zero during the evaluation phase indicating that the logic states are held constant by the adiabatic circuit and there is no charge flow.
Figure 3.4: Simulated Input and Output Waveforms of Adiabatic Amplifier

Figure 3.5: Simulated Energy Dissipation Curve of Adiabatic Amplifier
It is seen from Figure 3.5 that the more than 90% energy expended during charging is only recovered during recovery period. This can be attributed to the fact that the energy lost in pull-up pMOS transistor (added between power clock and load) in the form of heat is not recoverable.

The objective of the next sub-experiment was to compare the pattern of current drawn and energy dissipation of CMOS circuit with that of adiabatic circuit. A 2:1 MUX circuit was taken as a benchmark circuit (Refer Figure 3.6). The pull down network of four NMOS transistors (N1, N2, N3 and N4) are arranged to implement the Boolean expression of 2:1 MUX i.e. $A.S + B.S$. The pull up network of four PMOS transistors (P1, P2, P3 and P4) implement the complement of the above Boolean expression. The Virtuoso implementation of the CMOS 2:1 MUX is shown in Figure 3.7. The output signal ‘F’ is high when the inputs are, ‘A’=high, ‘B’=0 and ‘S’=high. The output ‘Fbar’ is the complementary output of ‘F’. The current flowing through the point ‘X’ (Refer Figure 3.6) in the circuit is measured. The simulated waveforms are shown in Figure 3.8. It is seen that this current is always positive whenever the output /F is at logic high level. Hence, there is no energy recovery in conventional CMOS circuits. The negative spikes are the switching transients. The energy dissipation curve depicts the energy loss of in every input cycle and has a step like nature. This is in contrast to the working of adiabatic circuit where current flows in both directions and the energy gets recovered.

3.2.3 Clocked CMOS Adiabatic Logic (CAL):

The objective of this experiment was to implement Clocked CMOS Adiabatic Logic (CAL) style proposed by D Maksimovic and et al [8].

Circuit Description: The basic circuit structure of CAL inverter is shown in Figure 3.9. It uses a cross coupled CMOS inverters made up of P1, P2, N1 and N2. An auxiliary timing control signal ‘CX’ controls transistors N3 and N4 those are in series with the logic blocks; for inverters the logic blocks are NMOS transistors N5 and N6. The CX-enabled transistors allow the use of single power-clock. If ‘CX’ and the inverter input ‘F0’ both are logic high then the NMOS transistors, N3 and N5, tie the output pin ‘F1’ to ground potential. This low ‘F1’ output turns on the PMOS transistor P2. The ‘PC’ signal adiabatically charges output ‘F1’ to $V_{DD}$ through P2. As the ‘PC’ signal ramps down the output node ‘F1’ adiabatically discharges into the power-clock supply.

When the input ‘F0’ gets toggled to logic zero and assuming ‘CX’ is still at logic high then the output node ‘F1bar’ gets connected to ground potential. The output node ‘F1’ is now adiabatically charged and discharged by the power-clock signal through the PMOS transistor P1. The implementation of CAL inverter in
Figure 3.6: Circuit Schematic of CMOS 2:1 MUX

Figure 3.7: Circuit Schematic of CMOS 2:1 MUX in Virtuoso
Figure 3.8: Simulated Waveforms of CMOS 2:1 MUX Circuit

Figure 3.9: Circuit Schematic of CAL Inverter [8]
There are two cases to consider; the output does or does not change after the power-clock has returned to zero. For the case when the output does not change when the power-clock is reapplied, the output that ramped down to $V_T$ will charge up from $V_T$ to $V$ adiabatically.

If the input gets toggled i.e. the output is discharged by the pull-down NMOS, then when the power-clock is applied, both the outputs will try to simultaneously charge up once the power-clock voltage exceeds $V_T$. The output that is now held low by the pull down NMOS will charge while other output will stay clamped low. There will be some short-circuit current through the pull down NMOS of the clamped low output which will decrease as the other output charges up.

CAL logic style is designed to overcome the need of the multiphase power-clock supplies required for proper interfacing between stages. The proper switching timings of ‘CX’ signal allow the same clock signal to be applied to the next inverter stage and thus eliminates the need of multi-phase power-clock. CAL logic circuits can be implemented with integrated single-phase power-clock supply and thus eliminates high complexity of both the logic and the required power-clock generator. In general, N5 and N6 can be replaced with NMOS logic trees to perform switching involved in the evaluation of an arbitrary binary function.
### Variables and Analysis:

<table>
<thead>
<tr>
<th>Variables</th>
<th>Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Initial value</td>
</tr>
<tr>
<td>‘V(_{DD})’</td>
<td>3.0V</td>
</tr>
</tbody>
</table>

#### Input Stimuli:

| DC Signal | DC Signal | Pulse Signal | Initial Value | Initial Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | 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Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | Final Value | FinalValue  |
capacitance is $0.5CV^2$ and cannot be recovered. But a major portion of the output energy is recovered in CAL.

CAL logic style is designed to overcome the need of the multiphase power-clock supplies required for proper interfacing between stages. The proper switching timings of ‘CX’ signal allows the same clock signal to be applied to the next inverter stage and thus eliminates the need of multi-phase power-clock. CAL logic circuits can be implemented with integrated single-phase power-clock supply and thus eliminates high complexity of both the logic and the required power-clock generator.

3.2.4 Split-Rail Charge-Recovery Logic (SCRL):

The objective of this experiment was to study Split-Rail Charge-Recovery Logic (SCRL) designed by S.G. Younis [1] which is of full adiabatic logic style.

Circuit Description: SCRL inverter is based on conventional static CMOS structure as shown in Figure 3.12 and its implementation in Virtuoso is shown in Figure 3.13. The main idea is to encode the idle interval as $V/2$. A split power-clock supply is used to drive the inverter. The body of the PMOS transistor is tied to $V_{DD}$ whereas the body of the NMOS transistor is tied to $V_{SS}$. Ideally the two body terminals should be tied to the respective sources to avoid any performance degradation due to body effect. A separate test circuit is designed based on SCRL inverter as shown in Figure 3.14. This circuit uses the symbol of SCRL inverter created in Virtuoso environment. The two PMOS transistors are used in the path of the two split power supplies to monitor the current flowing into and out of the

Figure 3.11: Simulated Waveforms of CAL Inverter
power supply.

In this experiment, the input signal is assumed to be pulsed signal.

<table>
<thead>
<tr>
<th>Input Stimuli:</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>Signal</td>
<td>$V_{DD}$</td>
<td>$V_{SS}$</td>
<td>$t_d$</td>
<td>$t_r$</td>
<td>$t_f$</td>
</tr>
<tr>
<td>Pulse</td>
<td>Splitvdd</td>
<td>0</td>
<td>‘$V_{DD}$’</td>
<td>15ns</td>
<td>40ns</td>
<td>40ns</td>
</tr>
<tr>
<td>Pulse</td>
<td>Splitvss</td>
<td>‘$V_{DD}$’</td>
<td>0</td>
<td>15ns</td>
<td>40ns</td>
<td>40ns</td>
</tr>
<tr>
<td>Pulse</td>
<td>in</td>
<td>0</td>
<td>‘$V_{DD}$’</td>
<td>5ns</td>
<td>1ps</td>
<td>1ps</td>
</tr>
</tbody>
</table>

In this experiment, the input signal is assumed to be pulsed signal.

**Input and Output Waveforms:** The timings of the input signal are critical in full adiabatic circuit. The inputs have to be applied when both the split power supplies are in the idle stage having $V/2$ voltage level. Simulated input and output waveforms are shown in Figure 3.15. The first two waveforms /splitvdd and /splitvss are the trademark power-clock supplies of SCRL and the third waveform is the input to the SCRL inverter i.e. /in. The output of the SCRL inverter has
Figure 3.13: Circuit Schematic of SCRL Inverter in Virtuoso

Figure 3.14: Test Circuit Schematic of SCRL Inverter
three discrete voltage levels viz. 0, \( V_{DD}/2 \) and \( V_{DD} \). The valid logic levels of the output are 0 and \( V_{DD} \). The valid output is obtained during the time when the split power clock is applying a differential voltage of \( V_{DD} \) across the inverter. The energy recovery waveform is shown in Figure 3.16. The second last waveform is the current drawn by \( /\text{splitvdd} \) supply. The last waveform is the energy recovery waveform and proves the adiabaticity of the SCRL inverter circuit.

**Figure 3.15: Simulated Waveforms of SCRL Inverter**

**Results:** It is seen from Figure 3.16 i.e. the energy dissipation curve that almost zero energy is dissipated after one cycle.

**Observations and Comments:** SCRL is truly full-adiabatic logic style. The energy recovery is complete. The incorrect switching timings of the input signal may result in non-adiabatic loss as explained in Section 2.3.

Most of the quasi-adiabatic logic styles need dual rail inputs. These dual-rail versions of quasi-adiabatic logic styles required that each logic function be implemented twice. The performance of many adiabatic logic styles degrade due to body effect. SCRL is based on conventional, static logic structure and hence dual-rail logic and signaling are not needed. Body effects are less severe due to different type of signal-swing.

It has been reported in the PhD thesis report of S G Younis that the main disadvantage of SCRL is the number of power-clocks needed to sustain a reversible SCRL pipeline. Power-clock requirements range from sixteen signals for two-
Figure 3.16: Simulated Waveforms of Energy Recovery in SCRL Inverter

phase dynamic logic to twenty for four-phase static logic [81].

Another disadvantage of SCRL is that its signals cannot be directly interfaced to conventional logic because of the voltage level for the idle state.

But SCRL goes a long way in achieving energy recovery and is the best adiabatic logic style. Researchers are working on reducing the number of clock ticks of SCRL.

3.2.5 Efficient Charge Recovery Logic (ECRL):

The objective of this experiment was to implement Efficient Charge Recovery Logic (ECRL) style proposed by Y. Moon and et al [6].

Circuit Description: ECRL logic style has the same circuit structure as cascade voltage switch logic. The schematic of ECRL inverter is shown in Figure 3.17. NMOS transistors N1 and N2 implement the inverter logic whereas P1 and P2 allow the output nodes to discharge into the ‘V_{CLK}’.

Assuming that the ‘in’ signal is at logic high and ‘\textit{in}’ is at logic low, when the power-clock supply ‘V_{CLK}’ rises from 0 to $V_{DD}$, voltage at ‘out’ remains at $V_{SS}$ i.e. low due to switching on of the N1 transistor. The voltage at the ‘\textit{out}’ node capacitance follows the ‘V_{CLK}’ signal. When the power-clock reaches $V_{DD}$ level, the outputs hold valid logic levels. These values are maintained during the hold phase.

After the evaluation or hold phase, the ‘$V_{CLK}$’ falls down to a ground level, the ‘\textit{out}’ node capacitance discharges adiabatically into the power-clock supply.
recovering the energy. Again like CAL logic style, N1 and N2 can be replaced with NMOS logic trees to perform switching involved in the evaluation of an arbitrary binary function. The Virtuoso implementation of the ECRL inverter is shown in Figure 3.18.

![Figure 3.17: Circuit Schematic of ECRL Inverter [6]](image1)

![Figure 3.18: Circuit Schematic of ECRL Inverter in Virtuoso](image2)
Variables and Analysis:

<table>
<thead>
<tr>
<th>Variables</th>
<th>Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Initial value</td>
</tr>
<tr>
<td>‘V_DD’</td>
<td>3.0V</td>
</tr>
</tbody>
</table>

Input Stimuli:

<table>
<thead>
<tr>
<th>DC Signal</th>
<th>Pulse Signal</th>
<th>Initial</th>
<th>Final</th>
<th>t_d</th>
<th>t_r</th>
<th>t_f</th>
<th>t_on</th>
<th>period</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DD</td>
<td>PC</td>
<td>0</td>
<td>‘V_DD’</td>
<td>0ns</td>
<td>40ns</td>
<td>40ns</td>
<td>40ns</td>
<td>160ns</td>
</tr>
<tr>
<td>V_DD</td>
<td>in</td>
<td>0</td>
<td>‘V_DD’</td>
<td>0ns</td>
<td>1ns</td>
<td>1ns</td>
<td>160ns</td>
<td>320ns</td>
</tr>
<tr>
<td>V_DD</td>
<td>inbar</td>
<td>0</td>
<td>‘V_DD’</td>
<td>0ns</td>
<td>1ns</td>
<td>1ns</td>
<td>160ns</td>
<td>320ns</td>
</tr>
</tbody>
</table>

In this experiment, the input signal is assumed to be pulsed signal.

Input and Output Waveforms: Simulated input and output waveforms are shown in Figure 3.19. The two complementary inputs /in and /inbar (inbar) are simulated as square wave signals. The power-clock signal /vpc is taken as ramp type signal. The simulated output waveforms at /out and /outbar (outbar) nodes are shown. The output waveforms have replica of the power-clock signal whenever the logic level is high. The energy recovery in the ECRL inverter is shown in Figure 3.20. The last two waveforms are the current flowing through the inverter circuit and the energy dissipation curve respectively. The current waveform showing positive pulses when the power-clock is ramping up indicates that the current is flowing from the power-clock supply to the output node capacitance. This is adiabatic charging of the load capacitance. Whereas the negative current pulses indicate the adiabatic discharging of the load capacitance into the power-clock supply leading to energy recovery.

Results: The energy dissipated after two input cycles is 1.56fJ.

Observations and Comments: ECRL is developed as a refinement over ADL [4] and 2N-2N2D [50] discussed in Chapter 2. ADL and 2N-2N2D logic styles are designed to deliver the energy in the precharge phase, and recover their energy during the evaluation phase. These logic styles use diode [4] or diode-like devices for precharge and hence cause unavoidable energy loss due to voltage drop across the diodes. ECRL performs precharge and evaluation simultaneously and eliminates the need of precharge diode. Hence it dissipates less energy as compared to ADL and 2N-2N2D.
Figure 3.19: Simulated Waveforms of ECRL Inverter

Figure 3.20: Simulated Waveforms of Energy Recovery in ECRL Inverter
3.2.6 Four Stage ECRL Inverter Chain:
The objective of this experiment was to study the effect of cascading of adia-
batic logic circuits on four stage ECRL inverter chain.

Circuit Description: The circuit symbol of the ECRL inverter is created in Vir-
tuoso and then used for cascading four stages of similar ECRL inverters as shown
in Figure 3.21. Such cascading of adiabatic circuit requires multi-phase power
clocking scheme. Two inverters are used as shown to convert the two comple-
mentary simulated signals (/VPC and /VPC1) into four-phase clocks. This clock
scheme is shown in Figure 3.22. Thus, when the first inverter stage is holding the
outputs (after evaluation) these outputs are fed to the next inverter as inputs. The
power-clock signal is again taken as ramp type signal.

Figure 3.21: Circuit Schematic of Four Stage ECRL Inverter Chain

Variables and Analysis:

<table>
<thead>
<tr>
<th>Variables</th>
<th>Analysis</th>
<th>Name</th>
<th>Initial value</th>
<th>Type</th>
<th>Duration</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>'V\textsubscript{DD}'</td>
<td>3.0V</td>
<td>Transient, conservative</td>
<td>500ns</td>
<td>Output simulation,</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Input Stimuli:

<table>
<thead>
<tr>
<th>DC</th>
<th>Signal</th>
<th>Initial</th>
<th>Final</th>
<th>t\textsubscript{d}</th>
<th>t\textsubscript{r}</th>
<th>t\textsubscript{f}</th>
<th>t\textsubscript{on}</th>
<th>period</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse</td>
<td>VPC1</td>
<td>'V\textsubscript{DD}'</td>
<td>0</td>
<td>0ns</td>
<td>40ns</td>
<td>40ns</td>
<td>160ns</td>
<td></td>
</tr>
<tr>
<td>Pulse</td>
<td>VPC2</td>
<td>0</td>
<td>'V\textsubscript{DD}'</td>
<td>0ns</td>
<td>40ns</td>
<td>40ns</td>
<td>160ns</td>
<td></td>
</tr>
<tr>
<td>Pulse</td>
<td>in</td>
<td>0</td>
<td>'V\textsubscript{DD}'</td>
<td>0ns</td>
<td>1ns</td>
<td>1ns</td>
<td>160ns</td>
<td></td>
</tr>
<tr>
<td>Pulse</td>
<td>inbar</td>
<td>'V\textsubscript{DD}'</td>
<td>0</td>
<td>0ns</td>
<td>1ns</td>
<td>1ns</td>
<td>160ns</td>
<td></td>
</tr>
</tbody>
</table>
In this experiment, the input signal is assumed to be pulsed signal.

**Input and Output Waveforms:** Simulated input and output waveforms are shown in Figure 3.23. The first waveform $\text{/MP1/S}$ is the current flowing through the first and the third inverter stages. The two complementary inputs $\text{/in}$ and $\text{/inbar (in)}$ are simulated as square wave signals are shown as fifth and forth waveforms respectively. $\text{/out}$ and $\text{/outbar (out)}$ are shown as the second and the third waveform. The energy recovery in the ECRL inverter chain is shown in Figure 3.24.

**Results:** The energy dissipated after two input cycles is 6.6fJ.

The delay between the input of the first stage and the output of the forth stage is 100ns.

**Observations and Comments:** The delay introduced per stage is 25ns. The output voltage after the forth stage is distorted. The main reason of distortion is in the multi-phase power-clock supply generation scheme. The two inverters used for this purpose generate CMOS like outputs and hence have sharp transitions. These sharp transitions reduce the efficiency of adiabatic operation. This generation of power-clock scheme is definitely practical and better circuit techniques [8] must be employed. Overall, the efficiency of power-clock supply generation decides the practical implementation of adiabatic logic.
Figure 3.23: Simulated Waveforms of Four Stage ECRL Inverter Chain

Figure 3.24: Simulated Waveforms of Energy Recovery in Four Stage ECRL Inverter Chain
3.3 Summary

The basic objective of this experimentation phase was to establish the close link between the theory of energy recovery adiabatic technique and its implementation. This experimental work also provided the hands-on experience to Cadence design environment which is the industry accepted tool worldwide. Finally by verifying the theory presented in published IEEE papers, the energy and delay measurement techniques have been confirmed.

The analysis of the above experimental work brings about the following important design considerations of adiabatic circuit:

1. The evaluation (charging) and recovery (discharging) time has to be correctly chosen such that it is greater than 3 times the circuit time constant.

2. It is essential to verify whether the circuit is really behaving as adiabatic or not. It can be done by plotting and inspecting either the current drawn by the circuit or the energy dissipation curve.

3. The cross coupled CMOS inverters reduces the complexity of power-clock as explained in the Experiment no. 3 at the cost of energy loss of $0.5CV_f^2T$. This seems to be the attractive design solution for designing quasi-adiabatic logic style in which the design aim is to hold the output levels even after the input is removed.

4. Design of suitable power-clock supply for a given adiabatic logic style is a different research area in itself. Researchers have used resonant based oscillators followed by wave-shaping circuits. The size and value of on-chip passive components like L and C are not suitable for generating power-clock supply. This has prompted the use of off-chip external inductors and capacitors (ECRL[6], CAL[8], RERL[52], nRERL[35], QSERL[10], work by Akers[70]). The energy efficiency of these power clock schemes diminishes the use of adiabatic logic in real life applications. MEMS based resonators (Refer Fig. 3.22) are being tried for generating power-clock supply generation [78]. Power-clock supply generation for adiabatic circuits is a still a challenging and separate research area. Hence, the focus of our research area has been kept on designing a better quasi-adiabatic logic style only. For the rest of the experimentation work, a simulated (ideal) power-clock supply will be used.

To design a more refined quasi-adiabatic logic style which may be able to outperform the previously established quasi-adiabatic logic styles, it is essential to compare these logic styles on a common platform or a benchmarking circuit. The
need of such experimental work arises because the previous research work has been carried out on different technologies, using different benchmarking circuits and under different simulated conditions. In the next chapter, the research work on performance evaluation of selected quasi-adiabatic logic styles is presented.