Chapter 2

LITERATURE SURVEY

This chapter presents the detail survey of relevant literature on adiabatic logic published in the standard journals and database. Energy recovery adiabatic logic is a circuit or logic level low power design solution. There are many low power design techniques at different abstraction levels of digital system design which were briefly mentioned in the previous chapter. This chapter starts with literature survey on low power design techniques and justifies the need of energy recovery adiabatic technique. In the consequent sections, an overview of literature on adiabatic logic identifying the research gaps in this area is given.

2.1 Degrees of Freedom in Low Power CMOS Design

The motivations in minimizing power consumption differ from application to application. The different power requirements for different types of applications decide the trade-off between area, power and delay. CMOS has prevailed as the superior logic style because of its negligible static power dissipation. The other type of power dissipation that occurs in CMOS is short-circuit power dissipation which is also negligible because the short circuit current flows for a very small duration. The major contributor of the total power dissipation in CMOS is the dynamic power and any measure taken to reduce the dynamic power results in substantial decrease in overall power dissipation in CMOS. The three degrees of freedom inherent in low-power CMOS design space are voltage, capacitance and switching activity. These three parameters cannot be optimized independently.

With a quadratic relationship to power, voltage reduction is the must step in power reduction. The fact that the supply voltage reduction causes circuit delays to increase puts a lower bound on reduction in supply voltage, typically to $2V_T$. The issue of compatibility should also be considered while scaling down the volt-
age supply since there is some penalty involved in supporting different supply voltages.

Minimizing the capacitance i.e. the device and interconnect capacitance is another technique for minimizing the power dissipation. The capacitances can be kept at a minimum by using less logic, smaller devices, register sharing, proper placement and routing, etc. Reducing device sizes also reduces physical capacitance, but it also reduces the current drive of the transistors making the circuit operate at lower speed. This loss in performance may force the designer to increase supply voltage and hence the designer may have to give up possible quadratic reduction in power through voltage scaling for a linear reduction through capacitance scaling.

The third factor is the switching activity governed by frequency and data activity. Certain data representations such as sign magnitude have an inherently lower activity than two’s-complement. Glitching should be avoided whenever possible as it can cause unnecessary dynamic power dissipation. Again, optimization of activity cannot be undertaken independently without consideration for the effects on voltage and capacitance. The number of power reduction techniques applicable at various levels of abstraction are presented in the next section.

\section*{2.2 Low Power Themes}

Low power digital design is an optimization problem at all levels of the design i.e. technology, device, circuits, logic, architecture, algorithm and system levels. The optimization of different low power solutions is a challenging task for the researchers and largely depends upon the application requirements. Many researchers and technocrats are working in low power domain to develop innovative techniques for achieving this low power objective. Figure 2.1 shows an integrated low-power design approach and possible energy savings that can be achieved. The percentage of energy savings goes on decreasing from system level to technology level. A brief literature survey on low power digital design techniques given below compares these techniques and emphasizes the need of energy recovery technique.

At the top abstraction level i.e. system level, power management can be implemented with system logic or software controlling the power consumption of the processor and peripherals. The research work done by J. Gallant [16], S. Gary [17] and L. Gwennap [18] shows that;

1. Power dissipation of PowerPC603 microprocessor can be minimized up to 80% if clocks are supplied only to data cache, snooping logic and time base in the stand-by mode.
2. Similarly, power dissipation of MIPS 4200 microprocessor can be minimized up to 70% if the clock frequency is reduced to 25%.

3. Power reduction of 95% to 98% can be achieved in Hitachi SH7032 and PowerPC603 microprocessors respectively if all clocks are stopped.

These researches have introduced various modes of microprocessors namely ‘doze’, ‘nap’, ‘sleep’, ‘standby’ etc. But the major obstacle to weighing architectural decisions with respect to power is the difficulty in estimating the power effects of these trades-offs, especially in the absence of an implementation.

The power dissipation factor is used for comparing algorithms and for measuring the effect of algorithm level decisions. This demands for ‘estimating the algorithm-inherent dissipation’ and ‘estimating the implementation overhead’. The algorithm-inherent dissipation refers to the power consumed by the execution units and memory. V. Tiwari, S. Malik and A. Wolfe have proposed a measurement based technique to determine the weighting factor for each operation in the Intel-486 instruction set [19]. Experimental results by R. Mehra et al show that memory access and multiplication operations are power hungry and hence these functions should be optimized [20].

The implementation overhead consists of the control, overhead and implementation related memory/register power. It has been shown that the implementation-dependent power is strongly correlated to the structural property of an algorithm namely ‘spatial locality’ and ‘temporal locality’ [20]. Given a targeted hardware platform and a number of algorithm properties, techniques can be developed for prediction of implementation overhead. Low power goal at algorithmic level can be achieved in following ways;
1. If there are several algorithms for a given task, the one with least number of operations is generally preferred [21].

2. Reducing the algorithmic-inherent dissipation by replacing energy consuming operations by a combination of simpler operations [22] and reducing memory size using loop reordering and loop merging transformations [23].

3. Reducing the implementation overhead by retiming and reducing the chip area considerably [22].

Due to lack of implementation details at the algorithm level, the accuracy on estimating the implementation overhead is not so high. This can be improved only by stochastic modeling. Researchers have made the power estimation at this level more reliable with the help of the capacitance of an RTL level module [24], Dual Bit Type (DBT) model [25], and Activity-Based Control (ABC) model [26]. The accuracy of power estimation is higher at architectural level than at algorithm level.

Various circuit and logic level techniques to reduce power dissipation are:

1. Glitch power reduction: Glitches occur as a result of statistical delay variations [27] and can be avoided by precharge (domino) logic. But any hardware solution to avoid glitches will always add to power consumption.

2. Power reduction by reducing voltage swing: Power can be reduced by reducing voltage swing in case of high capacitance nodes and I/Os.

3. Power reduction in timing circuits: The research study [28] shows that gate based static flip-flop has lower power consumption than the transmission gate flip-flop, the non-precharged TSPC (True Single Phase Clock) dynamic flip-flop consumes the least power and the RS flip-flop latch is the most energy efficient.

4. Many CMOS circuit techniques have been proposed in the research literature namely standard static logic (SL), Complementary Pass-Transistor Logic (CPL), Precharged Logic (PCL), Cascade Voltage Switch Logic (CVSL) and PCVSL [28]. The experimental results by the researchers show:

   (a) Static Logic is the power-lean circuit technique.
   (b) PCL and PCVSL are the most power-hungry but these are faster as compared to others.
   (c) The differential techniques such as CPL and CVSL consume large power [29] but are advantageous in self-contained blocks like adders, multipliers etc.
5. Large capacitive loads like clock network are driven by a tapered inverter chain and its power consumption can be reduced by decreasing the tapering factor of ‘f’ [30].

6. The energy recovery adiabatic approach to low power design can be used to any digital design system. With energy-recovery CMOS, circuit energy is conserved for later use instead of allowing it to dissipate as heat in the system. Historically, the first adiabatic circuit was designed and tested by W. C. Athas and et al in 1994 [2]. Since then few researchers have shown considerable interest and subsequently developed some fully adiabatic and quasi-adiabatic circuits [31, 4, 6, 32, 33, 8, 7, 34, 35, 11, 36].

7. To minimize the power dissipated by clock, the distributed buffering scheme can be used [37] and an optimization scheme can be used to minimize skews introduced by buffers [38].

The effect of voltage scaling on reduction in power dissipation is unparalleled by any other techniques and offers quadratic power reduction. But as the $V_{DD}$ is lowered, the gate speed is also lowered if the device technology is not changed. Hence it is imperative to optimize the energy-delay product. It was shown that the energy-delay product may be expressed in terms of technology parameters [39, 40] as:

$$E \tau \propto \frac{C^2V_{DD}^{1.7}L^{0.5}T_{ox}^{0.5}}{(0.9 - \frac{V_T}{V_{DD}})^{1.3}} \left( \frac{1}{W_n} + \frac{2.2}{W_p} \right)$$  

(2.1)

The equation shows that if voltage scaling method is used to reduce the power without significantly increasing the delays, then $V_T$ should be also scaled down appropriately to maintain ratio of ($V_T / V_{DD}$) around four. Unfortunately, every 0.1V reduction in $V_T$ raises the leakage current by ten times. Low $V_T$ devices can be used when the active circuit blocks and higher $V_T$ devices can be used in idle circuit blocks. This can be achieved with DTCMOS (Double Threshold CMOS) devices or using circuit techniques namely ‘Switched-Source-Impedance’ to raise source potential [13] or by raising the body potential using ‘active well control’ method. Transistor sizing and gate oxide thickness can be also appropriately selected for optimizing the energy-delay product.

Alternative novel device structures namely ‘devices based on quantum tunneling, single-electron effect’ [41], ‘Silicon-on-Insulator (SOI)’ [42], ‘surround-gate MOSFET’ with 60mV per decade sub-threshold slope [43], ‘inter-band tunneling transistor- a PN junction acting as a non-FET voltage controlled switch’ [43], and ‘Quantum interference transistor’ [43] have been proposed for low power applications.
More accurate models are available at circuit and device level to predict the power dissipation and delay. The major obstacle to weighing architectural decisions with respect to power is the difficulty in estimating the power effects of these trades-offs, especially in the absence of an implementation. Due to lack of implementation details at the algorithm level, the accuracy on estimating the implementation overhead is not so high. This can be improved only by stochastic modeling. It has been demonstrated by several researchers that algorithm and architecture level design decisions can have a dramatic impact on power consumption [44, 45]. However there is a need of accurate design automation techniques at this level of abstraction [14]. All the low power design methodologies above the abstraction level of circuit logic can’t reduce the energy below $0.5CV^2$. The energy recovery principle which is the only solution to achieve sub-$0.5CV^2$ energy dissipation is explained in the next section.

2.3 Introduction to Energy Recovery Adiabatic Logic

Adiabatic switching technique based on energy recovery principle is one of the innovative solutions at circuit and logic level to achieve reduction in power. The circuit energy that would otherwise be dissipated as heat is conserved and reused. This concept has been adopted from thermodynamics where the literal meaning of the word ‘adiabatic’ means ‘without the flow of heat’. An ideal adiabatic process in the Carnot cycle has zero heat energy exchange with the environment. Hence, there is no energy loss in terms of heat in the adiabatic process. All the energy is retained within the system.

In the context of digital system, the ‘charge transfer’ process (instead of heat transfer in thermodynamics) between the power supply and the capacitive load can be adiabatic. The total charge in the given digital system is retained by energy recovery method. The charge is supplied by the power supply to the capacitive load when the bit/information is to be written and again recovered by the power supply when the bit/information is to be erased. Thus, the adiabatic digital circuit recovers the energy from the load whenever the bit/information is to be erased and hence has no ‘charge losses’. The circuits which make use of energy recovery adiabatic logic are called adiabatic circuits. Energy recovery principle can be best understood by comparing the energy dissipation in conventional CMOS circuit with that of adiabatic switching circuit. In the next section, the process of charge transfer from the power supply to the load and back to the power supply in conventional CMOS is unfolded so as to understand where exactly the energy is lost. Then, in the consequent section, energy recovery principle is explained with the help of charge transport phenomenon.
2.3.1 Energy Dissipation in Conventional CMOS

CMOS has prevailed as the technology for low power digital design so far because of its negligible static power dissipation. The leakage currents and subthreshold leakage currents give rise to a static component of CMOS power dissipation. The short circuit power dissipation is also low because it occurs for a very short time. The major contributor is dynamic power dissipation which arises from charging and discharging of a load capacitor during logic level transitions as shown in Figure 2.2.

![Figure 2.2: Charging and Discharging in CMOS Inverter](image)

The energy dissipation per input transition in CMOS is given by:

\[ E_{\text{diss}} = \frac{1}{2} CV^2 \]  

(2.2)

The equation indicates that this energy dissipation is independent of transistor size.

A CMOS inverter can be modeled as a RC circuit where NMOS and PMOS are characterized as resistors and the load as a capacitor. The charging current through this RC circuit is exponential and its magnitude is determined by the voltage drop between \( V_{DD} \) and the load capacitor. The equation for the current can be written as:

\[ i(t) = \frac{V}{R} e^{-\frac{t}{RC}} \]  

(2.3)

Where, \( R \) is the resistance of PMOS when the C is charging or the resistance of NMOS when the C is discharging. The term RC is known as circuit time constant. The instantaneous power dissipation in this FET resistor can be computed as;
The energy dissipation in a time $T$ is the integration of power from zero to $T$.

$$E_{\text{diss}} = \int_0^T P(t).dt = \int_0^T i(t)^2 R.dt = \int_0^T \frac{V^2}{R} e^{-\frac{2t}{RC}}.dt$$

$$E_{\text{diss}} = \frac{1}{2} CV^2[1 - e^{-\frac{2T}{RC}}]$$  \hspace{1cm} (2.5)

(2.5) equals (2.2) as $T$ approaches infinity. This discussion shows that the energy dissipation in the CMOS inverter is caused by the resistance of FET channels and capacitive nature of load when it is powered by a dc voltage supply.

### 2.3.2 Energy Recovery Principle

The energy dissipated in charging and discharging the load capacitor is $CV_{DD}^2$ and it is dissipated as a heat. The amount of energy lost is exactly twice the signal energy. The term signal energy refers to either the amount of energy stored on the load capacitor (output signal energy) or supplied by the load capacitor (input signal energy) to the next gate. The energy is dissipated in the PMOS or NMOS because of the resistance offered by the channel (or by the resistor in case of RC circuit) to the charge that flows from the dc power supply to the load capacitor. The energy that would be dissipated in the channel can be minimized if this charge transport in the channel is slowed down [14, 2] and this technique is called adiabatic charging. This adiabatic charging can be explained with the help a discrete solution called as ‘step charging’ [46].

**A) Step Charging:**

The analysis of energy dissipation in conventional CMOS shows that the exponential nature of charging (or discharging) current, power and energy cause $0.5CV^2$ dissipation. All these parameters are exponential in time relative to the circuit’s RC time constant. It is clear from (2.5) that the energy dissipation will reach to 97.5% of its final value after 3(RC). If a staircase voltage having a step size of $V/n$ is applied as power supply and the charging time is kept as $n(RC)$ then energy dissipation can be scaled down by $n$ times i.e.,

$$E_{\text{diss-\text{steps-charging}}} = \frac{1}{n} (E_{\text{diss-normal-charging}})$$  \hspace{1cm} (2.6)

**B) Charging with a Constant Current Source:**

As the number of steps in the staircase approach infinity, the power supply voltage generates a ramp type voltage. This ramp type voltage can be approximated as a constant current supply. Therefore, instead of using a staircase voltage
supply as mentioned in step charging, a constant current source can be used to
deliver a charge of \(CV_{DD}\) for a time \(T\). The energy dissipation will be,

\[
E_{diss} = P \times T = I^2 \times R \times T = \left(\frac{C \times V_{DD}}{T}\right)^2 \times R \times T
\]

\[
E_{diss} = \left(\frac{R \times C}{T}\right) \times C \times V_{DD}^2
\]

The above equation indicates that it is possible to reduce the energy dissipation by using a constant current source instead of constant voltage supply and by increasing charging (or discharging) time \(T\). This principle is called ‘adiabatic charging’ because the energy is not dissipated in the channel and prevented from dissipating as heat to the external world (adiabatic means without the flow of heat!). From (2.7) it is observed that;

1. If charging time is greater than \(2RC\) then the dissipated energy is smaller than that for conventional CMOS circuit.

2. Dissipated energy is inversely proportional to \(T\), which means that dissipated energy can be made arbitrarily smaller by increasing the charging time.

3. Dissipated energy is proportional to \(R\) in contrast to conventional CMOS case wherein dissipated energy depends on load capacitor and voltage swing. As charging resistance decreases, the energy dissipated decreases.

### 2.3.3 Adiabatic Logic Circuit

A simple block schematic for adiabatic charging and discharging is shown Figure 2.3.

Instead of using a separate power supply for \(V_{DD}\) and for clock, the clock signal can be reshaped and be used for both the purposes. This clock signal is called power-clock following the example of Denker [3]. Dynamically adjusting the power-clock voltage to comply with constant-current charging results in adiabatic-charging effect. A ramp type power-clock supply \(VA\) is shown in the Figure 2.3. The power-clock voltage may be sinusoidal signal also. The power-clock supply charges the load capacitor adiabatically during the time it is ramping up and allows the load capacitor energy to recycle back when it is ramping down. This adiabatic cycling of energy between the logic circuit load and the power-clock supply needs an adiabatic path. It is possible to have the same path for charging and discharging, called as temporal [3] or trivial [1] reversibility. Adiabatic circuit may have separate paths for charging and discharging as shown in
Figure 2.3. Many charge steering and pre-charge design techniques can be employed to design adiabatic circuits.

The adiabatic circuit has adiabatic loss and non-adiabatic loss in addition to leakage loss. The adiabatic loss occurs if the charge is transferred through a transistor which is turned ON. This adiabatic loss can only be avoided if the rise time of the pulsed voltage supply is at least three times the time constant of the circuit i.e. by reducing the charge transfer rate through the channel. The non-adiabatic loss occurs when there is a nonzero voltage difference between the terminals of a switch when it is being turned ON. The energy dissipated per transition can be reduced by operating the transistors according to two principles [3];

1. When the FET is OFF, the source and drain are brought to the same potential.

2. When the FET is ON, the source potential can vary while the drain floats. The variations should be sufficiently slow so that the drain with a negligible potential difference between source and drain.

Adiabatic circuits are of two types: quasi-adiabatic circuits and fully adiabatic circuits. Quasi-adiabatic circuits do have non-adiabatic loss whereas fully adiabatic circuits do not have any non-adiabatic loss. Although full adiabaticity can not be achieved as a digital system can not be isolated from the external environment completely, it can be asymptotically achieved. The fully adiabatic circuit employs reversible logic to eliminate non-adiabatic loss virtually. But the complexity of this adiabatic circuit is high because they have forward and backward logic paths due to reversible logic.
2.4 Energy Recovery Adiabatic Logic Styles

Seitz et al were the first to formulate the fundamental relationship of adiabatic principle (2.7) in early 1985 [47]. It was in 1993 that Younis and Knight practically demonstrated the reversible logic pipelines based on energy recovery principle [48] and followed by Athas [49]. They showed that it was possible to build asymptotically zero power CMOS using adiabatic techniques. They further modified their circuit technique and introduced the first fully adiabatic logic style called ‘Split-Level Charge Recovery Logic’ or popularly known as SCRL in 1994 [31]. SCRL is based on conventional, static, logic structures [1] and does not need dual rail input. A SCRL inverter and its voltage waveforms are shown in Figure 2.4.

![Figure 2.4: SCRL Inverter and Its Voltage Waveforms [1]](image)

ϕ and −ϕ are two power-clock supplies. When the SCRL inverter is in the idle condition then all the voltage waveforms i.e. power-clock, input and output are at a voltage of $V_{DD}/2$. To evaluate the inverter operation, the input $V_{in}$ is applied and then power-clock supply voltages are changed so as to apply a voltage of $V_{DD}$ as shown in the Figure 2.4. Once the valid output voltage is available the power-clock supply voltages are brought to a level of $V_{DD}/2$. The energy dissipation is reduced to 25% by this split voltage level scheme as it reduces the voltage swing to half. The drawback of this scheme is that its outputs are not compatible and the SCRL logic requires more number of clock cycles to achieve full adiabaticity. Another disadvantage of SCRL logic style is the less time available for the consequent cascaded stages to evaluate its’ logic functions.

During the same year, L. Svenssoon, and J. G. Koller proved that it is possible to reduce the energy dissipation below $0.5CV^2$ by ‘Step charging’ a capacitive load [49]. But the real momentum in adiabatic research gathered after December 1994 when William C. Athas et al developed the first adiabatic amplifier based on adiabatic switching principles in 1994 [2]. The adiabatic amplifier and its ramp type power-clock waveform are shown in Figure 2.5.
The total energy dissipated per cycle was found to be equal to;

\[ E_{\text{total}} = E_{\text{diss}} - \text{driving} - C_{\text{input}} + E_{\text{Load}} \]  \hspace{1cm} (2.8)

\[ E_{\text{diss}} = \alpha C_n V_{DD}^2 + \frac{2\xi}{T} \frac{K_n}{C_n(V_{DD} - 2V_T)} C_L V_{DD}^2 \]  \hspace{1cm} (2.9)

Where, \( \xi \) is a shape factor that takes into account a non-constant charge current (which takes the value of 1.23 for a sine-shaped current). The above equation defines the important trade-off in adiabatic CMOS circuits i.e. if the input capacitance \( C_n \) is increased then the energy dissipated in adiabatically charging the load \( E_{\text{Load}} \) decreases but the energy dissipated in charging the input increases \( (E_{\text{diss}} - \text{driving} - C_{\text{input}}) \). If \( C_n \) is a free parameter in the design, the minimum energy is achieved when both the terms are equal. Researchers also proved that the switching energy will only scale to \( T^{-0.5} \) as opposed to the \( T^{-1} \) if the input signals are conventionally driven. The desirable \( T^{-1} \) scaling can only be achieved with all-adiabatic operation, demands that the logic be fully reversible. For successful full-adiabatic approach, the overhead of storing the intermediate bits, so that they may later reversed, is more and puts additional constraints on logic implementation. Therefore, the important inference that can be drawn is that, if adiabatic switching is to be useful for achieving low-power digital design then either hybrid configuration is to be used or partial (semi/quasi) adiabatic approach is to be used.

Denker et al proposed two quasi-adiabatic logic styles 2N-2N2P [3] and 2N-2N2D [50] in 1994 based on quasi-adiabatic irreversible latches. A pair of cross coupled PMOS as shown in Figure 2.6 was used in 2N-2N2P to reduce the stranded energy on the output node to \( 0.5CV_T^2 \) as opposed to conventional \( 0.5CV^2 \). The energy on the output node capacitance discharges into power-clock through the PMOS transistor till the voltage on that node decreases to \( V_{TP} \). Therefore, only \( 0.5CV_T^2 \) energy remains stranded on that output node and rest is recovered. The idea of using PMOS to recover major portion of the total energy is still the lucrative solution. 2N-2N2D logic style deploys two diodes instead of PMOS transis-
Adiabatic Dynamic Logic (ADL) was proposed by Dickinson and Denker in 1995 [4] to overcome the drawback of the SCRL that it required sixteen times number of devices as compared to conventional logic. ADL is developed based on the application of adiabatic techniques to dynamic CMOS logic structures. ADL is not completely adiabatic (quasi-adiabatic) but delivers few order of magnitude reduction in energy dissipation. An ADL inverter and its associate waveforms are shown in Figure 2.7.

![Figure 2.6: 2N-2N2P Inverter [3]](image)

![Figure 2.7: ADL Inverter and Its Associate Waveforms [4]](image)

The ADL inverter reduces the energy dissipation and enhances the cascading ability of the adiabatic logic. But the use of diode affects its performance considerably and the energy gain is marginal.

Adiabatic Pseudo-domino Logic (APDL) designed by W. Y. Wang, K. T. Lau in 1995 was based on adiabatic theory and the CMOS domino logic (latching version) structure [5]. As per the results reported in the literature, APDL logic minimized the energy dissipation by 40% as compared to 2N-2N2D but required additional dc voltage supply. An APDL buffer/inverter and its clock supply are shown in Figure 2.8.
The concept of positive feedback was used in adiabatic logic styles called Positive Feedback Adiabatic Logic (PFAL) by Vetuli, et al in 1996 [33]. PFAL gate uses adiabatic amplifier, a latch and two NMOS transistors to avoid logic level degradation at the output. The literature survey showed that PFAL minimized the energy dissipation as compared to APDL.

Y. Moon and D-K Jeong adopted a new method that performed precharge and evaluation simultaneously and designed ‘Efficient Charge Recovery Logic (ECRL)’ in 1996 [6]. ECRL eliminated the precharge diode which were used in 2N-2N2P, 2N-2N2D, ADL and APDL and the experimental results showed that it dissipated less energy than these logic styles. ECRL has the same circuit structure as cascade voltage switch logic (CVSL) with differential signaling. An ECRL inverter and its power-clock supply are depicted in Figure 2.9. The high ‘in’ signal pulls the ‘out’ node at ground potential and the PMOS transistor P2 adiabatically charges and discharges the ‘out’ node.

An inverter chain and a pipelined carry lookahead (CLA) adder were used as benchmark circuits to show the effectiveness of the ECRL adiabatic logic style. ECRL needed four-phase clocking for the efficient energy recovery. Researchers used a LC resonant circuit which performed like a Colpitts oscillator as a supply clock generator. It consisted of one inductor and two capacitors with MOS switches. The Power gain of 16-bit ECRL CLA adder over conventional CMOS was 56% and it was reported that ECRL also outperformed 2N-2N2D in terms of energy consumption.

M. C. Knapp, et al studied the performance of 4X4 bit adiabatic multiplier against that of conventional CMOS [51] and showed that adiabatic circuits have large latencies due to the dynamic nature of their gates. Although it was possible to build adiabatic memory elements, these elements had a latency of one clock cycle. Therefore M. C. Knapp, et al concluded that adiabatic technology is more
Figure 2.9: ECRL Inverter and Its Power-clock Supply [6]

effective for low speed, combinational circuits.

Pass-transistor Adiabatic Logic was designed by V. G. Oklobdzija, et al in 1997 [7]. PAL uses only one single sinusoidal power-clock supply and is dual-rail logic. A PAL gate consists of true and complementary NMOS functional blocks as shown in Figure 2.10. Whenever the logic block ‘F’ evaluates the function, the power-clock adiabatically charges and discharges the ‘out’ node. The pair of cross-coupled PMOS transistors comprised of P1 and P2 maintains the dual-rail output.

Figure 2.10: PAL Logic Structure [7]

PAL has simple implementation and relatively low gate count. As per the results reported in the research paper [7] PAL outperformed 2N-2N2D and ADL.
The maximum frequency of PAL 2:1 multiplexer was reported as 160MHz when designed with 1.2µm transistors and operated by peak to peak power-clock supply of 3.0V. The major drawback of PAL adiabatic circuit was that its' outputs were ‘tri-stated’ when the circuit was not evaluating. This drawback was removed in PAL with NMOS pull-down configuration. The modified PAL was called PAL-2N [12] and the comparison between energy dissipation of PAL-2N shift register and that of PAL showed that the PAL-2N dissipated more energy.

Another adiabatic logic style called ‘Clocked CMOS Adiabatic Logic (CAL)’ developed by D. Maksimovic, et al in 1997 can be operated in adiabatic and non-adiabatic modes [8]. It was operated from single-phase power-clock supply in adiabatic mode and from a dc power supply in non-adiabatic mode. A generalized CAL structure is shown in Figure 2.11.

![CAL Logic Structure](image)

The performance of CAL logic circuit against other adiabatic logic styles does not seem to be available. The comparison of CAL chain of inverters in adiabatic and non-adiabatic mode showed significant energy savings in adiabatic mode at relatively low clock rates up to 12.5MHz. Researchers designed the on-chip power-clock supply. The energy dissipated in the power-clock supply and hence the efficiency of the on-chip power-clock supply was not computed.

A 5X5 ternary digit multiplier was designed based on the Quasi-Adiabatic Ternary CMOS Logic (QAT-CMOS) by Diego Mateo and Antonio Rubio in 1998 [32]. QAT-CMOS logic consumed less silicon area as compared to then previously published adiabatic logic styles. The performance evaluation of QAT-CMOS 5X5 trits (using ternary logic) multiplier against CMOS 8X8 multiplier showed 90% reduction in energy dissipation and 1.5 times increase in silicon area. The comparison with other quasi-adiabatic logic styles showed that QAT-CMOS dissipated less energy and consumed less than 50% silicon area. QAT-CMOS logic con-
sumed more energy dissipation as compared to SCRL. The major drawbacks of the ternary implementation reported in the literature were; the requirements of three voltage levels to represent three logic levels and complex power-clock supply. Researchers selected supply voltage of 5V for CMOS and other adiabatic logic styles and maximum supply voltage of 3.2V for their QAT-CMOS. This made the comparative study weak.

Another full-adiabatic logic circuit was designed by J. Lim, et al in 1998 and was called ‘Reversible Energy Recovery Logic (RERL)’ [52]. It was also referred to as ‘tRERL’ since it used transmission gates as logic switches for charge transport. tRERL eliminated the non-adiabatic loss occurring due to degraded ‘High’ level across the NMOS logic switch but it was reported that it consumed eight times more silicon area as compared to CMOS.

Same researchers used the concept of bootstrapping to eliminate the non-adiabatic loss as well as to minimize the silicon area. The new full adiabatic logic style was called ‘Bootstrapped RERL’ or ‘bRERL’ [9]. bRERL used a bootstrapped NMOS switch as a logic switch instead of transmission gates reducing the silicon area consumed by transmission gates. The non-zero voltage problem across a NMOS due to degraded ‘high’ signal caused non-adiabatic losses and this problem was solved in NMOS bootstrap switch. The experimental results showed that bRERL consumed less energy as compared to tRERL. Figure 2.12 shows the bootstrapped switch and its waveforms. The point ‘G’ is bootstrapped above $V_{DD+} + V_{THB}$ and the output follows exactly without the threshold voltage drop.

But the problems associated with full-adiabatic circuits like multi-phase power-clock supply and requirement of more number of clock ticks to recover energy completely were also observed in tRERL. Researchers then further refined their bRERL logic and designed a new fully reversible logic style which used NMOS transistors only and the bootstrapping principle. It was aptly called ‘nRERL’ [35]. As per the experiments conducted by the researchers on a 2400 stage nRERL inverter chain (operated at 3.5V), it consumed 48% energy as compared to CMOS circuit driven by 1.15V. Bootstrap circuits did not have a signal restoration capability. It was also reported that at higher frequencies when there was a voltage drop on the on-resistance of the bootstrapped transistor, the degraded output level diminished the bootstrap efficiency of the next gate and the operation of the logic failed [35].

Quasi-Static Energy Recovery Logic (QSERL) designed by Y. Ye and Kaushik Roy in 2001 was designed to reduce the switching activity of the adiabatic circuit as it resembled behavior of static CMOS [10]. Circuit nodes do not charge and discharge every clock cycle which reduces the switching activity. A generalized QSERL adiabatic logic structure is shown in Figure 2.13. QSERL was based
Figure 2.12: Bootstrapped Switch and Its Waveforms [9]

Figure 2.13: QSERL Logic Structure [10]
on static CMOS gate with two additional diodes, \( P_d \) and \( N_d \). It required two sinusoidal clocks in complementary phases. Simulation on eight inverter chain resulted into 50% energy savings at 100MHz compared to static CMOS. It was observed that the use of diodes or diode like structures increased the non-adiabatic losses considerably and had the possibility of increasing leakage loss as well.

In the same year (2001) an ‘Improved Pass-Gate Adiabatic Logic (IPGL)’ was introduced by L. Varga, et al [11]. IPGL claimed to minimize the non-adiabatic loss during the charge phase. The IPGL gate eliminated non-adiabatic loss, caused by the threshold voltage drop, with the use of NMOS logic blocks parallel with the pair of PMOS transistors. However, in the discharge phase, the output node retain a \( V_T \) voltage as the cross coupled PMOS transistors are shut off. Thus, the energy recovery was incomplete. The simulation results showed that IPGL performed better than CMOS from the energy minimization point of view. L. Varga, et al added two more NMOS so as to recover the energy completely. The schematic of IPGL gate with complete recovery path is shown in Figure 2.14. NMOS transistor is connected between the output node and power-clock to provide complete charge recovery. The inputs of these two NMOS are driven by the logic gate in next phase. The experimental results on a chain of 100 IPGL inverters indicated 50% energy reduction over similar chain of inverters implemented using 2N2N2P. It seems that there are no published results which compare IPGL with PAL, PAL-2N, CAL etc. The area penalty of introducing four logic blocks (two ‘F’ and two ‘F’ logic blocks) is high i.e. number of gates are at least two times that of other quasi-adiabatic logic styles.

![Figure 2.14: IPGL Gate With Complete Recovery Path](image)

Two more quasi-adiabatic logic styles based on cross coupled PMOS transis-
tors viz. ‘True Single-Phase Energy-Recovery Logic’ (TSEL) and ‘Source Coupled Adiabatic Logic’ (SCAL) were proposed by S. Kim and M. C. Papaefthymiou [53]. TSEL and SCAL adders outperformed the corresponding designs in static CMOS and 2N2P. Researchers also used 8X8 multiplier as benchmark circuit [54].

Three more adiabatic logic styles were introduced viz. ‘High Efficient Energy recovery Logic’ (HEERL) by D. Hongyu, et al [55] and ‘Dual Transmission Gate Adiabatic Logic’ (DTGL) by J. Hu, et al [56] and ‘Adiabatic Differential Voltage Switch Logic’ (ADVSL) by Q. Yang et al [57]. All three used the concept of cross coupled PMOS transistors. DTGL used dual gate transmission gate to eliminate non-adiabatic loss. The experimental simulated results indicated that DTGL inverter and 8X8 multiplier dissipated less energy as compared to ECRL adiabatic circuit. ADVSL required multi-phase clocking scheme and it seems that the energy penalty in generating multi-phase clock was not calculated by the researchers.

Table 2.1 summarises the performances of some adiabatic logic styles as reported in the literature. These studies have been carried out discretely and do not really depict a good picture for comparison. There is a need to do further study these aspects on a common platform which is one of the objectives of this research work.

2.5 Adiabatic Circuits

A few research papers are available on IEEE, IET and DELNET database which report the results of various experiments performed on adiabatic benchmark circuits. In this section, the literature survey of these papers is presented.

M. C Knapp, et al studied the performance of 4X4 bit adiabatic multiplier against that of conventional CMOS [54] and showed that adiabatic circuits have large latencies (i.e. output lags three to five phase delays after the input signal) due to the dynamic nature of their gates. They observed that adiabatic memory elements had a latency of one clock cycle and hence they concluded that adiabatic technology was more effective for low speed, combinational circuits.

M. Alioto, et al evaluated the performance of adiabatic gates and their analysis indicated that additional reversible logic circuit required in full-adiabatic circuit increased power dissipation and complexity of the adiabatic circuit [58]. These were among the first few researchers who emphasized on quasi-adiabatic logic styles for their practical advantages like less complex logic structure, less silicon area at the price of additional non-adiabatic loss. Their experiments indicated that 2N-2P and 2N-2N2P do not perform well at the gate level.

The method of evaluating power consumption in adiabatic circuits based on linear modeling was proposed in 2000 by Alioto and G. Palumbo [59]. Re-
Table 2.1: Summary of Performance of Some Adiabatic Logic Styles

<table>
<thead>
<tr>
<th>Sr No</th>
<th>Logic Style</th>
<th>Compared With</th>
<th>Technology ($\mu m$)</th>
<th>Benchmark Circuit</th>
<th>Change in $E_{Diss}$ %</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SCRL</td>
<td>CMOS</td>
<td>-</td>
<td>Inverter</td>
<td>-75</td>
</tr>
<tr>
<td>2</td>
<td>ADL</td>
<td>CMOS</td>
<td>0.9</td>
<td>Inverter</td>
<td>-90</td>
</tr>
<tr>
<td>3</td>
<td>APDL</td>
<td>CMOS</td>
<td>0.8</td>
<td>4-Bit shift register</td>
<td>-80</td>
</tr>
<tr>
<td>4</td>
<td>ECRL</td>
<td>CMOS</td>
<td>1.0</td>
<td>Inverter chain</td>
<td>-95</td>
</tr>
<tr>
<td>5</td>
<td>ECRL</td>
<td>CMOS</td>
<td>1.0</td>
<td>16-bit CLA</td>
<td>-56</td>
</tr>
<tr>
<td>6</td>
<td>PAL</td>
<td>2N2D</td>
<td>1.2</td>
<td>1600 Stage shift register</td>
<td>-50</td>
</tr>
<tr>
<td>7</td>
<td>PAL2N</td>
<td>2N2N2P</td>
<td>0.8</td>
<td>2:1 Multiplexers</td>
<td>-33</td>
</tr>
<tr>
<td>8</td>
<td>PAL2N</td>
<td>PAL</td>
<td>0.8</td>
<td>2:1 Multiplexers</td>
<td>+6</td>
</tr>
<tr>
<td>9</td>
<td>CAL</td>
<td>Non-adiabatic operation</td>
<td>1.2</td>
<td>Chain of 736 inverters</td>
<td>-66</td>
</tr>
<tr>
<td>10</td>
<td>QAT-CMOS</td>
<td>CMOS</td>
<td>0.7</td>
<td>8X8 Multiplier</td>
<td>-90</td>
</tr>
<tr>
<td>11</td>
<td>bRERL</td>
<td>CMOS</td>
<td>0.6</td>
<td>Chain of 512 inverters</td>
<td>-85</td>
</tr>
<tr>
<td>12</td>
<td>nRERL</td>
<td>CMOS</td>
<td>0.8</td>
<td>Chain 04 2400 inverters</td>
<td>-48</td>
</tr>
<tr>
<td>13</td>
<td>QSERL</td>
<td>CMOS</td>
<td>-</td>
<td>Chain of 8 inverters</td>
<td>-50</td>
</tr>
<tr>
<td>14</td>
<td>IPGL</td>
<td>2N2N2P</td>
<td>-</td>
<td>Chain of 100 inverters</td>
<td>-85</td>
</tr>
<tr>
<td>15</td>
<td>SCAL</td>
<td>CMOS</td>
<td>0.5</td>
<td>8-Bit multiplier</td>
<td>-55</td>
</tr>
</tbody>
</table>
searchers used linear modeling technique to represent each adiabatic gate by a resistor and two capacitances at the two nodes. Their simple mathematical model evaluated the energy consumption of adiabatic circuits with worst case error of 7%. One more research paper from the same researchers on power estimation in adiabatic circuits [60] reported the accuracy of their model as 20% and this showed improvement in their own model which indicated 7% accuracy in the previously published paper.

D. Soudris, et al used pass transistors to design adiabatic adders and presented a formula to find out a delay in the carry select adder [61]. Many researchers have used the adder circuit for benchmarking or testing adiabatic logic [53],[61, 62, 63, 64, 65, 66, 67, 68, 69, 70]. An adiabatic circuit based on energy recovery flip-flop circuit presented by C. Ziesler, et al [71] reduced the dissipation in clock tree and state elements. Researchers claimed that their design eliminated the need of clock gating approach and reduced the energy by a factor of four as compared to conventional CMOS.

M. Alioto and G. Palumbo, in their third paper on evaluation of power consumption in adiabatic circuits, showed that the power advantage of adiabatic diminished when the complexity of the implemented Boolean function was increased [72]. The simulated results of their experiment indicated that the adiabatic style was advantageous at frequencies lower than 30MHz and if the fan-out of the adiabatic circuit was five then the power advantage drastically reduced to frequencies below 1MHz.

E. Amirante, et al tested the performance of PFAL 0.25\(\mu\)m inverter gate against threshold voltage variations. The experimental results proved that the power variations could reach up to 20% for threshold voltage variations as low as 50mV [73]. Another experiment on 8-bit CLA circuit using 0.35\(\mu\)m technology had shown that full-adiabatic circuit (nRERL) saved energy dissipation up to 71% as compared to conventional CMOS [74].

The research papers on power-clock generation [75, 76, 77] report that the design, implementation and energy-efficiency of these circuits/systems are some of the hindrances in the commercialization of the adiabatic circuit. All these power-clock generation circuits use LC based resonant circuit to generate sinusoidal power-clock signal. The ramp type (used in CAL) and triangular shape (used in ADL,CPERL and APDL) of power-clock signals are not being used by the researchers nowadays for the need of additional wave shaping circuits. Some adiabatic logic styles viz. SCRL, bRERL, ECRL, require multi-phase clock supply to feed the energy back to the supply whereas some adiabatic logic styles require two-phase clocking e.g. QATCMOSL, QSEL etc.

PAL and TSEL use single-phase power clock supply for adiabatic charging and discharging in case a combinational circuit of low complexity is being implemented. If the application demands cascading of multiple functional blocks then
two phase non-overlapping clocking is required for PAL logic style. The scheme for single-phase and two phase non-overlapping power-clock generation is simpler than multi-phase clocking generation schemes. In terms of energy-efficiency (i.e. the ratio of the energy dissipated in generating the power-clock supply to the energy dissipated in adiabatic circuits), single-phase driven adiabatic circuits appear to be the optimal possible option. The experimental data is not available to compare the energy-efficiency of these power clock supply generation circuits.

2.6 Towards Research Objectives

Following inferences can be drawn from the above literature survey;

1. Energy recovery adiabatic technique achieves sub-0.5$C V^2$ energy dissipations and estimation of the energy dissipations is highly accurate due to more elaborately defined MOSFET models.

2. Full-adiabatic circuits like SCRL, RERL go long way towards achieving adiabatic operation. However the complex clocking scheme, low throughput of the retractile cascades and the logic overhead of the full reversible pipelines are the major practical barriers. In this context, quasi-adiabatic approach offers the simplicity of the adiabatic operation and functionality of the CMOS.

3. Quasi-adiabatic logic styles viz. 2N2P, 2N-2N2P, PAL, CAL, and PAL-2N which use cross coupled inverters (like conventional latch) or cross coupled PMOS transistors are more practical circuits as these reduce the complexity of the quasi-adiabatic circuit at the cost of little non-adiabatic loss ($\approx CV_{DD}V_T$). It appears that there is a possibility of improving the performance of such quasi-adiabatic circuits, in terms of energy dissipation and delay, by using circuit techniques.

The following research gaps can also be identified from the literature survey;

1. To test the new quasi-adiabatic logic style for robustness. Many researchers have preferred to design a complex circuit using adiabatic logic but the characterization study of quasi-adiabatic logic style behavior in adverse conditions is not cited in the literature. Hence, this research work proposes to study the effect of noise and jitter on the quasi-adiabatic logic style.

2. To put design efforts to reduce the leakage power dissipation in quasi-adiabatic circuits. Efforts in this direction by the researchers do not seem to have taken so far.
3. Finally, the researcher strongly feels that ‘ASIC design using only quasi-adiabatic logic style’ is not possible due to the low speeds of operation of the adiabatic logic and larger silicon area consumed by it. A practical low power digital design solution is the hybridization of CMOS and quasi-adiabatic logic style. Again, the research work in this direction is not cited in the literature. Therefore, this research work proposes to study the design issues in making outputs of quasi-adiabatic circuits compatible with CMOS signal levels.

Based on the above inferences and research gaps it was proposed to:

1. Compare various quasi-adiabatic logic styles already reported in the literature for power consumption and energy-delay product using one common platform of 180 nm technology since the reported results from literature are on adiabatic circuits developed at different times and hence of different technologies.

2. Select and hypothesize a suitable quasi-adiabatic MOS logic style for a typical digital circuit and experimentally prove that it is superior to conventional optimized CMOS logic styles.

3. Propose and demonstrate a way to reduce leakage power dissipation in quasi-adiabatic logic and develop a boundary circuit which would act as interface between adiabatic logic and CMOS logic.

The subsequent chapters of this thesis explain the details of various experiments performed by simulation using Cadence ASIC design suite and the inferences thereof.