Chapter 6

RESEARCH CONTRIBUTIONS IN QUASI-ADIABATIC CIRCUIT THEORY

The objective of this research work was to minimize the power dissipation in digital system using energy recovery adiabatic logic. Quasi-adiabatic circuit theory was used to achieve low power design objective and the proposed new quasi-adiabatic logic style, ‘PAL2NSM’ proved to be superior quasi-adiabatic logic style in terms of minimizing the energy dissipation and producing clean output. In the quest of reducing the energy dissipation of this logic style further, the research work was carried out in minimizing the leakage power dissipation. The traditional leakage reduction techniques were not found suitable in quasi-adiabatic theory due to the nature of the signals. The experimentation work was carried out in this direction so that leakage power in the quasi-adiabatic circuit can be dynamically minimized. The research work was also carried out to design boundary circuits between adiabatic circuits and CMOS circuits. These two totally new research contributions made in quasi-adiabatic theory viz. ‘Leakage Power Reduction in Quasi-adiabatic Circuit’ and ‘Partially Reversible Boundary Circuit between Quasi-adiabatic and CMOS Circuits’ are presented in this chapter.

6.1 Leakage Power Reduction in Quasi-adiabatic Circuit

The dependence of threshold voltage $V_T$ of a MOS transistor on Bulk-to-Source voltage, $V_{SB}$ is given by,
\[ V_T = V_{T0} + \gamma \sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \]  \hspace{1cm} (6.1)

where the different terms in this equation have usual meaning. This effect is called as Body Effect. This equation indicates that the substrate bias can be varied to steer the threshold voltage of a MOS device. The power dissipation due to leakage is a strong function of threshold voltage. Higher the threshold voltage lower is the leakage dissipation. The approach used in low power CMOS designs is to use low threshold voltage transistors in active mode, thereby reducing the supply voltage requirement and hence reducing the dynamic power dissipation, while high threshold voltage transistors in stand-by mode reducing the leakage power dissipation. The low leakage mode is achieved by ‘active well’ control using the body effect. The well potentials of PMOS and NMOS transistors are altered above \( V_{DD} \) and below \( V_{SS} \) respectively to increase the threshold voltage of the two transistors.

Switched Source Impedance (SSI) CMOS technique [13] shown in Figure 6.1 has been introduced by the researchers for this purpose. Here, switched impedance is set at the source of NMOS/PMOS transistor in parallel with one NMOS/PMOS switch. The switch is turned ON in the active mode and turned OFF in the standby mode. When turned ON, the switch brings the source to the ground potential and \( V_{SB} \) becomes zero. When the switch is turned OFF, the potential drop across the resistor brings the source at a higher potential and maintains the bulk at ground potential. This applies a positive \( V_{SB} \) and increases the threshold voltage. Though this technique resulted in reducing the leakage power dissipation, the additional power dissipation taking place in the switch during active mode and in the resistor while in stand-by mode was unavoidable.

![Switched Source Impedance (SSI) CMOS technique](image.png)

Figure 6.1: Switched Source Impedance (SSI) CMOS technique [13]

To eliminate this additional power loss in the standby mode, a new concept of
shifted ground is proposed. We tested the concept on one of the quasi-adiabatic circuits viz. a CAL inverter to prove conclusively that this approach leads to about 50% reduction in power dissipation. The details of the quasi-adiabatic CAL inverter and sub-adiabatic CAL inverter are presented in the next section. The basic circuit schematic of CAL inverter is as shown in Figure 6.2. The working of CAL logic style is already presented in Chapter 4.

![Figure 6.2: Circuit Schematic of CAL Inverter](image)

The simulation results indicated an energy dissipation of about 36 pJ after 320ns with $V_{DD}$ of 3V. This is a reference parameter for comparison after applying the proposed new approach. It should be noted that though inverter was used as a benchmark circuit for this exercise, any combinational circuit could replace transistor MN1 and MN4 of the inverter to design quasi-adiabatic circuits of desired logic function.

Figure 6.3 depicts the above CAL inverter with NMOS and PMOS transistors of same dimensions with only difference that substrates of PMOS transistors (‘VBS_PMOS’) and those of NMOS transistors (‘VBS_NMOS’) forming the required logic were connected to a variable DC supply. The ‘F0’ and ‘F0bar’ inputs are of ramp-type. Here, it is necessary to ensure that ‘F0’ input does not make transitions during the Evaluation, and Recovery phase. The other input, ‘CX’ is a pulse input as mentioned above. This inverter was simulated with same operating conditions viz. $V_{DD}$=3V and transient analysis time of 320 ns.
The following variations were implemented in simulation runs as is seen from TABLE 6.1. The figures for energy dissipation in this table were calculated using Spectre tool of Cadence.

1. Conventional substrate biasing viz. $V_{BS\_PMOS}$ at $V_{DD}$ and $V_{BS\_NMOS}$ at ground (zero) potential.
2. Varying substrate biasing of PMOS by keeping $V_{BS\_NMOS}$ at ground voltage.
3. Varying substrate biasing of NMOS by keeping $V_{BS\_PMOS}$ at $V_{DD}$.
4. Keeping the substrate bias for PMOS transistors at twice $V_{DD}$ and substrate bias for NMOS transistor at $-V_{DD}$.
5. It is noted that the circuit does not generate valid output when $V_{BS\_PMOS} < 3V$ and $V_{BS\_NMOS} > 2V$.

The results indicated that NMOS substrate biasing had profound effect on energy dissipation as compared to that of PMOS substrate biasing. This may be due to the fact that the circuit has three times more number of NMOS transistors.
Table 6.1: Effect of $V_{BS}$ Variations on Energy Dissipation

<table>
<thead>
<tr>
<th>VBS_PMOS (V)</th>
<th>VBS_NMOS (V)</th>
<th>Energy Dissipated (pJ)</th>
<th>Energy Gain over Conventional Biasing %</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>0</td>
<td>15.64</td>
<td>–</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>12.58</td>
<td>20</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>9.26</td>
<td>41</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>7.06</td>
<td>55</td>
</tr>
<tr>
<td>3</td>
<td>-1</td>
<td>9.56</td>
<td>39</td>
</tr>
<tr>
<td>3</td>
<td>-2</td>
<td>6.72</td>
<td>57</td>
</tr>
<tr>
<td>3</td>
<td>-3</td>
<td>5.13</td>
<td>67</td>
</tr>
<tr>
<td>6</td>
<td>-3</td>
<td>1.52</td>
<td>90</td>
</tr>
</tbody>
</table>

than PMOS transistors and this may be true for all quasi-adiabatic circuits which implement logic function using NMOS tree. About ten times less energy was dissipated if $V_{BS}$ for PMOS and $V_{BS}$ for NMOS were kept at 6V and -3V respectively. Though the simulation results indicated that this test condition was the most promising one, a practically working approach would be with $V_{BS}$ for PMOS at $V_{DD}$ and $V_{BS}$ for NMOS at about -1V. With this $V_{BS}$ values the circuit gave about 39 % reduction in energy dissipation w.r.t. conventional bulk-to-substrate biasing approach as is evident from the Table 6.1.

Instead of giving negative bias to the substrate of NMOS, shifted ground concept was implemented where the substrate was always at the ground potential $V_{SS}$ but source was elevated in potential by 1V. The bulk was connected to 1V dc during the active mode making the $V_{SB}=0V$. As soon as the circuit stopped evaluating the Boolean expression the circuit was switched to stand-by mode and the bulks were connected to zero potential making $V_{BS}=-1V$ or $V_{SB}=1V$. This increased the threshold voltage and reduced the leakage power dissipation. Further, this approach was used in the stand-by mode only while usual conventional substrate biasing ($V_{BS}$ for PMOS at $V_{DD}$ and $V_{BS}$ for NMOS at $V_{SS}$) in active mode was used. Thus, the substrate potentials of the PMOS and NMOS were switched simultaneously to appropriate potentials depending upon the stand-by or active mode.

### 6.1.1 Control Circuits for Switching Purpose

A separate control circuit is required to apply conventional bulk-source bias when the circuit is in the active mode and to apply ‘ground-shifted $V_{BS}$ for NMOS’ in the stand by mode. Three different control circuits with their performance de-
tails are presented below.

1. **Pass Transistor Based Circuit:**

Two pass transistors can be used to dynamically select the $V_{BS}$ for NMOS as shown in Figure 6.4a. The corresponding bulk-source biasing voltage waveform, $V_{BS}$ is shown by waveform ‘a’ in the waveform pane. Whenever the logic block ‘F’ is evaluating the function, the output signal ‘F1’ goes to logic ‘1’. In quasi-adiabatic circuits, the output signal follows the power-clock signal as long as the circuit is evaluating the given function or it is in the active mode. This is shown in the waveform pane as ‘F1’ output. The same output signal can be used to operate the circuit of Figure 6.3 in active mode or standby mode as required. The voltage at ‘vss1’ was kept at 1V while that at ‘GND’ at zero volts. The drawback of this circuit is that there would be additional energy dissipation in pass transistors. However this can be minimized using the minimum sized transistors. When the CAL circuit was tested with this control circuit (with pass transistor length and width of 180nm and 400 nm respectively), the energy dissipation was reduced from 46pJ in the active mode to 40pJ in the standby mode over a transient analysis time of 500ns which gave a gain of 13%. In more complex quasi-adiabatic circuits, the energy gain will be more and it will compensate for the energy loss in the pass transistors.

2. **Additional XNOR Based Wave Shaping Circuits:**

The $V_{SB}$ biasing voltage as generated by the control circuit in Figure 6.4a is not a steady waveform and it varies largely with the power-clock supply variations. An additional wave-shaping circuit is required. A simple wave-shaping circuit based on ‘XNOR’ing the /PC and /F1 signal is shown in Figure 6.4b. The XNOR logic was implemented using conventional CMOS logic gates and the corresponding bulk-source biasing voltage waveform, $V_{SB}$ is shown by waveform ‘b’ in the waveform pane. It can be observed that the $V_{SB}$ biasing voltage is not varying in either active or in passive mode. The delay penalty caused by the wave-shaping circuit in generating the $V_{SB}$ may be ignored as it would reduce the standby time by a small amount and still the energy gain would be high. But the energy overheads of this control circuit would be appreciable because of large number of transistors required to implement XNOR logic. This energy dissipation penalty can be reduced if the wave-shaping circuit is implemented using pass transistors as

159
shown in Figure 6.4c. The circuit consists of less number of transistors and produces slightly degraded but still an acceptable $V_{SB}$. The corresponding bulk-source biasing voltage waveform, $V_{SB}$ is shown by waveform ‘c’ in the waveform pane. The same circuit is interfaced with PAL2NSM 2:1 MUX and tested. The circuit schematic is shown in Figure 6.5.

Ten transistors were required to implement the control circuit shown in Figure 6.4c. Instead of XNORing the /PC and /out signals, a simple multiplexing of the two $V_{SB}$ voltages (1V and 0V) using /mode and /modebar signals can be also used for the leakage power control. This circuit requires only two transistors. Moreover, it reduces power dissipation further as mode signal is a low frequency signal as compared to ‘PC’ and ‘out’.

6.1.2 Conclusions and Remarks

1. Energy recovery adiabatic circuit is a solution for reducing dynamic power dissipation. PAL2NSM is designed with the objective of reducing the dynamic power dissipation further and for achieving adiabatic dissipation levels. PAL2NSM is made to work in sub-adiabatic mode by monitoring the substrate bias so as to reduce the leakage dissipation in the stand-by mode.

2. The new ‘shifted ground concept’ of reducing leakage power resulted in
about 39% reduction in power dissipation for CAL inverter. This concept of leakage power reduction can be applied to all quasi-adiabatic circuit without any change in the control circuit design.

3. The immunity to ground noise may improve as the circuit works on an elevated ground voltage.

4. Appreciable reduction can be achieved in more complex adiabatic circuits because of the reduced overheads of additional circuitry implemented to do the switching.

5. The energy dissipation was further reduced by multiplexing $V_{SB}$ voltages with the help of mode signals and in the case of PAL2NSM circuit it was reduced by 1%.

6.2 Partially Reversible Boundary Circuit Between Quasi-adiabatic and CMOS

The simulation results and discussions from Chapter 4 lead to a conclusion that the adiabatic circuits can be used for low power low speed applications. Quasi-adiabatic circuit techniques can be used to design a low frequency functional block
in a CMOS based digital system. This hybrid approach can reduce the overall energy dissipation of the digital system. But the outputs of quasi-adiabatic circuits are not conventional CMOS logic levels and interfacing of these two logic styles need a boundary circuit which will achieve the compatibility between these two types of signals. A boundary circuit which interfaces a quasi-adiabatic logic style driven by a sinusoidal power-clock supply to a conventional CMOS is presented in this section. The charge flow through the boundary circuit is analyzed to check the reversibility of energy from the input capacitance of the boundary circuit to the power-clock supply.

### 6.2.1 Design of Boundary Circuit

XNORing of power-clock signal with the output signal i.e. ‘out’ can produce a CMOS compatible waveform. This has been shown in the previous section. Before designing such a boundary circuit, it is better to check whether the recycling of energy from the load capacitance (input capacitance of the boundary circuit) to power-clock supply of adiabatic circuit is possible or not. The circuit diagram and its paper (hand)-analysis showed that the partial reversibility of energy is possible, although, the energy transfer from boundary circuit to CMOS circuit was obviously going to be non-adiabatic.

The hand analysis shows that the ‘OUT’ signal drives the gate capacitances of the PMOS and NMOS at the input pin of the boundary circuit. Note that the boundary circuit is a CMOS based design and so; every input of it is connected to at least one PMOS-NMOS pair. This interfacing is shown in Figure 6.6. The controlling charge varies adiabatically and controls the charge flowing through the channel. The charge transfer from the power-clock to these capacitances is quasi-adiabatic and hence there is reversibility of energy between these two. The reversibility is shown in the Figure 6.7. The waveform /PM34/D depict the current flow at the input NMOS transistor. It shows positive current flow as well as negative current flow.

It was also expected that the current through the NMOS (measured at the source) would be higher when it would start conducting as compared to the current through it when it would stop conducting. The current through the NMOS is shown in Figure 6.8. This happens because the current through the NMOS is contributed by the adiabatic charging through ‘OUT’ signal as well as the non-adiabatic discharge of the capacitor connected to its drain.

When the /out is at logic low, the gate charge on the PMOS varies sinusoidal. The output at the PMOS charges through the P-channel. When the /out goes high (>VTH), NMOS turns on. The charge supplied by /out now controls the gate capacitance of NMOS and the output at NMOS discharges through the channel.
Figure 6.6: Interfacing of the Boundary Circuit and PAL2NSM 2:1 MUX

Figure 6.7: Current through the NMOS Gate Showing Reversal of Energy
of NMOS. Since the two charges are isolated it can be concluded that the charge transfer from /out to the gate capacitances of PMOS and NMOS is reversible and their charge is being recovered by the power-clock supply. The other part of the boundary circuit dissipates energy as observed in conventional CMOS. Since the boundary circuit is designed using conventional CMOS circuit style, it is not possible to recover the load capacitance energy of the boundary circuit.

The XNOR based boundary circuit is shown in Figure 6.9 and its actual circuit schematic in Figure 6.10 below,
adiabatic circuit. The /PC is sinusoidal.

The simulated input-output waveforms are shown in Figure 6.11. Note the /out signal which shows the replica of the /PC signal when the output of the PAL2NSM circuit is at logic high. The CMOS compatible output /CMOSout is shown in the first waveform. It was observed that an unwanted logic high (glitch) was produced during the period when the negative cycle of PC and the /out was at logic zero. The glitch appears in the output of the boundary circuit /CMOSout because the negative cycle of the /PC is treated as logic zero and hence the XNOR circuit produces the logic high output whenever /out and /PC has a negative cycle (logic zero). This glitch is shown in Figure 6.12.

It is possible to remove this glitch with the help of one D flip-flop as shown in Figure 6.13. Here, we have used negative edge triggered D flip-flop. CMOS output signal of the boundary circuit is given as an input to the D flip-flop which is triggered on a falling edge of the clock. The frequency of the clock signal is same as the frequency of power-clock signal. The glitch which is observed in the ’/CMOSout’ signal is completely removed by the addition of D flip-flop in the boundary circuit. The circuit schematic of the refined boundary circuit is shown in Figure 6.14.

Here, the /Q output signal is the desired CMOS level output signal. This is
Figure 6.11: Simulated Input-output Waveforms of XNOR Based Boundary Circuit

Figure 6.12: Glitch in the Output of the Boundary Circuit
Figure 6.13: Refined Boundary Circuit

Figure 6.14: Virtuoso Circuit Schematic of the Refined Boundary Circuit
shown in Figure 6.15. The addition of the D flip-flop has introduced a negligible propagation delay of 200ps as can be observed from the two waveforms viz. /CMOSout and /Q.

6.2.2 Effectiveness of the New Boundary Circuit

1. Adiabatic circuits are used to minimize the energy dissipation and the effectiveness or efficiency of the adiabatic circuit is governed by three major factors viz. energy dissipation, delay and silicon area consumed by the adiabatic circuit. Any additional circuit designed for improving the performance of the adiabatic circuit should consume lowest possible energy and silicon area.

2. XNOR based boundary circuit is a generic boundary circuit which uses 18 transistors (L=180nm and W=2µm). The circuit works well with all types of power-clock supplies except for sinusoidal power-clock supply. A glitch is generated by the XNOR based boundary circuit when a sinusoidal power-clock supply is used. Therefore for non-sinusoidal power-clock supply driven adiabatic circuit; XNOR-based boundary circuit without D flip-
flop is the simplest, generic and effective design solution. The D flip-flop based solution assumes the availability of a conventional clock signal having a frequency same as that of power-clock signal. Usually this conventional clock signal has a very high frequency compared to the frequency of power-clock signal (which has constraint $T > 3RC$ to ensure adiabaticity) of the adiabatic circuit. The frequency divider circuit is needed to convert high frequency conventional clock signal to low frequency (equal to frequency of sinusoidal power-clock signal) conventional clock signal. This one more additional circuit will reduce the energy efficiency of the boundary circuit.

3. For adiabatic circuits which are driven by sinusoidal power-clock supply, D flip-flop based boundary circuit may offer minimum energy dissipation as it uses only 16 transistors ($L=180\text{nm}$ and $W=2\mu\text{m}$) but there would be additional energy dissipation and area penalty caused by the frequency divider circuit.

4. Finally, XNOR-based circuit without D flip-flop can be used as a generic low power boundary circuit. The D flip-flop based circuit is useful for designing boundary circuit for sinusoidal power-clock driven adiabatic circuits.

6.2.3 Conclusion and Remarks

1. This circuit is able to produce a logic signal which is compatible to conventional CMOS circuit. The analysis of charge flow between the adiabatic and boundary circuit indicated the partial reversibility. Hence the energy injected into the input gate capacitance of the boundary circuit by the adiabatic output signal can be recovered by the power-clock supply.

2. XNOR-based boundary circuit appears to be simple, generic and low power design solution to interface quasi-adiabatic circuit to conventional CMOS circuit.

3. The output of the boundary circuit is not clean when it is driven by sinusoidal output signals from quasi-adiabatic circuits; it has glitches. These glitches can be avoided with the help of D flip-flop.

4. This problem is not observed in case of adiabatic circuits driven by ramp type of power-clock and hence D flip-flop is not required.
6.3 Conclusions

In this chapter, we presented two totally new design ideas for improving the performance of quasi-adiabatic circuits. Both the circuits viz. ‘Leakage Power Reduction Circuit’ and ‘Partially Reversible Boundary Circuit’ can be deployed with any quasi-adiabatic logic style. These two designs are important contributions in the field of quasi-adiabatic circuit theory. Finally, we record our important conclusions and significant contributions in the next chapter.